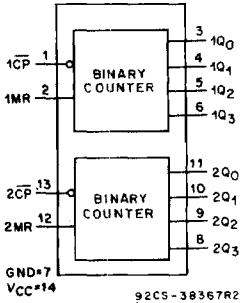
File Number **1653**

CD54/74HC393
CD54/74HCT393

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual 4-Stage Binary Counter

Type Features:

- *Fully static operation*
- *Buffered inputs*
- *Common reset*
- *Negative-edge clocking*
- *Typical f_{MAX} = 60 MHz @ V_{CC} = 5V, C_L = 15 pF, T_A = 25° C*

The RCA-CD54/74HC393 and CD54/74HCT393 are 4-stage ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of the stage advances one count on the negative transition of each clock pulse; a high voltage level on the MR line resets all counters to their zero state. All inputs and outputs are buffered.

The CD54HC393 and CD54HCT393 are supplied in 14-lead *hermetic dual-in-line ceramic packages* (F suffix). The CD74HC393 and CD74HCT393 are supplied in 14-lead *dual-in-line plastic package* (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity: N_{IL}=30%, N_{IH}=30% of V_{CC} @ V_{CC}=5 V
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  V_{IL}=0.8 V max., V_{IH}=2 V min.
  CMOS input compatibility
  $I_{IN} \leq 1\ \mu A$ @ V_{OL}, V_{OH}

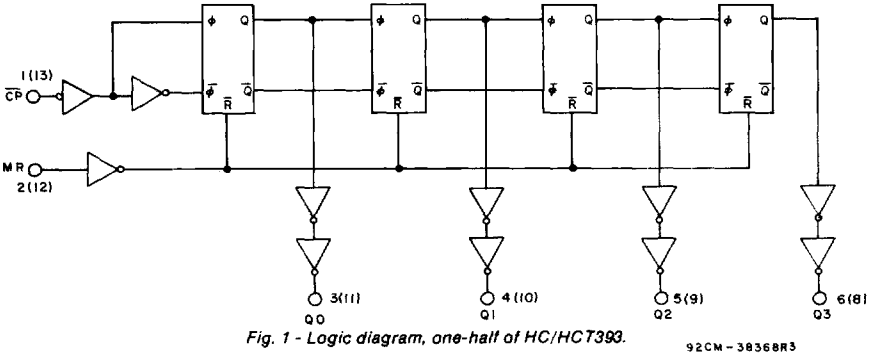


Fig. 1 - Logic diagram, one-half of HC/HCT393.

CD54/74HC393
CD54/74HCT393

MAXIMUM RATINGS, *Absolute-Maximum Values:*

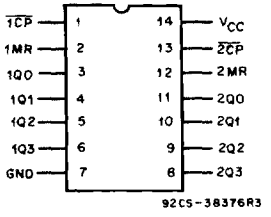
DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\ V < V_O < V_{CC}$ +0.5 V) ..... ±25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}) ..... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.



TERMINAL ASSIGNMENT

CD54/74HC393
CD54/74HCT393

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC393/CD54HC393										CD74HCT393/CD54HCT393										UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE			
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	-25°C			-40/ +85°C		-55/ +125°C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—		V
			4.5	3.15	—	—	3.15	—	3.15	—											
			6	4.2	—	—	4.2	—	4.2	—											
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8		V
			4.5	—	—	1.35	—	1.35	—	1.35											
			6	—	—	1.8	—	1.8	—	1.8											
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—		V
			4.5	4.4	—	—	4.4	—	4.4	—											
			6	5.9	—	—	5.9	—	5.9	—											
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—		V
		-5.2	6	5.48	—	—	5.34	—	5.2	—											
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1		V
			4.5	—	—	0.1	—	0.1	—	0.1											
			6	—	—	0.1	—	0.1	—	0.1											
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4		V
		5.2	6	—	—	0.26	—	0.33	—	0.4											
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1		μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160		μA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490		μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
$n\overline{CP}$	0.4
nMR	1

*Unit load is Δ I_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC393
CD54/74HCT393

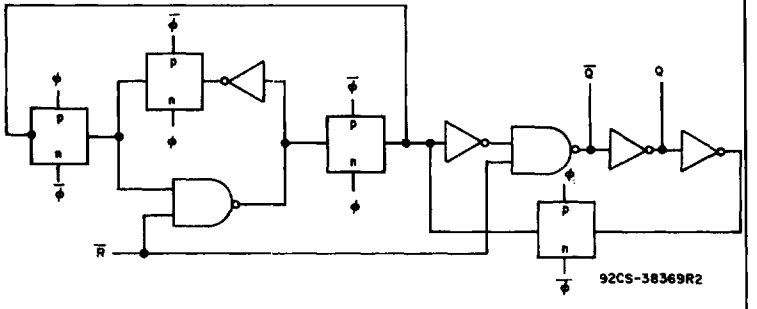


Fig. 2 - Flip-flop logic detail.

TRUTH TABLES

CP COUNT	OUTPUTS Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

CP	MR	OUTPUT
⌐	L	NO CHANGE
⌐	L	COUNT
X	H	L L L L

X = Don't Care

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L pF	Typical HC	HCT	Units
Propagation Delay n$\overline{CP}$ to nQ0 Output	t_{PLH} t_{PHL}	15	12	13	ns
Propagation Delay Qn to Qn + 1	t_{PLH} t_{PHL}	15	4	4	ns
Propagation Delay MR to Qn Output	t_{PHL}	15	11	13	ns
Power Dissipation Capacitance*	C_{PD}	—	20	21	pF

*C_{PD} is used to determine the power consumption.
$PD=C_{PD}\ V_{CC}^2\ fi + \Sigma\ (C_L\ V_{CC}^2\ fi/M)$ where: $M=2^1,2^2,2^3,2^4$
C_L=output load capacitance
fi=input frequency

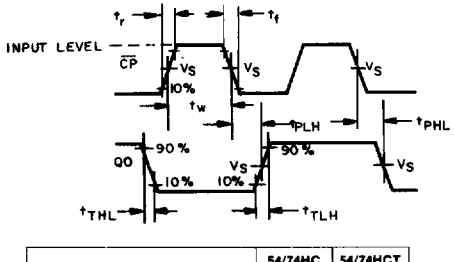
Pre-requisite for Switching Function

CHARACTERISTIC	SYMBOL	V_{CC}	25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Maximum Clock Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	27	—	24	—	22	—	20	—	18	—	
		6	35	—	—	—	28	—	—	—	24	—	—	—	
Clock Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	19	—	20	—	24	—	24	—	29	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Reset Recovery Time	t_{REC}	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
		4.5	5	—	5	—	5	—	5	—	5	—	5	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	
Reset Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	

CD54/74HC393
CD54/74HCT393

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Time: Qn to Qn+1	t_{PLH}	2	—	45	—	—	—	55	—	—	—	70	—	—	ns
	t_{PHL}	4.5	—	9	—	12	—	11	—	15	—	14	—	18	
		6	—	8	—	—	—	9	—	—	—	12	—	—	
nC̄P to nQ0	t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
	t_{PHL}	4.5	—	30	—	32	—	38	—	40	—	45	—	48	
		6	—	26	—	—	—	33	—	—	—	38	—	—	
nC̄P to nQ1	t_{PLH}	2	—	190	—	—	—	245	—	—	—	295	—	—	
	t_{PHL}	4.5	—	38	—	32	—	49	—	55	—	59	—	66	
		6	—	33	—	—	—	42	—	—	—	50	—	—	
nCP to nQ2	t_{PLH}	2	—	240	—	—	—	300	—	—	—	360	—	—	
	t_{PHL}	4.5	—	48	—	50	—	60	—	70	—	72	—	84	
		6	—	41	—	—	—	51	—	—	—	61	—	—	
nC̄P to nQ3	t_{PLH}	2	—	285	—	—	—	355	—	—	—	430	—	—	
	t_{PHL}	4.5	—	57	—	62	—	71	—	85	—	86	—	102	
		6	—	48	—	—	—	60	—	—	—	73	—	—	
MR to Qn	t_{PLH}	2	—	135	—	—	—	170	—	—	—	205	—	—	
	t_{PHL}	4.5	—	27	—	32	—	34	—	40	—	41	—	48	
		6	—	23	—	—	—	29	—	—	—	35	—	—	
Output Transition Time	t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	
	t_{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF



	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3 V
SWITCHING VOLTAGE, V_S	50% V_{CC}	1.3 V

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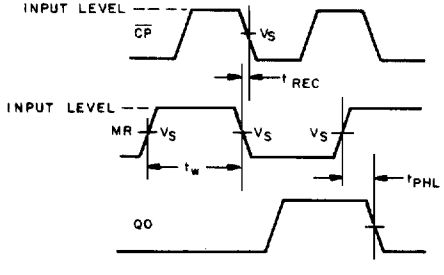
Fig. 3 - Clock pre-requisite, propagation-delay, and output-transition times.



	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3 V
SWITCHING VOLTAGE, V_S	50%	1.3 V

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Fig. 4 - Master-Reset pre-requisite and propagation-delay times.