Rochester Electronics

Datasheet

PART NUMBER

5475BEA-ROCS

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL,
TTL, BISTABLE LATCHES, MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, TTL, 4-bit bistable latch microcircuits. Three product assurance classes and a choice of case outline/lead finish are provided for each type and are reflected in the complete part number.

1.2 Part number. The complete part number shall be in accordance with MIL-M-38510.

1.2.1 Device type. Device type shall be as shown in the following:

Device type	Circuit
01	4-Bit latch, complementary outputs
02	4-Bit latch
03	Dual, 4-bit latch
04	4-Bit latch, master reset

1.2.2 Device class. Device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

Case outline letter	MIL-M-38510, appendix C, case outline
A	F-1 (14-lead, 1/4" x 1/4", flat pack)
B	F-3)14-lead, 1/4" x 1/8", flat pack)
C	D-1 (14-lead, 1/4" x 3/4", dual-in-line pack)
D	F-2 (14-lead, 1/4" x 3/8", flat pack)
E	D-2 (16-lead, 1/4" x 7/8", dual-in-line pack)
F	F-5 (16-lead, 1/4" x 3/8", flat pack)
J	D-3 (24-lead, 1/2" x 1/4", dual-in-line pack)
K	F-6 (24-lead, 3/8" x 1/2", flat pack)
L	F-7 (24-lead, 3/8" x 1/2", flat pack)
Z	F-8 (24-lead, 1/4" x 3/8", flat pack)

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 to 7.0 Vdc
Input voltage range	-1.5 Vdc at 12 mA to 5.5 Vdc
Storage temperature range	-65° to 150°C
Maximum power dissipation, P_D 1/	
Device types 01 and 02	280 mW
Device type 03	630 mW
Device type 04	325 mW

1/ Must withstand the added P_D due to short circuit condition (e.g. I_{OS}) at one output for 5 seconds duration.

Beneficial comments (recommendations, additions, deletions) any and pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center ATTN: RADC (RBE-2) Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

Lead temperature (soldering, 10 seconds)		300°C
Thermal resistance, junction to case	θ_{JC}	= 0.15°C/mW for flat pack 0.08°C/mW for dual-in-line pack
Junction temperature	T_J	= 175°C

1.4 Recommended operating conditions.

Supply voltage	4.5 Vdc minimum to 5.5 Vdc maximum
Minimum high level input voltage	2.0 Vdc
Maximum low level input voltage	0.8 Vdc
Normalized fanout (each output) 1/	5 maximum
Ambient operating temperature range	-55° to 125°C
Setup time, $t_{(SETUP)}$	
Types 01 and 02	25 ns, minimum
Setup time, $t_{(SETUP)}$, type 03	
Data to enable (high)	10 ns, minimum
Data to enable (low)	16 ns, minimum
Setup time, $t_{(SETUP)}$, type 04	
Data to enable (high)	5 ns, minimum
Data to enable (low)	25 ns, minimum
Setup time, $t_{(SETUP)}$, type 04	
Data to set (high)	8 ns, minimum
Input hold time, $t_{(HOLD)}$, types 01 and 02	
Clock to data	5 ns, minimum
Data to clock	35 ns, minimum
Input hold time, $t_{(HOLD)}$, type 03	
Data to enable (high)	0 ns, maximum
Data to enable (low)	4 ns, maximum
Input hold time, $t_{(HOLD)}$, type 04	
Data to enable (high)	0 ns, maximum
Data to enable (low)	7 ns, maximum
Input hold time, $t_{(HOLD)}$, type 04	
Data to set (low)	8 ns, maximum

2. APPLICABLE DOCUMENTS

2.1 Issues of documents. The following documents of the issue in effect on date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

1/ Device will fanout in both high and low levels to the specified number of inputs of the same device type as that being tested.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline. Case outline shall be as specified in 1.2.3 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables and logic equations. The truth tables and logic equations shall be as specified on figure 2.

3.2.4 Schematic circuits and logic diagrams. The schematic circuits and logic diagrams shall be as specified on figure 3.

3.3 Lead material and finish. Lead material and finish shall be in accordance with MIL-M-38510 (see 6.6).

3.4 Electrical performance characteristics. The electrical performance characteristics are specified in table I, and apply over the full recommended ambient operating temperature range, unless otherwise specified.

3.5 Rebonding. Rebonding shall be in accordance with MIL-M-38510.

3.6 Electrical test requirements. Electrical test requirements shall be as specified in table III for the applicable device type and device class. The subgroups of table III which constitute the minimum electrical test requirements for screening, qualification, and quality conformance by device class are specified in table II.

3.7 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2. At the option of the manufacturer, the following marking may be omitted from the body of the microcircuit, but shall be retained on the initial container.

a. Country of origin.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 5 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

4.3 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).
   (1) Test condition D or E, using the circuit shown on figure 4, or equivalent.
   (2) T_A = 125°C minimum.

b. Interim and final electrical test parameters shall be as specified in table II, except the interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
c. Percent defective allowable (PDA) - The PDA for class S devices shall be as specified in MIL-M-38510. The PDA for class B devices shall be 10 percent based on failures from group A, subgroup 1 test after cool-down as final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

a. Tests shall be as specified in table II.
b. Subgroups 4, 5, 6, 7, and 8 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

a. End point electrical parameters shall be as specified in table II herein.
b. Subgroups 3 and 4 shall be added to the group C inspection requirements for class C devices and shall consist of the tests, conditions, and limits specified for subgroups 10 and 11 of group A.
c. Operating life-test (method 1005 of MIL-STD-883) conditions, or equivalent:
   (1) Test conditions D or E, using the circuit shown on figure 4, or equivalent.
   (2) T_A = 125°C, minimum.
   (3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows:

a. End point electrical parameters shall be as specified in table II herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions		Device types	Limits Min	Limits Max	Unit
High-level output voltage	V_{OH}	V_{CC} = 4.5 V; V_{IN} = 0.8 V	I_{OH} = -400 µA	01,02	2.4		Volts
			I_{OH} = -800 µA	03,04	2.4		Volts
Low-level output voltage	V_{OL}	V_{CC} = 4.5 V; V_{IN} = 2.0 V	I_{OL} = 16 mA	01,02,04		0.4	Volts
			I_{OL} = 14.4 mA	03		0.4	Volts
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V; V_{IN} = -12 mA		All		-1.5	Volts
Low-level input current, data	I_{IL1}	V_{CC} = 5.5 V; V_{IN} = 0.4 V		01,02	-1.4	-3.2	mA
				03 4/	-0.5	-2.4	mA
				04	-0.7	-2.7	mA
Low-level input current	I_{IL2}	V_{CC} = 5.5 V; V_{IN} = 0.4 V 1/					
Clock				01,02	-2.8	-6.4	mA
Master reset and enable				03,04	-0.7	-1.6	mA
Set				04	-0.7	-1.6	mA
High-level input current, data	I_{IH1}	V_{CC} = 5.5 V; V_{IN} = 2.4 V 1/		01,02		80	µA
				03		40	µA
				04		60	µA
High-level input current, data	I_{IH2}	V_{CC} = 5.5 V; V_{IN} = 5.5 V 1/		01,02		200	µA
				03,04		100	µA
High-level input current	I_{IH3}	V_{CC} = 5.5 V; V_{IN} = 2.4 V 1/					
Clock				01,02		160	µA
Master reset and enable				03,04		40	µA
Set				04		40	µA
High-level input current	I_{IH4}	V_{CC} = 5.5 V; V_{IN} = 5.5 V 1/					
Clock				01,02		400	µA
Master reset and enable				03,04		100	µA
Set				04		100	µA
Short-circuit output current	I_{OS}	V_{CC} = 5.5 V 2/ 3/		01,02	-20	-57	mA
				03 5/	-10	-70	mA
				04	-20	-100	mA
Supply current	I_{CC}	V_{CC} = 5.5 V 2/; V_{IN} = 4.5 V		01, 02		46	mA
				03		106	mA
				04		55	mA
Propagation delay time for types 01 and 02							
To high level, from D input to Q output	t_{PLH1}	C_L = 50 pF ±10%; R_L = 390 ohms ±5%		01,02	2	44	ns
To high level, from D input to $\overline{Q}$ output	t_{PLH2}			01	2	55	ns
To low level, from D input to Q output	t_{PHL1}			01,02	2	38	ns
To low level, from D input to $\overline{Q}$ output	t_{PHL2}			01	2	25	ns
To low level, from clock input to Q output	t_{PHL3}			01	2	25	ns
To high level, from clock input to Q output	t_{PLH3}			01,02	2	44	ns
To low level, from clock input to $\overline{Q}$ output	t_{PHL4}			01	2	25	ns
To high level from clock input to $\overline{Q}$ output	t_{PLH4}			01	2	44	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued

Test	Symbol	Conditions	Device types	Limits Min	Limits Max	Unit
Propagation delay time for types 03 and 04						
To high level, from enable to output	t_{PLH1}	C_L = 50 pF ±10%; R_L = 390 ohms ±5%	03,04	3	60	ns
To low level, from enable to output	t_{PHL1}		03,04	3	40	ns
To high level, from data to output	t_{PLH2}		03,04	3	49	ns
To low level, from data to output	t_{PHL2}		03,04	3	37	ns
To low level, from master reset to output	t_{PHL3}		03,04	3	37	ns
To high level, from set to output	t_{PLH4}		04	9	47	ns

1/ All unspecified inputs at 5.5 volts.
2/ All unspecified inputs grounded.
3/ Not more than one output should be shorted at a time.
4/ Circuit B limits for I_{IL1} shall be -1.6 mA, maximum.
5/ Circuit B and C limits for I_{OS} shall be -20 mA minimum to -57 mA maximum.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III) Class S devices	Class B devices	Class C devices
Interim electrical parameters (pre burn-in) (Method 5004)	1	1	None
Final electrical test parameters (Method 5005)	1*, 2, 3, 9, 10, 11	1*, 2, 3, 9	1
Group A test requirements (Method 5005)	1, 2, 3, 9, 10, 11	1, 2, 3, 9	1, 2, 3, 9
Group C end point electrical parameters (Method 5005)	N/A	1, 2, 3	1
Additional electrical subgroups for group C periodic inspection	N/A	10, 11	10, 11
Group D end point electrical parameters (Method 5005)	1, 2, 3	1, 2, 3	1

* PDA applies to subgroup 1 (see 4.3c).

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Life test and burn-in cooldown procedure. When devices are measured at 25°C following application of the operating life or burn-in test condition, they shall be cooled to room temperature prior to removal of bias. Alternately, the bias may be removed during cooling, if the case temperature is reduced to room temperature within 30 minutes after removal of the test condition.

4.6 Inspection of packaging. Inspection of packaging shall be in accordance with MIL-M-38510, except that the rough handling test shall not apply.

5. PACKAGING

5.1 Packaging requirements. The requirements for the packaging of microcircuits shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use for Government microcircuit applications (original equipment) and logistic support.

6.3 Ordering data. The contract should specify the following:

a. Complete part number (see 1.2).
b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
c. Requirement for certificate of compliance, if applicable.
d. Requirements for notification of change of product or process to procuring activity in addition to notification to the qualifying activity, if applicable.
e. Requirements for preservation and packing.
f. Requirements for failure analysis (including required test condition of method 5003), corrective action and reporting of results, if applicable.
g. Requirements for product assurance options.
h. Requirements for carriers, special lead lengths or lead forming, if applicable. These requirements shall not affect the part number.
i. Requirements for JAN marking.

6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-STD-1331, and as follows:

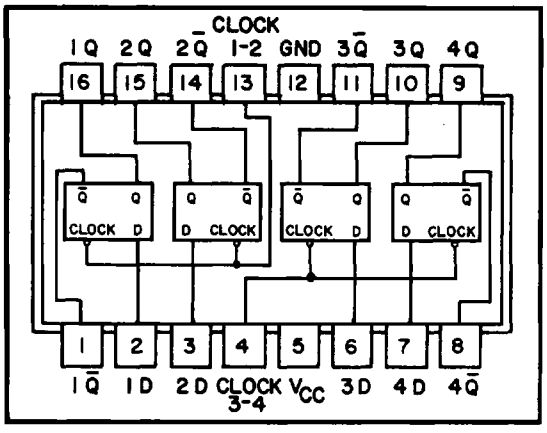
GND - - - - - - - - - Electrical ground (common terminal)
V_{IN} - - - - - - - - - Voltage level at an input terminal

6.5 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

6.6 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits procured for Government logistic support will be procured to device class B (see 1.2.2), lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

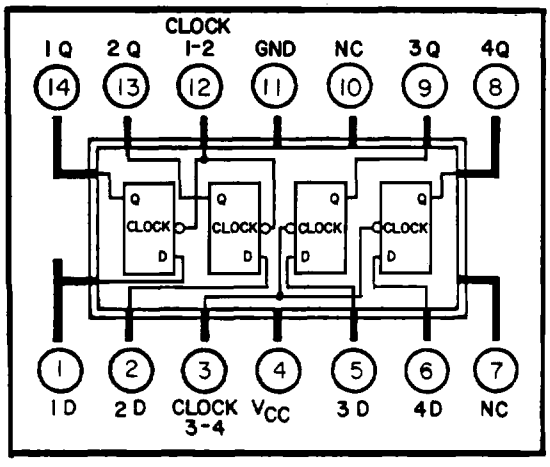
Device type 01

CASES E AND F



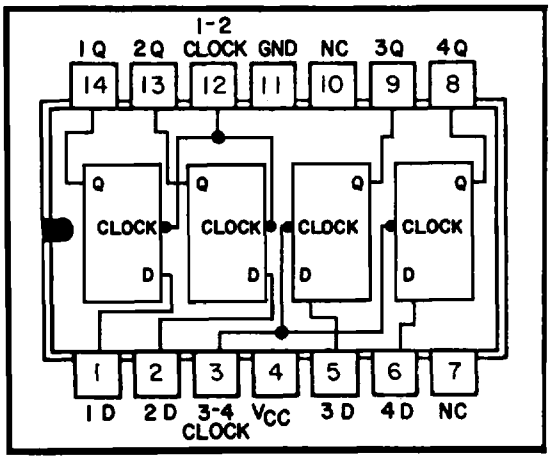
Device type 02

CASES A, B, AND D



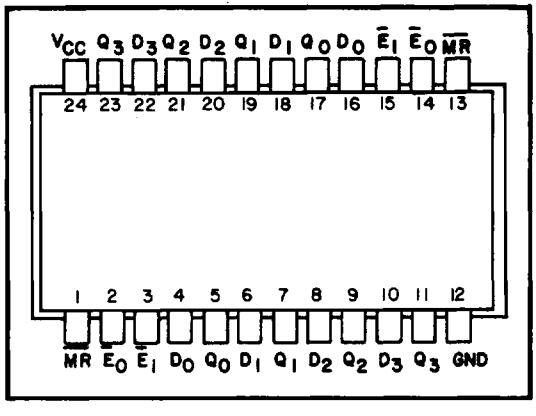
Device type 02

CASES C



Device type 03

CASES J, K, L AND Z



Device type 04

CASES E AND F

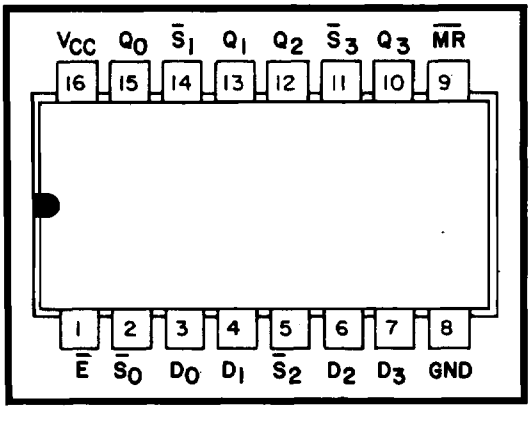


FIGURE 1. Terminal connections.

Device types 01 and 02

Truth table	
t_n	t_{n+1}
D	Q
H	H
L	L

NOTES:
1. t_n = bit time before clock negative-going transition.
2. t_{n+1} = bit time after clock negative-going transition.

Device type 03

Truth table					
$\overline{MR}$	$\overline{E_0}$	$\overline{E_1}$	D	Q_n	Operation
H	L	L	L	L	Data entry
H	L	L	H	H	Data entry
H	L	H	X	Q_{n-1}	Hold
H	H	L	X	Q_{n-1}	Hold
H	H	H	X	Q_{n-1}	Hold
L	X	X	X	L	Reset

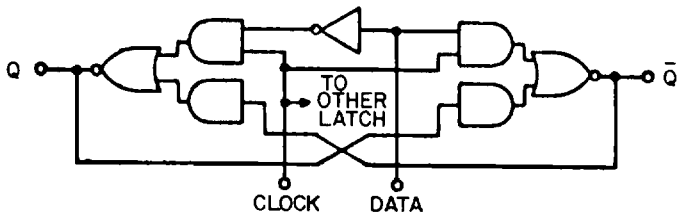
X = Don't care
L = Low voltage level
H = High voltage level
Q_{n-1} = Previous output state
Q_n = Present output state

Device type 04

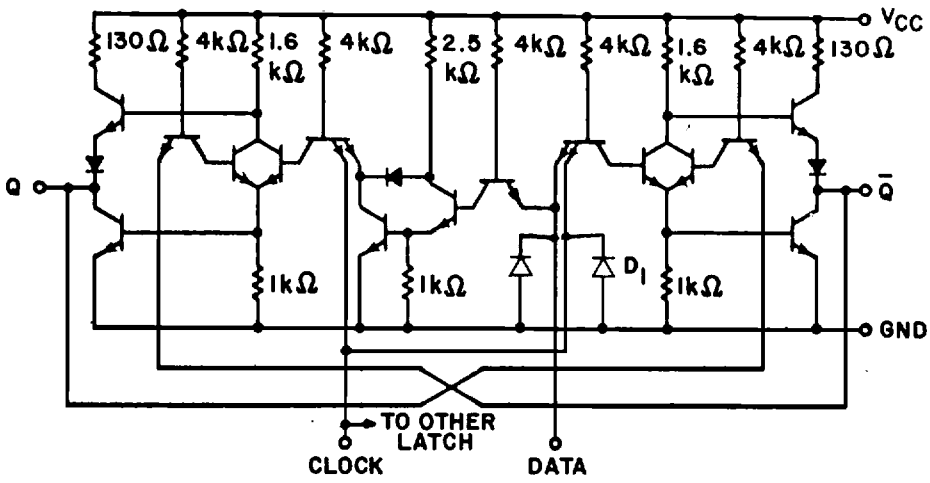
Truth table					
$\overline{MR}$	$\overline{E}$	D	$\overline{S}$	Q_{n-1}	Operation
H	L	L	L	L	D mode
H	L	H	L	H	
H	H	X	X	Q_{n-1}	
H	L	L	L	L	R/S mode
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	Q_{n-1}	
H	H	X	X	Q_{n-1}	
L	X	X	X	L	Reset

X = Don't care
L = Low voltage level
H = High voltage level
Q_{n-1} = Previous output state
Q_n = Present output state

FIGURE 2. Truth tables.

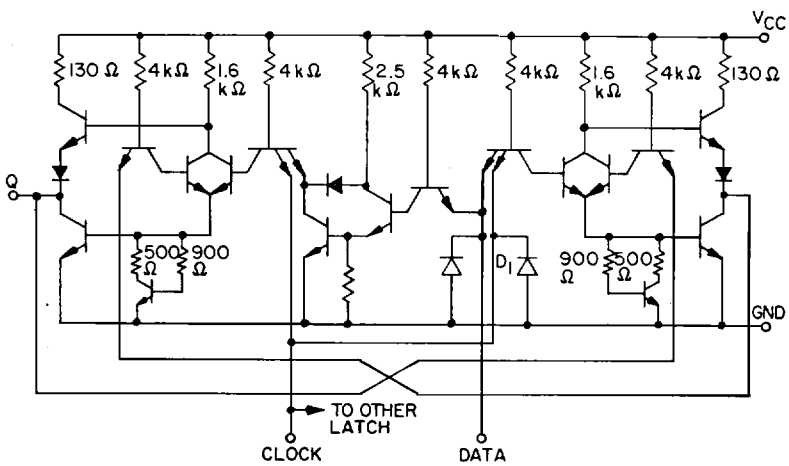


LOGIC DIAGRAM (EACH LATCH)



CIRCUIT A (EACH LATCH)

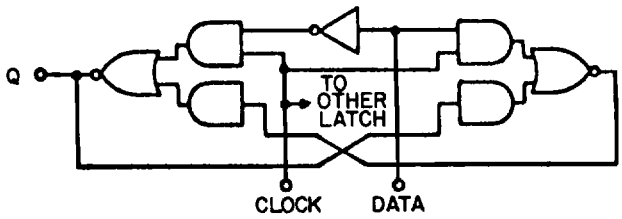
NOTES:
1. All resistance values shown are nominal.
2. D_1 is common to each latch in the pair.



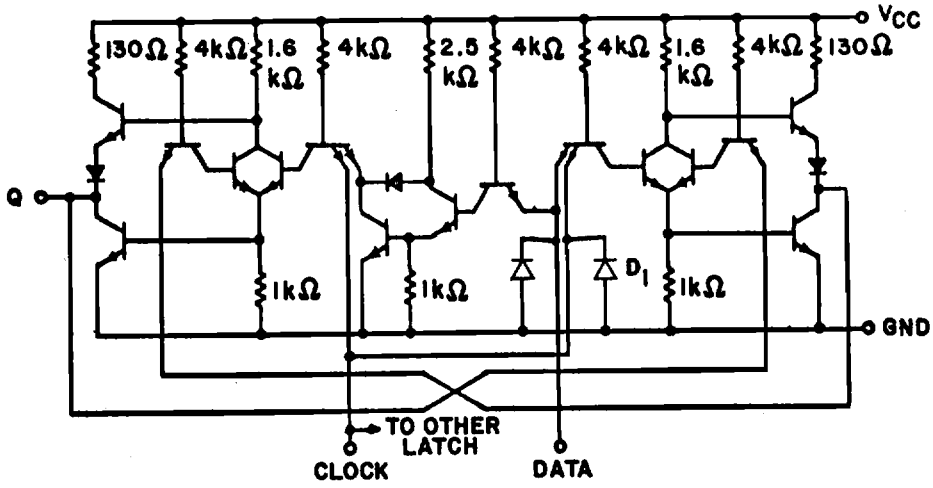
CIRCUIT B (EACH LATCH)

NOTES:
1. All resistance values shown are nominal.
2. D_1 is common to each latch in the pair.

FIGURE 3. Logic diagram and schematic circuits for device type 01.

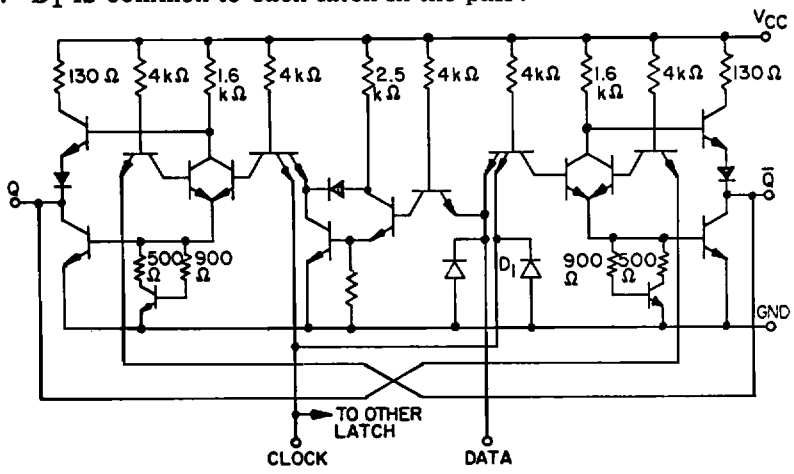


LOGIC DIAGRAM (EACH LATCH)



CIRCUIT A (EACH LATCH)

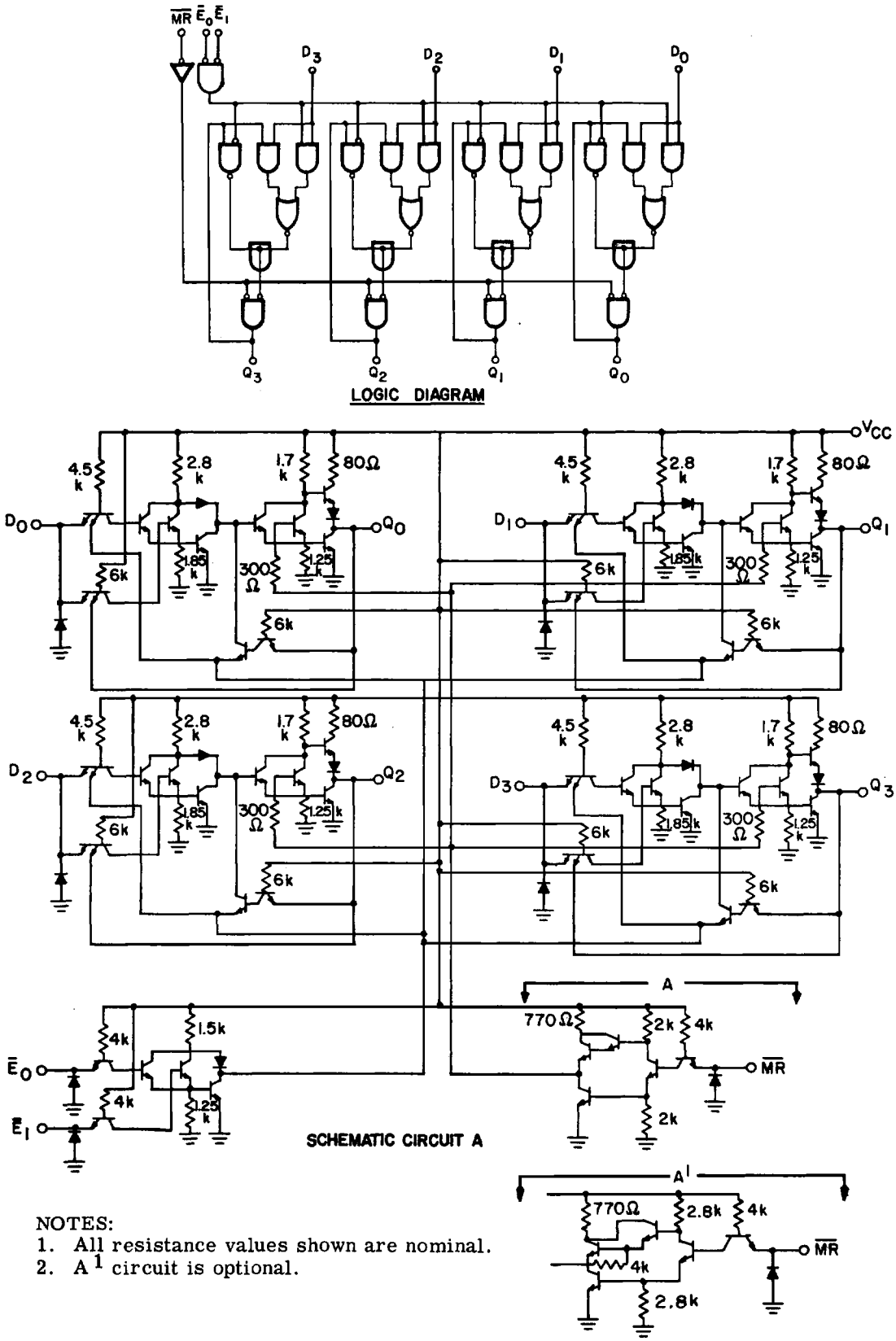
NOTES:
1. All resistance values shown are nominal.
2. D_1 is common to each latch in the pair.



CIRCUIT B (EACH LATCH)

NOTES:
1. All resistance values shown are nominal.
2. D_1 is common to each latch in the pair.

FIGURE 3. Logic diagram and schematic circuits for device type 02 - Continued.



NOTES:
1. All resistance values shown are nominal.
2. A 1 circuit is optional.

FIGURE 3. Logic diagram and schematic circuits for device type 03 - Continued.

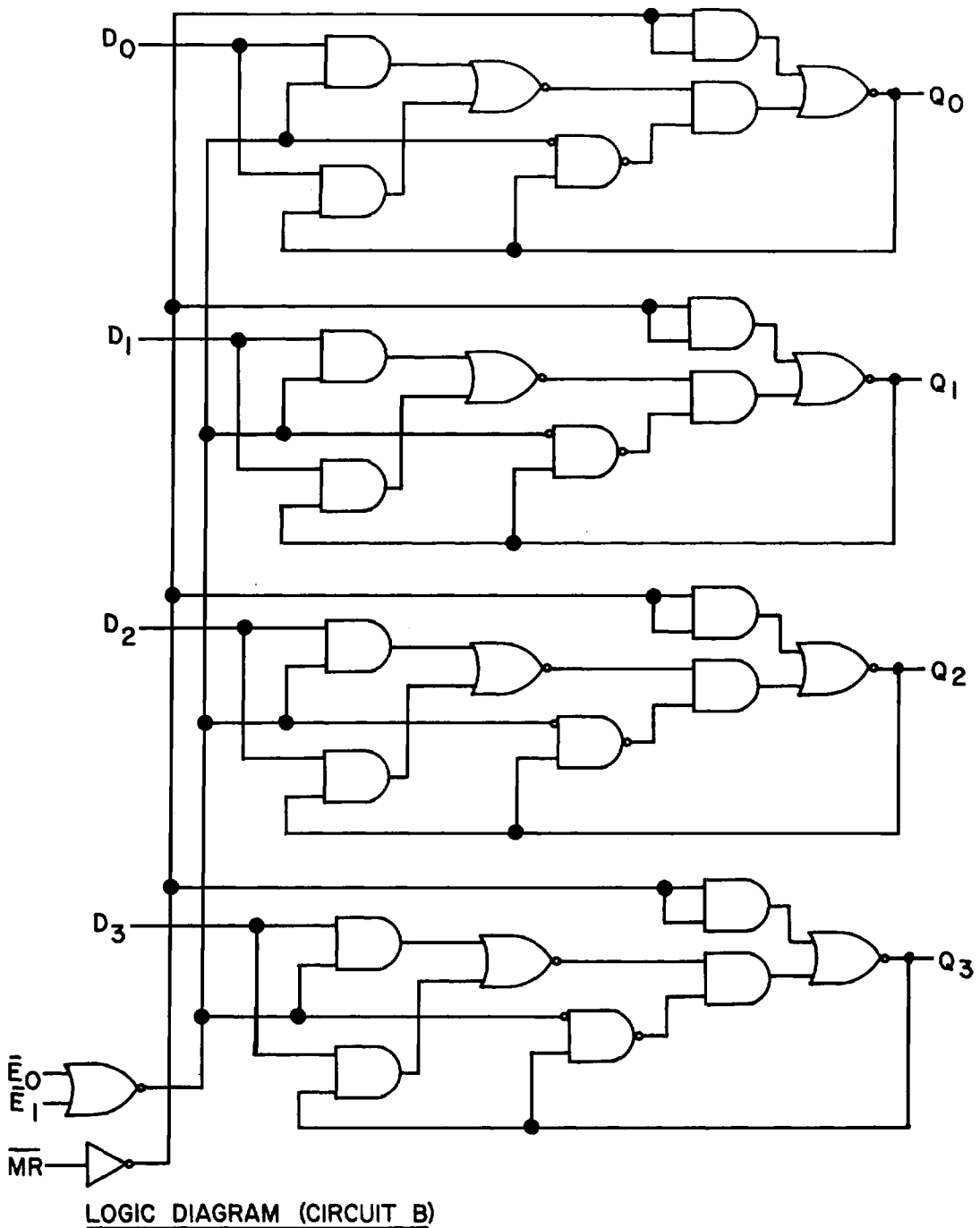


FIGURE 3. Logic diagram and schematic circuits for device type 03 - Continued.

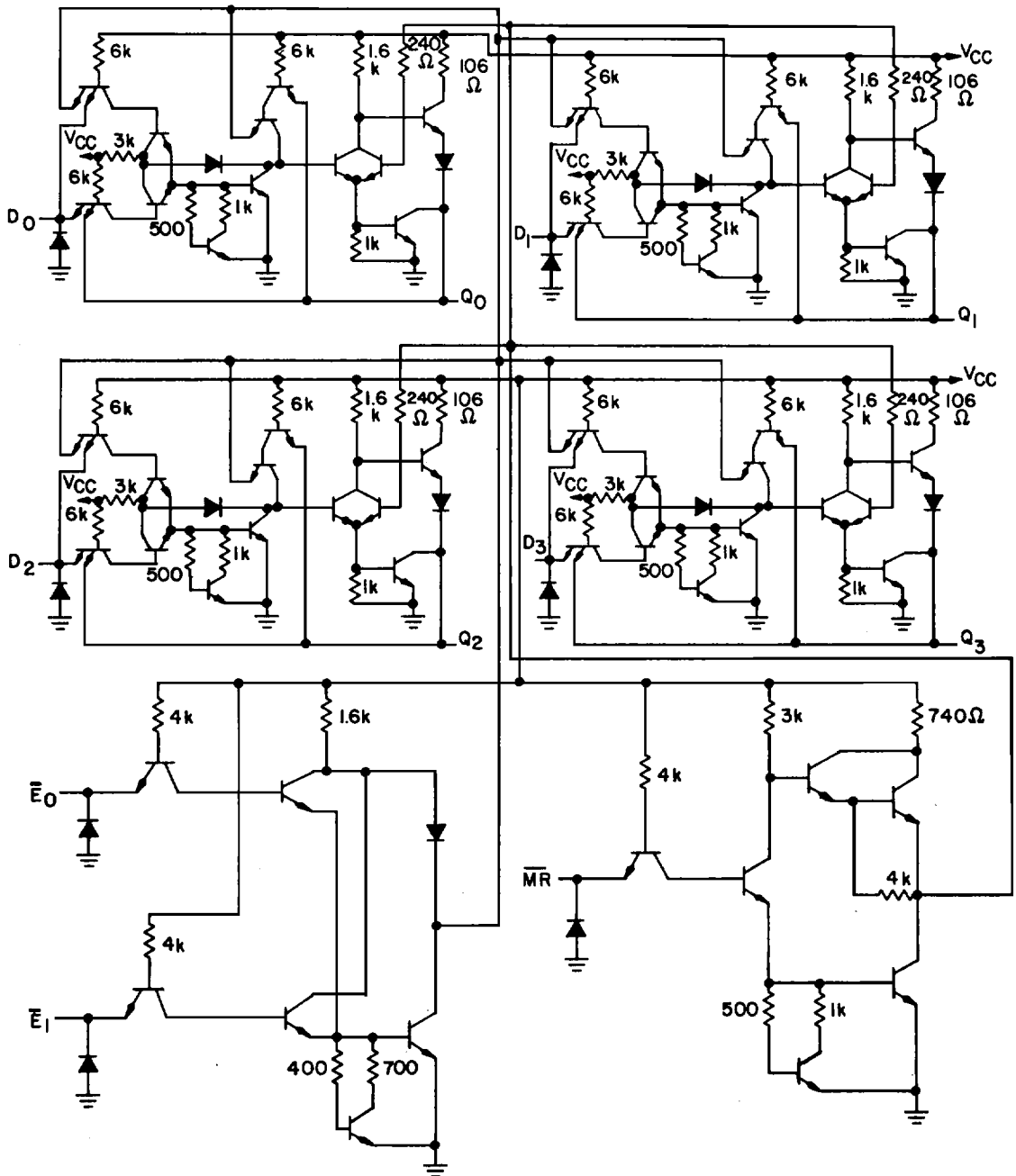
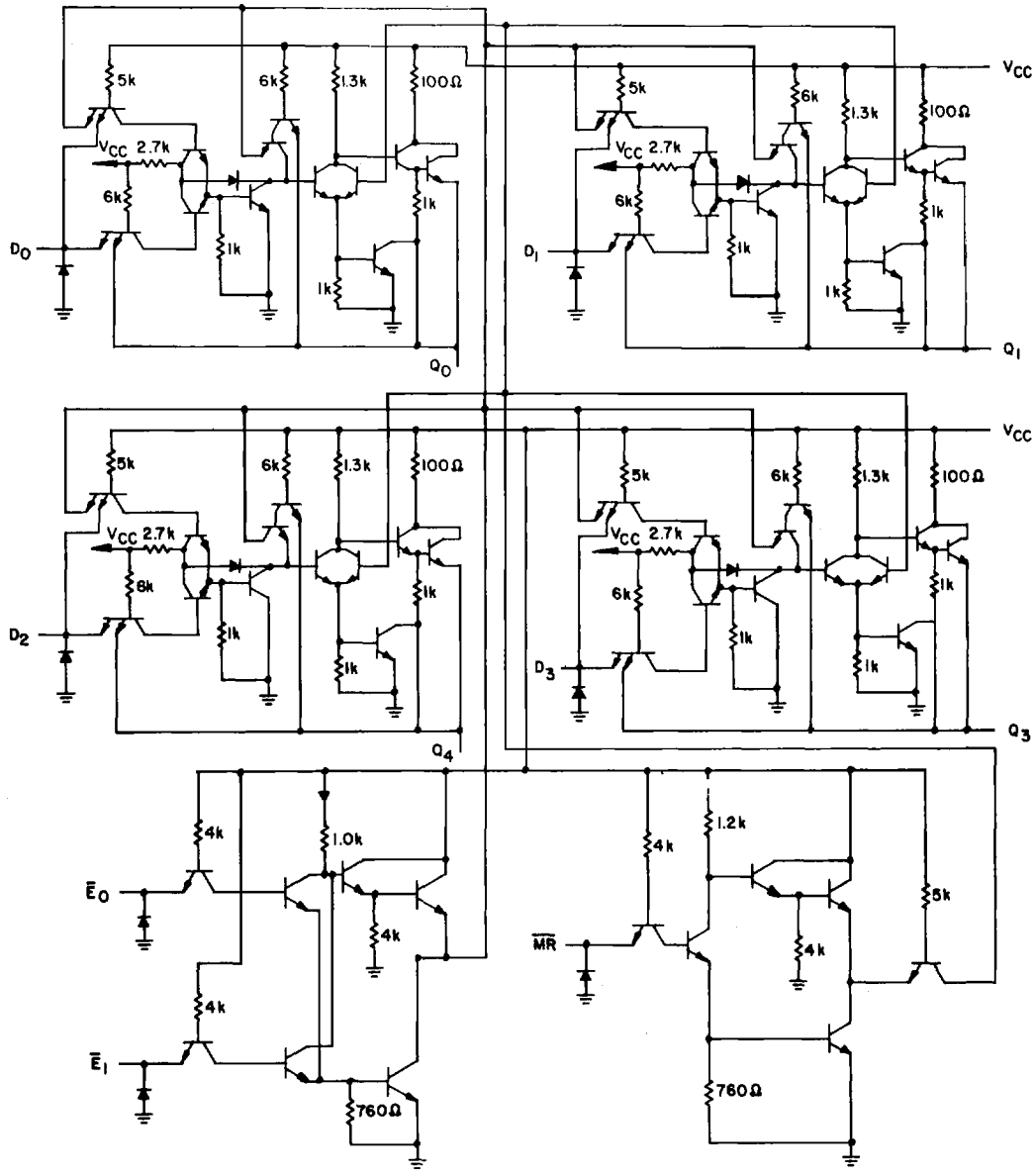
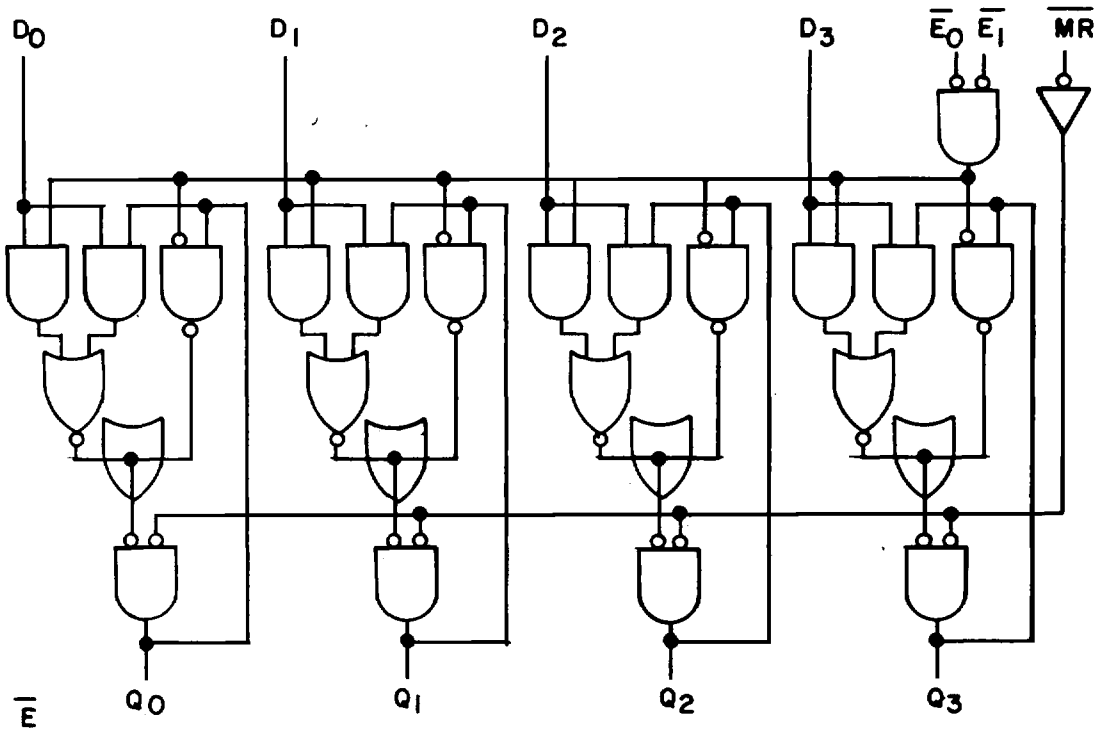


FIGURE 3. Logic diagram and schematic circuits for device type 03 - Continued.

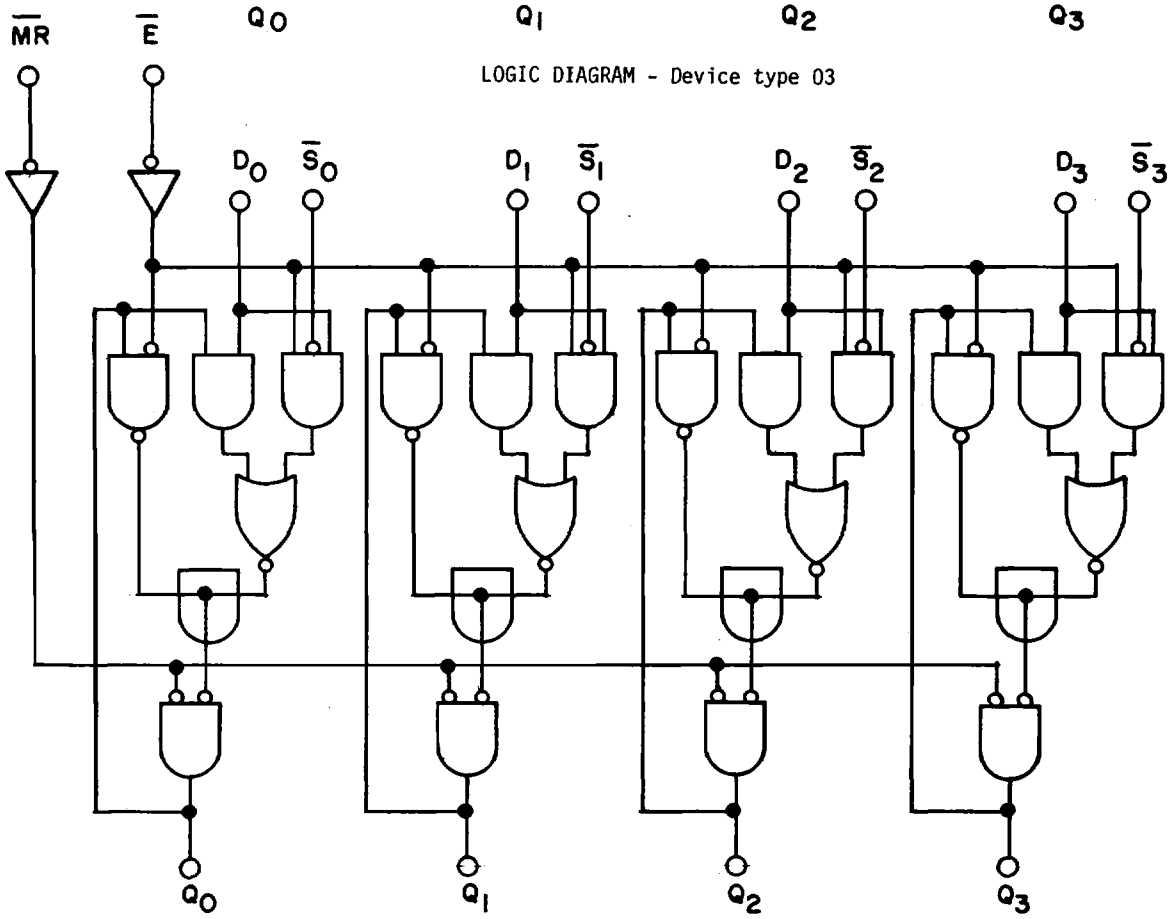


CIRCUIT DIAGRAM (CIRCUIT C)

FIGURE 3. Logic diagram and schematic circuits for device type 03 - Continued.

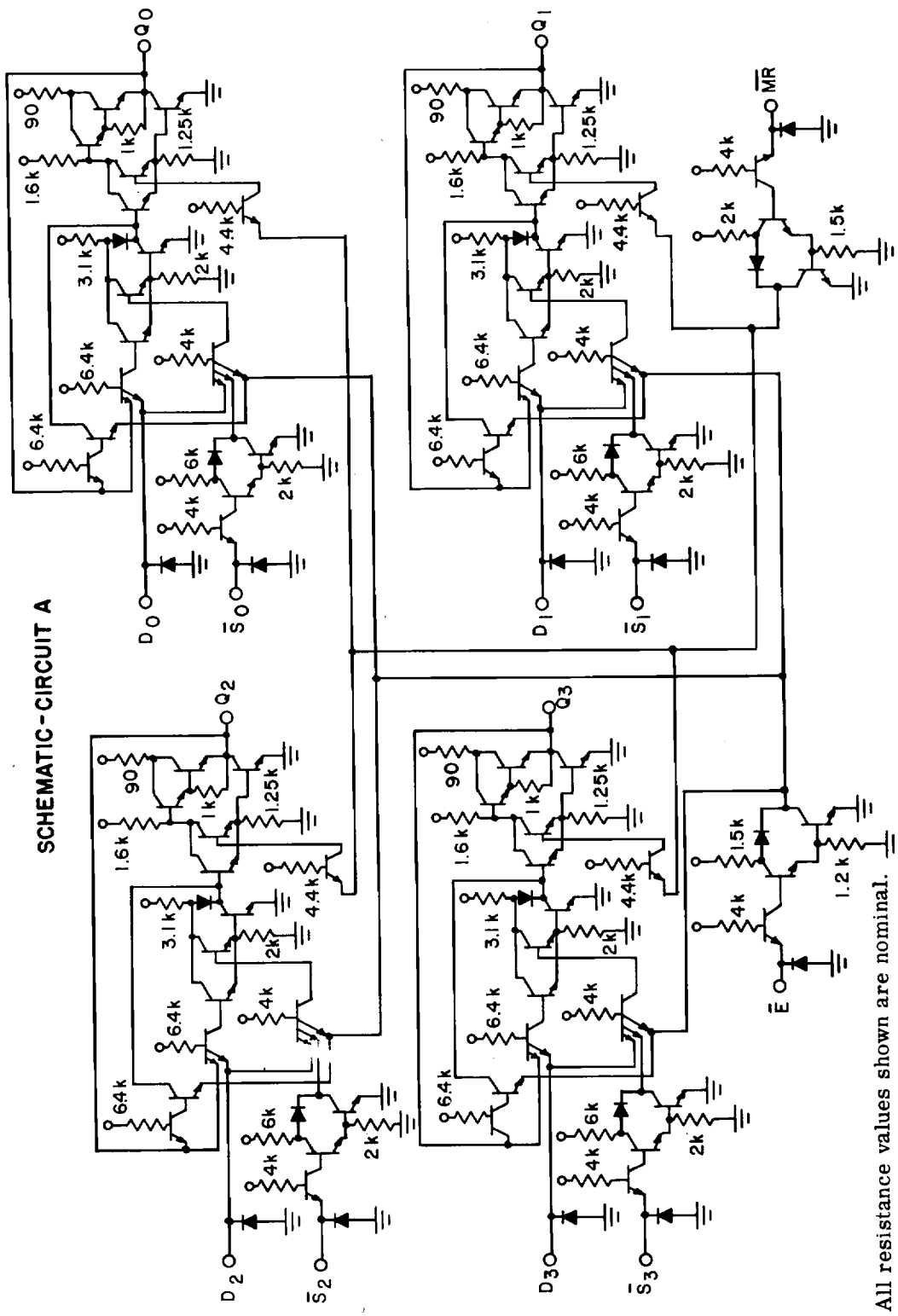


LOGIC DIAGRAM - Device type 03



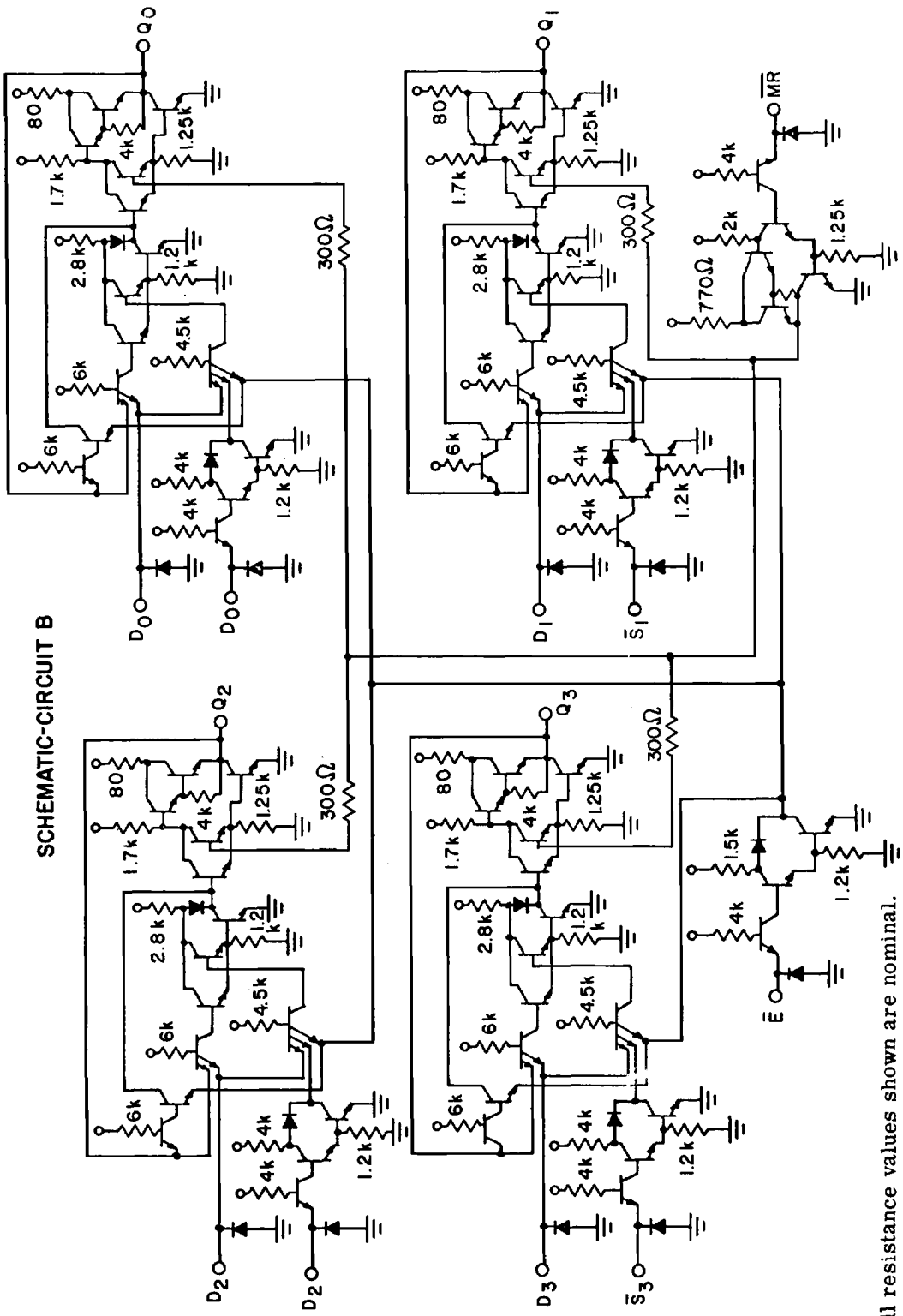
LOGIC DIAGRAM - Device type 04

FIGURE 3. Logic diagram and schematic circuits - Continued.



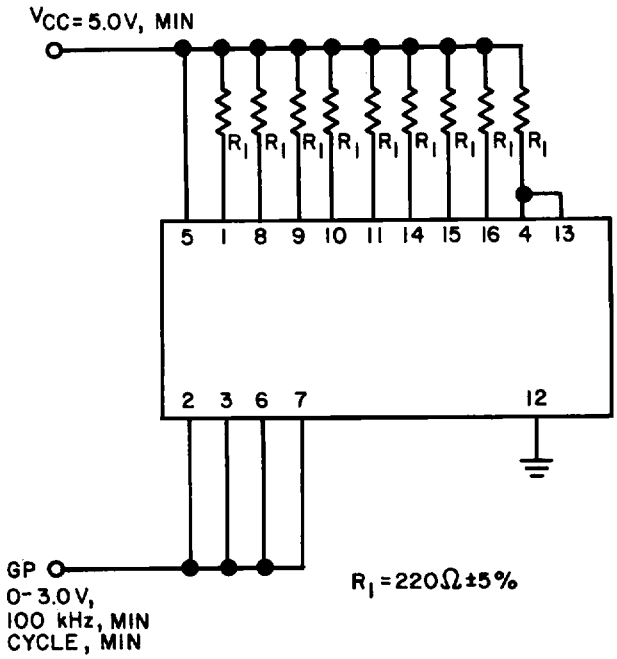
NOTE: All resistance values shown are nominal.

FIGURE 3. Logic diagram and schematic circuits for device type 04 - Continued.

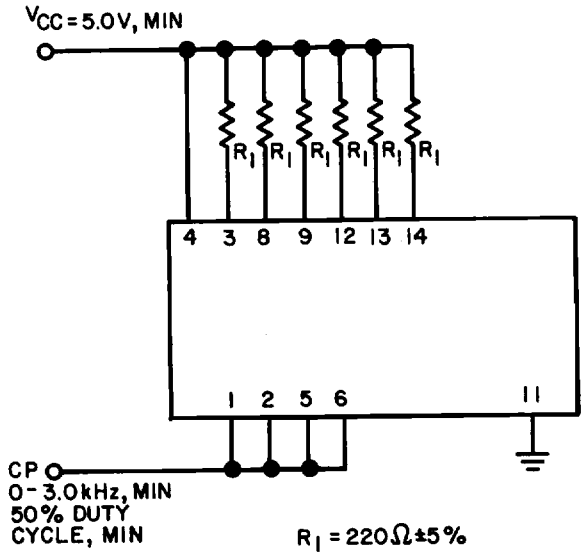


NOTE: All resistance values shown are nominal.

FIGURE 3. Logic diagram and schematic circuits for device type 04 - Continued.

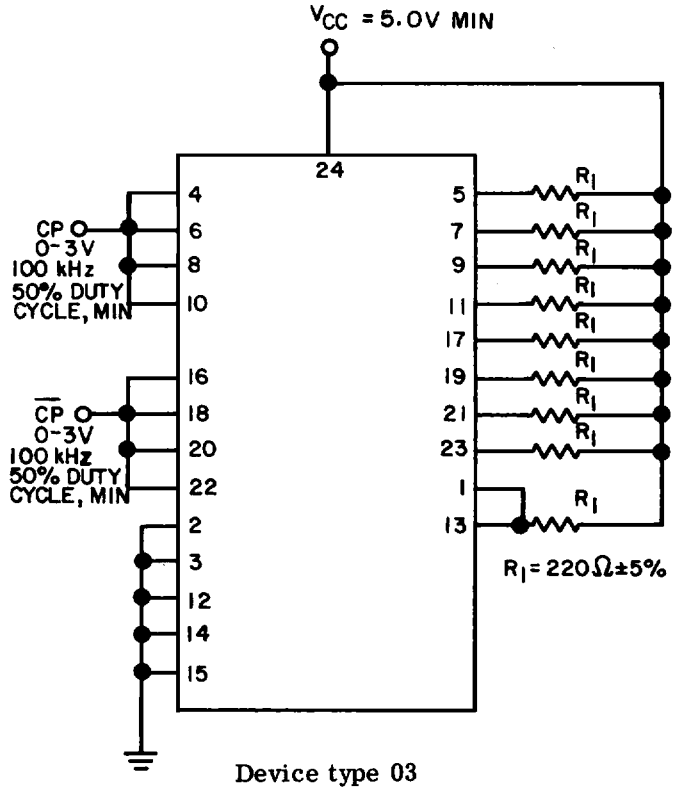


Device type 01

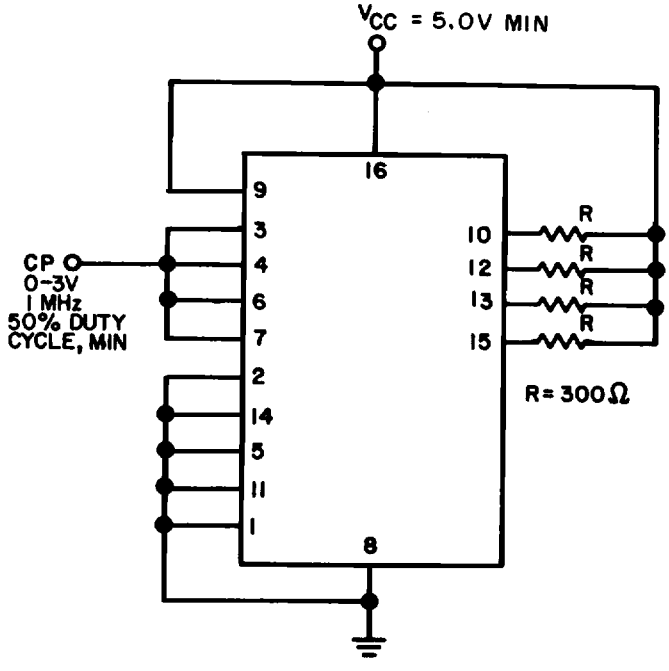


Device type 02

FIGURE 4. Burn-in and life test circuit.

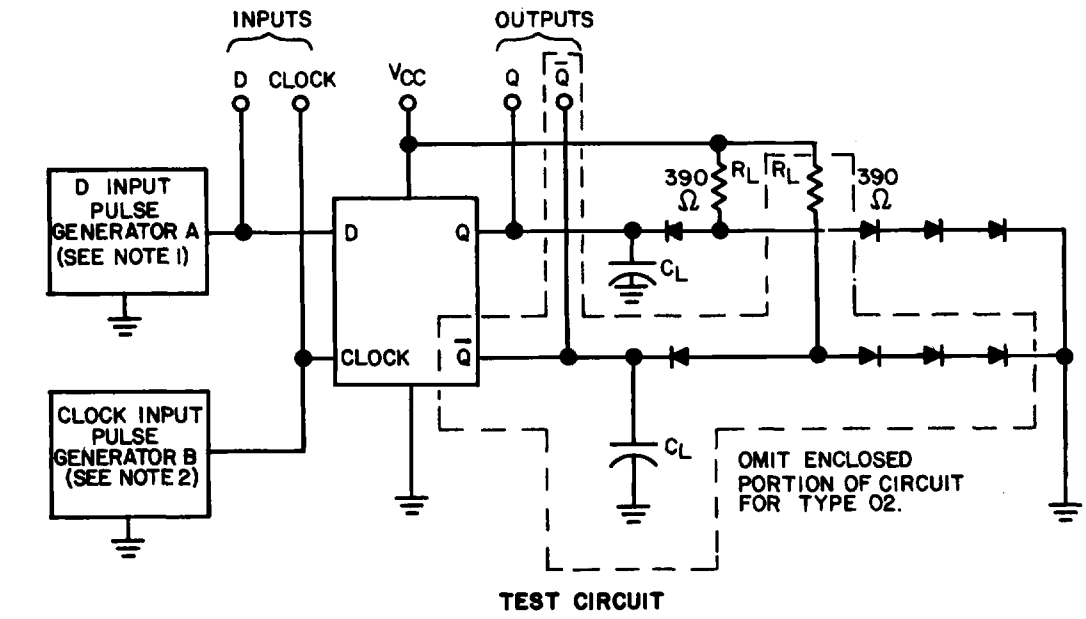


Device type 03

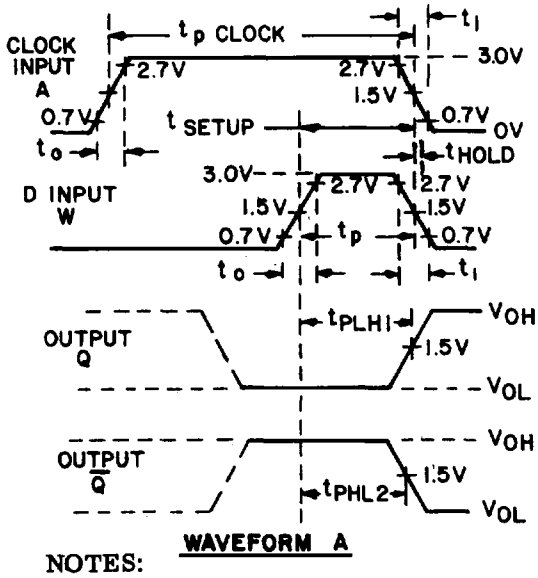


Device type 04

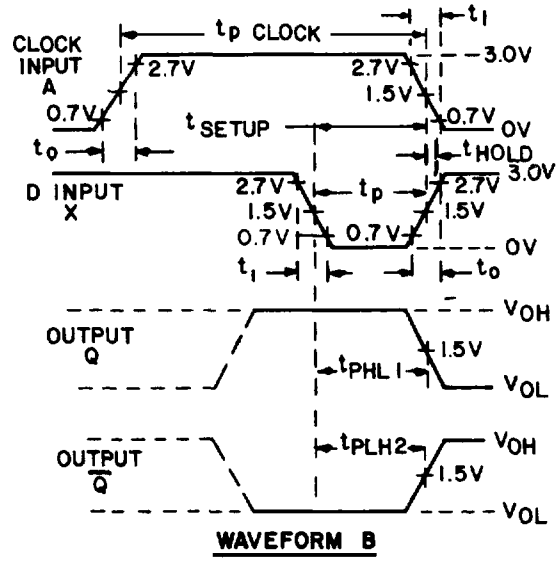
FIGURE 4. Burn-in and life test circuit - Continued.



TEST CIRCUIT



WAVEFORM A

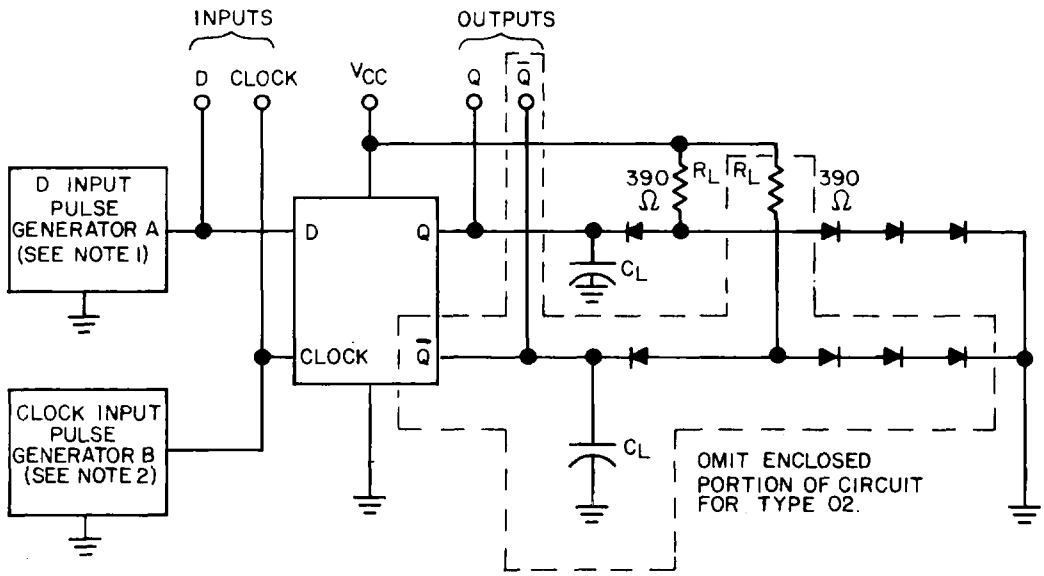


WAVEFORM B

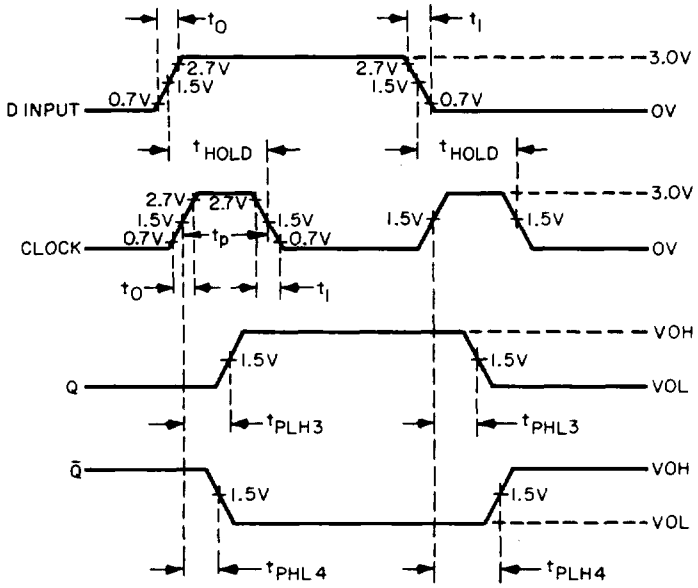
NOTES:

1. The D input pulse generator has the following characteristics: V_{gen} = 3 V, $t_1 = t_0 \leq 10$ ns, t_p = 30 ns, $t_{(setup)}$ = 25 ns, $t_{(HOLD)}$ = 5 ns, PRR = 1 MHz and $Z_{out} \approx 50\ \Omega$.
2. The clock pulse generator has the following characteristics: V_{gen} = 3 V, minimum, $t_1 = t_0 \leq 10$ ns, $t_{p(clock)}$ = 500 ns, and PRR = 1 MHz.
3. Prior to testing the device shall be precondition to a high logic level for waveform A and to a low logic level for waveform B.
4. Each latch is tested separately.
5. C_L = 50 pF, which includes probe and jig capacitance.
6. R_L = 390 Ω ±5%.
7. The $\overline{Q}$ waveforms are not applicable to type 02.
8. All diodes are 1N3064 or equivalent.

FIGURE 5. Switching test circuit and waveforms for device types 01 and 02.



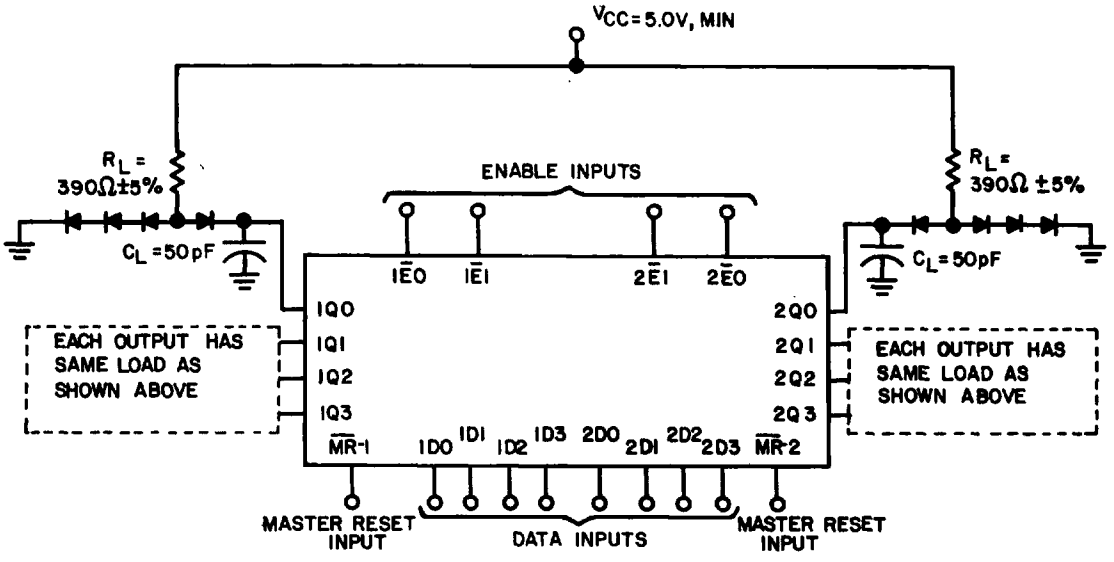
TEST CIRCUIT

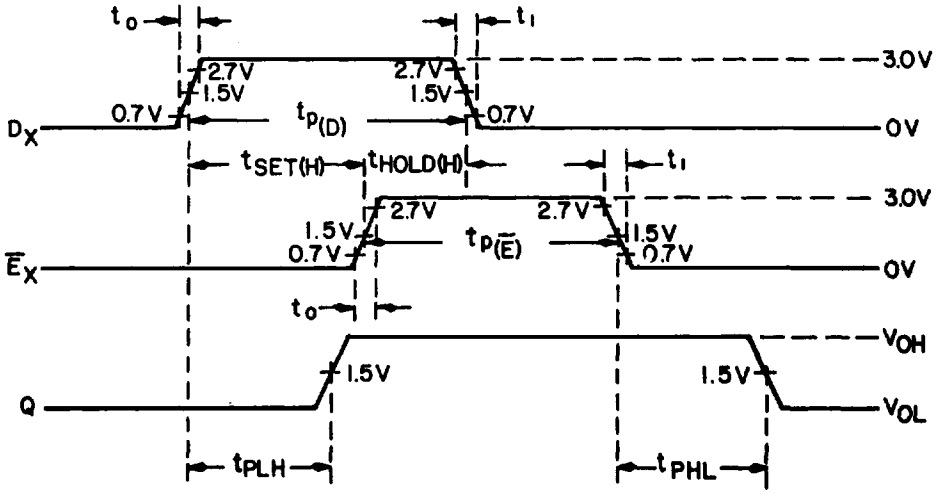


NOTES:

1. D input pulse generator has the following characteristics: V_{gen} = 3 V, minimum, $t_0 = t_1 \leq 10$ ns, and PRR = 500 kHz at 50% duty cycle. For subgroups 7 and 8, PRR $\leq$ 25 kHz at 50% duty cycle and PRR (D input) = 1/2 PRR (clock).
2. Clock input pulse generator has the following characteristics: V_{gen} = 3 V, minimum, $t_0 = t_1 \leq 10$ ns, $t_{p(clock)}$ = 35 ns, $t_{(HOLD)}$ = 35 ns and PRR = 1 MHz. For subgroups 7 and 8, PRR $\leq$ 50 kHz.
3. Each latch is tested separately.
4. C_L = 50 pF, which includes probe and jig capacitance.
5. R_L = 390 Ω ±5%.
6. The $\overline{Q}$ waveforms are not applicable to device type 02.
7. All diodes are 1N3064 or equivalent.

FIGURE 6. Switching test circuit and waveforms for device types 01 and 02.



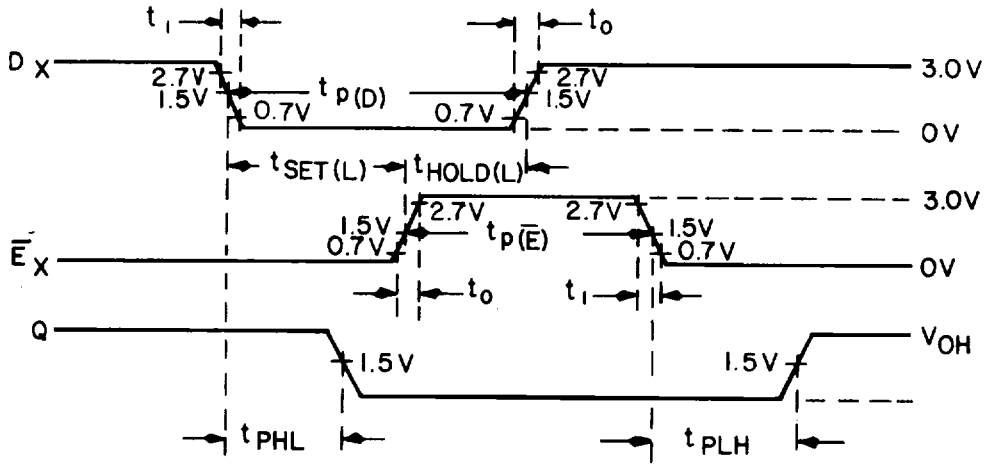


WAVEFORM A

NOTES:

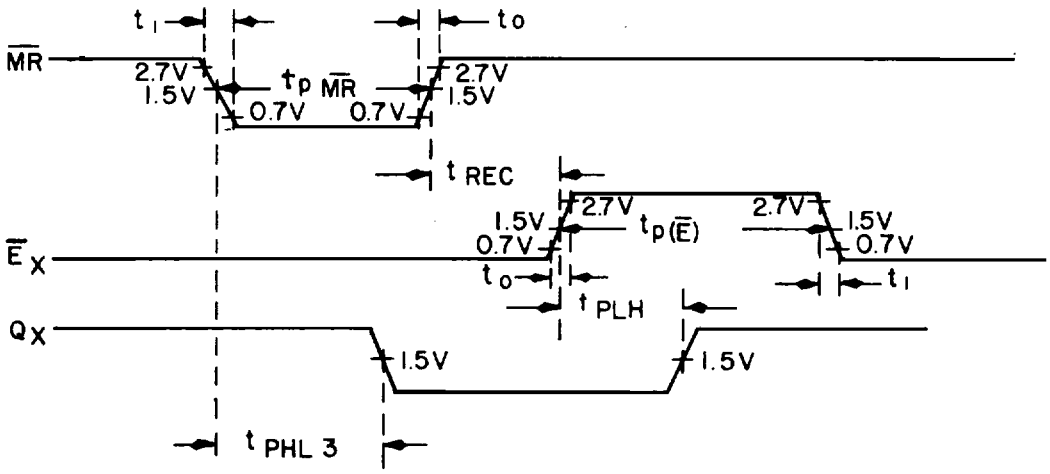
1. The data inputs have the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 10$ ns, $t_{p(D)}$ = 10 ns, and PRR = 1 MHz.
2. The enable inputs have the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq$ 10 ns, $t_{SET(H)}$ = 10 ns, $t_{HOLD(H)}$ = 0 ns, $t_{p(E)}$ = 20 ns, PRR = 1 MHz and $Z_{out} \approx 50\ \Omega$.
3. Each latch is tested separately.
4. C_L = 50 pF, which includes probe and jig capacitance.
5. R_L = 390 Ω ±5%.
6. All diodes are 1N3064 or equivalent.

FIGURE 7. Switching time test circuit and waveforms for device type 03.



WAVEFORM B

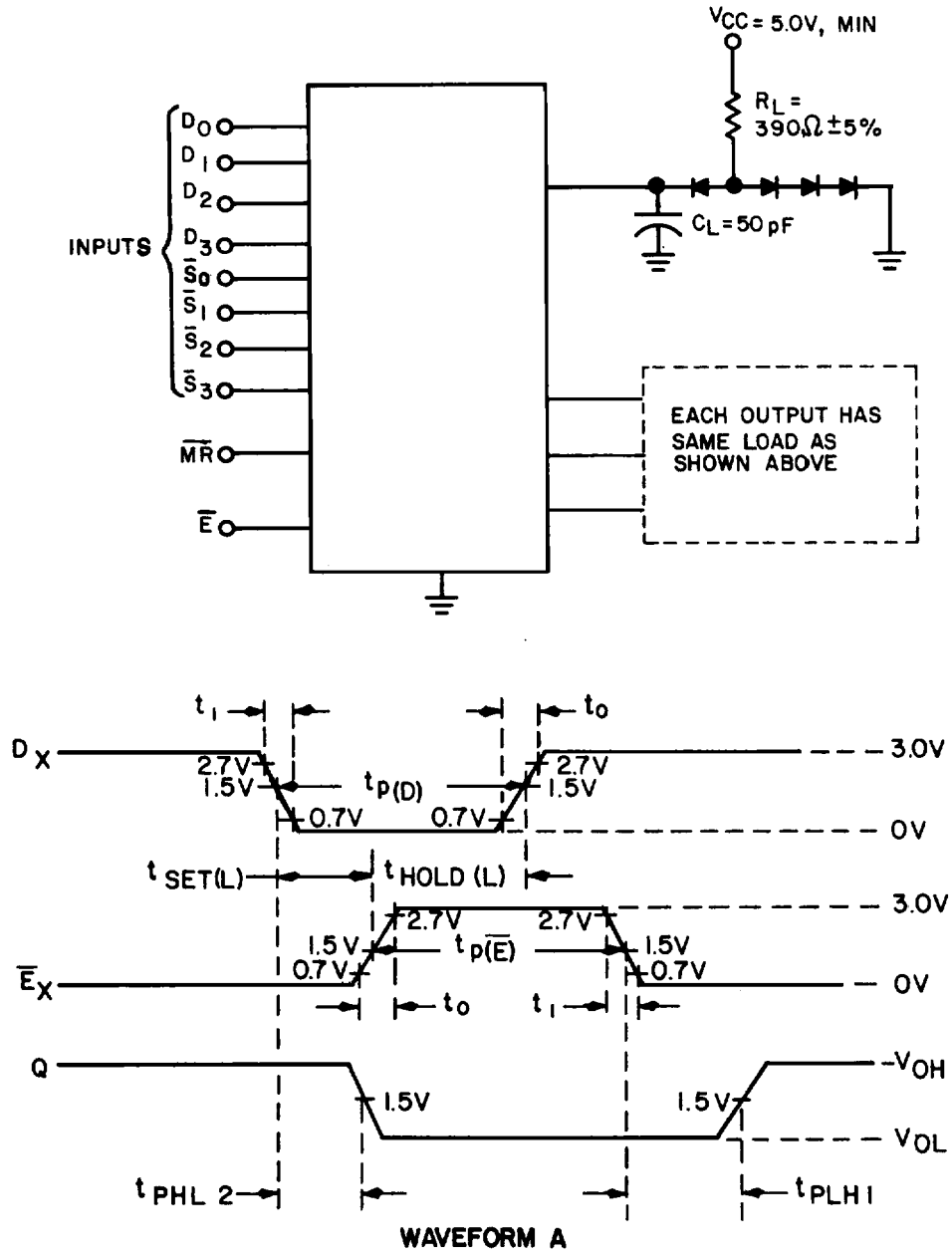
NOTES:
1. The data inputs have the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 10$ ns, $t_{p(D)}$ = 26 ns, and PRR = 1 MHz.
2. The enable inputs have the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 10$ ns, $t_{SET(L)}$ = 16, $t_{HOLD(L)}$ = 10, $t_{p(\overline{E})}$ = 20 ns, PRR = 1 MHz and $Z_{out} \approx 50\ \Omega$.



WAVEFORM C

NOTES:
1. The master reset inputs have the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 10$ ns, $t_{p(\overline{MR})}$ = 20 ns and PRR = 1 MHz.
2. The enable inputs have the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq = 10$ ns, t_{REC} = 10 ns, $t_{p(\overline{E})}$ = 20 ns, PRR = 1 MHz and $Z_{out} \approx 50\ \Omega$.

FIGURE 7. Switching time test circuit and waveforms for device type 03 - Continued.

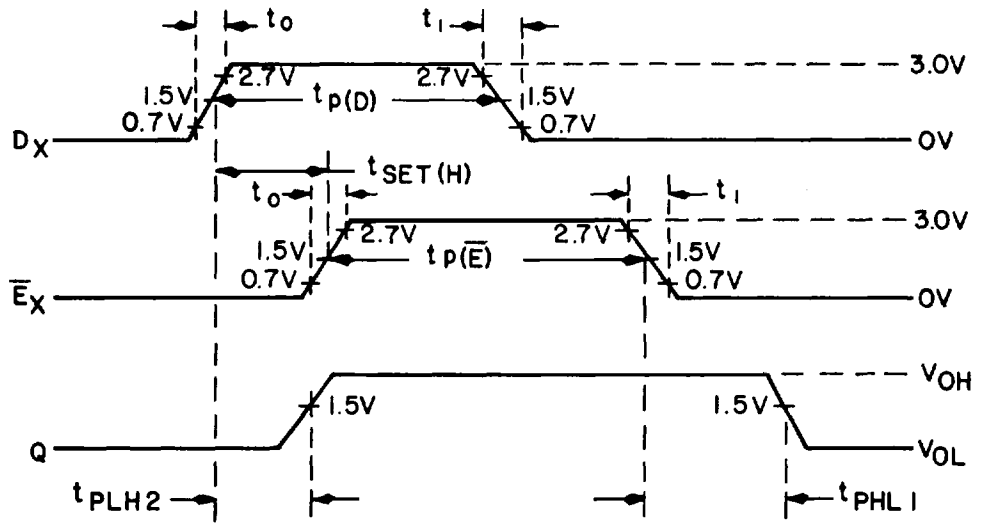


WAVEFORM A

NOTES:

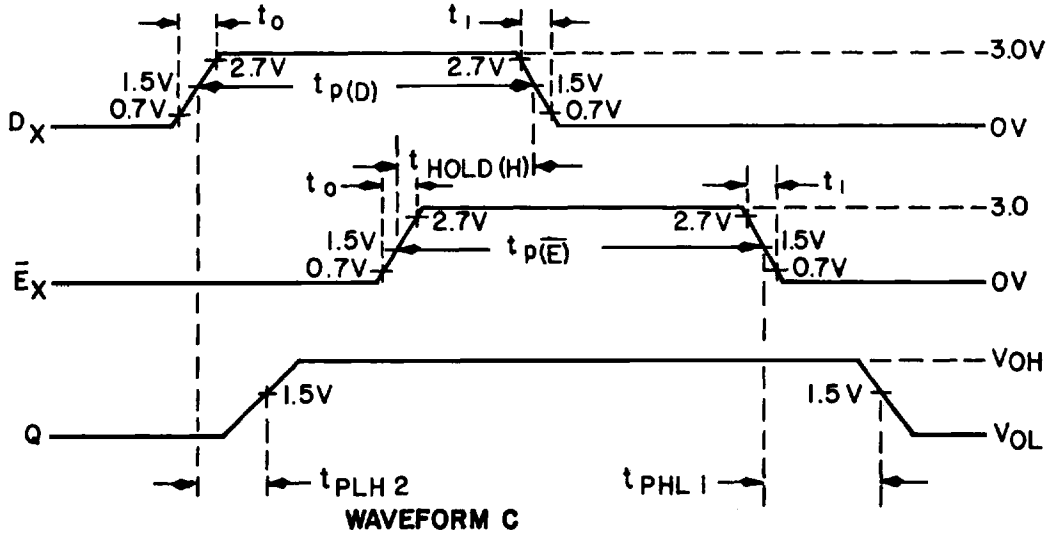
1. The data inputs have the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 10$ ns, $t_{p(D)}$ = 32 ns, and PRR = 1 MHz.
2. The enable input has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 10$ ns $t_{p(E)}$ = 20 ns, $t_{set(L)}$ = 25 ns, $t_{HOLD(L)}$ = 7 ns, PRR = 1 MHz and $Z_{out} \approx 50\ \Omega$.
3. Each latch is tested separately.
4. C_L = 50 pF, which includes probe and jig capacitance.
5. R_L = 390 Ω ± 5%.
6. All diodes are 1N3064 or equivalent.

FIGURE 8. Switching time test circuit and waveforms for device type 04.



WAVEFORM B

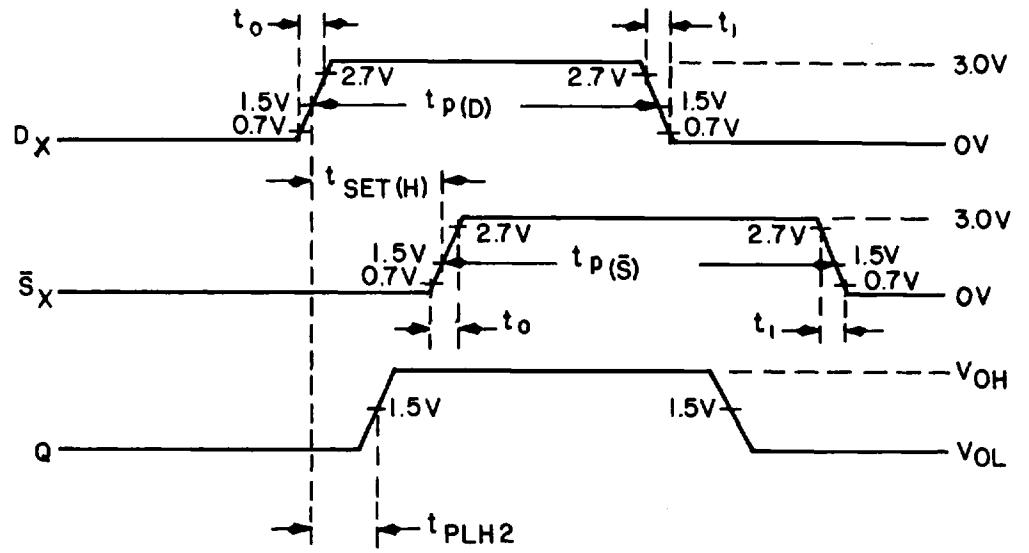
NOTES:
1. The data inputs have the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 10$ ns, $t_{p(D)}$ = 20 ns and PRR = 1 MHz.
2. The enable input has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 10$ ns, $t_{p(\overline{E})}$ = 20 ns, $t_{SET(H)}$ = 5 ns, PRR = 1 MHz and $Z_{out} \approx 50\ \Omega$.



WAVEFORM C

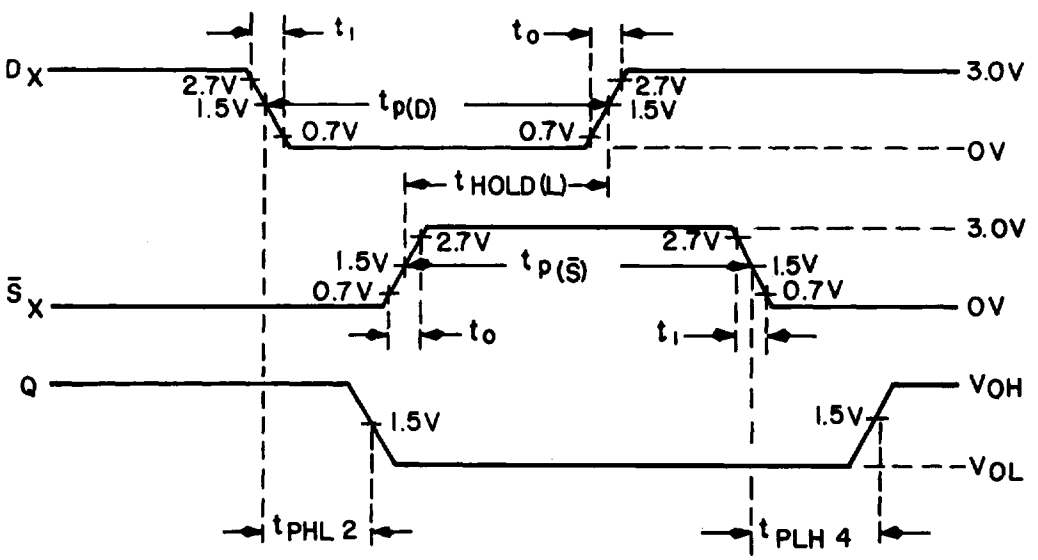
NOTES:
1. The data inputs have the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 10$ ns, $t_{p(D)}$ = 20 ns and PRR = 1 MHz.
2. The enable input has the following characteristics: Vgen = 3 V, t0 = $t_1 \leq 10$ ns, $t_{p(\overline{E})}$ = 20 ns, $t_{HOLD(H)}$ = 0 ns, PRR = 1 MHz and $Z_{out} \approx 50\ \Omega$.

FIGURE 8. Switching time test circuit and waveforms for device type 04 - Continued.



WAVEFORM D

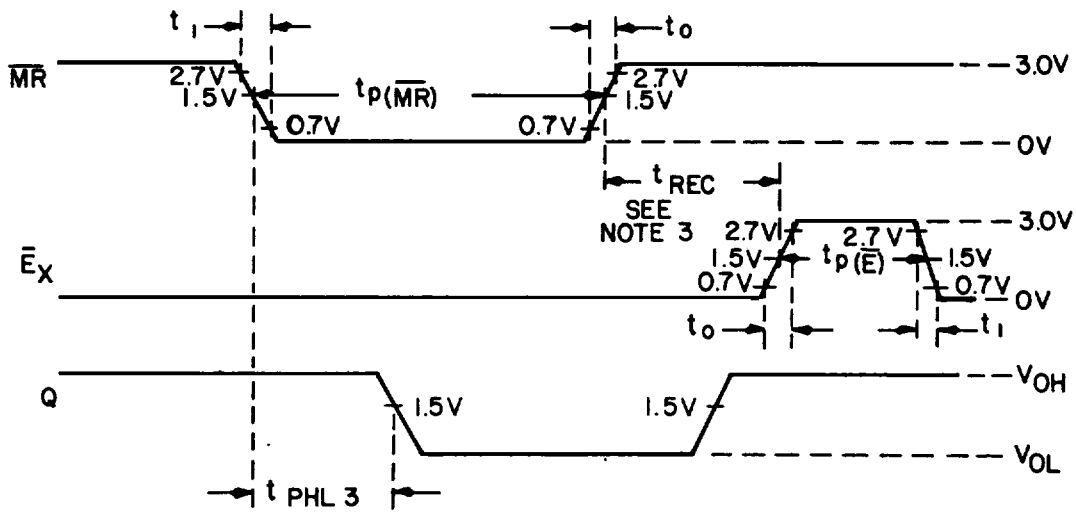
NOTES:
1. The data inputs have the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 10$ ns, $t_{p(D)}$ = 20 ns, and PRR = 1 MHz.
2. The set inputs have the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 10$ ns, $t_{p(\overline{S})}$ = 20 ns, $t_{SET(H)}$ = 8 ns, PRR = 1 MHz and $Z_{out} \approx 50\ \Omega$.



WAVEFORM E

NOTES:
1. The data inputs have the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 10$ ns, $t_{p(D)}$ = 20 ns, and PRR = 1 MHz.
2. The set inputs have the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 10$ ns, $t_{p(\overline{S})}$ = 20 ns, $t_{HOLD(L)}$ = 8 ns, PRR = 1 MHz and $Z_{out} \approx 50\ \Omega$.

FIGURE 8. Switching time test circuit and waveform for device type 04 - Continued.



WAVEFORM F

NOTES:

1. The master reset input has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 10$ ns, $t_{p(\overline{MR})}$ = 18 ns, and PRR 1 MHz.
2. The enable input has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 10$ ns, $t_{p(\overline{E})}$ 20 ns, t_{REC} = 0 ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
3. Recovery time is the minimum time that enable must remain low after the master reset transition from low to high in order for the latch to recognize and store high data.

FIGURE 8. Switching time test circuit and waveforms for device type 04 - Continued.

TABLE III. Group A inspection for device type 01.
Terminal conditions (pins not designated may be $H \geq 2.0$ V, or $L \leq 0.8$ V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case E & F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	$1\overline{Q}$	1D	2D	Clock 3-4	V_{CC}	3D	4D	$4\overline{Q}$	4Q	3Q	$3\overline{Q}$	GND	Clock 1-2	$2\overline{Q}$	2Q	1Q		Min	Max	Unit
1 T_A = 25°C	V_{OH}	3006	1	-0.4mA	0.8 v			4.5 v							GND	2.0 v				$1\overline{Q}$	2.4		Vdc
			2		2.0 v														0.4 mA	1Q			
			3			0.8 v											-0.4 mA			$2\overline{Q}$			
			4			2.0 v												-0.4mA		2Q			
			5				2.0 v		0.8 v					-0.4 mA						$3\overline{Q}$			
			6						2.0 v				-0.4 mA							3Q			
			7							0.8 v	-0.4 mA									$4\overline{Q}$			
			8							2.0 v		-0.4mA								4Q			
	V_{OL}	3007	9	16mA	2.0 v											2.0 v				$1\overline{Q}$		0.4	
			10		0.8 v														16 mA	1Q			
			11			2.0 v											16 mA			$2\overline{Q}$			
			12			0.8 v												16 mA		2Q			
			13				2.0 v		2.0 v					16 mA						$3\overline{Q}$			
			14						0.8 v				16 mA							3Q			
			15							2.0 v	16 mA									$4\overline{Q}$			
			16							0.8 v		16 mA								4Q			
	I_{IL1}	3009	17		0.4 v			5.5 v								4.5 v				1D	-1.4	-3.2	mA
			18			0.4 v										4.5 v				2D			
			19				4.5 v		0.4 v											3D			
			20				4.5 v			0.4 v										4D			
	I_{IL2}		21		0.8 v	0.8 v										0.4 v				CL 1-2	-2.8	-6.4	
	I_{IL2}		22				0.4 v		0.8 v	0.8 v										CL 3-4	-2.8	-6.4	
	I_{IH1}	3010	23		2.4 v											GND				1D		80	μA
			24			2.4 v										GND				2D			
			25				GND		2.4 v											3D			
			26				GND			2.4 v										4D			
	I_{IH2}		27		5.5 v											GND				1D		200	
			28			5.5 v										GND				2D			
			29				GND		5.5 v											3D			
			30				GND			5.5 v										4D			
	I_{IH3}		31		GND	GND										2.4 v				CL 1-2		160	
	I_{IH3}		32				2.4 v		GND	GND										CL 3-4		160	
	I_{IH4}		33		GND	GND										5.5 v				CL 1-2		400	
	I_{IH4}		34				5.5 v		GND	GND										CL 3-4		400	
	I_{OS}	3011	35	GND	GND			5.5 v								4.5 v			GND	$1\overline{Q}$	-20	-57	mA
			36		4.5 v												GND			1Q			
			37			GND														$2\overline{Q}$			
			38			4.5 v												GND		2Q			
			39				4.5 v		GND					GND						$3\overline{Q}$			
			40						4.5 v				GND							3Q			
			41							GND	GND									$4\overline{Q}$			
			42							4.5 v		GND								4Q			
	I_{CC}	3005	43		GND	GND	GND		GND	GND						GND				V_{CC}		46	

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case E & F Test No.	1 1Q̄	2 1D	3 2D	4 Clock 3-4	5 V_{CC}	6 3D	7 4D	8 4Q̄	9 4Q	10 3Q	11 3Q̄	12 GND	13 Clock 1-2	14 2Q̄	15 2Q	16 1Q	Meas. terminal	Test limits Min	Test limits Max	Test limits Unit
1 T_A = 25°C	V_{IC}		44 45 46 47 48 49		-12 mA	-12 mA	-12 mA	4.5 v	-12 mA	-12 mA					GND	-12 mA				1D CL 1-2 2D 3D CL 3-4 4D		-1.5	V
2	Same tests, terminal conditions and limits as for subgroup 1, except T_A = 125° C and V_{IC} tests are omitted.																						
3	Same tests, terminal conditions and limits as for subgroup 1, except T_A = -55° C and V_{IC} tests are omitted.																						
7 1/ T_A = 25°C	Truth table test	3014	50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65	L H L H	B B A A A A B B B A A A A B B B	B B A A A A B B B B A A A B B A	B A A B B A A B B B B A B B B A	5.0 v	B B A A A B B B B A A B A A B B	B B A A A B B B B A A B A A B B	L H L H	H L H L	H L L H	L H H L	GND	B A A B B A A B B B B A B B B A A	L H L H	H L H L	H L H L		See note 2		
8 1/ 3/	Same tests, terminal conditions and limits as for subgroup 7, except T_A = 125° C and -55° C.																						
9 T_A = 25°C	t_{PLH1}	3003 (Fig 5)	66 67 68 69		IN-W	IN-W	A A	5.0 v	IN-W	IN-W		OUT	OUT		GND	A A		OUT	OUT	1D-1Q 2D-2Q 3D-3Q 4D-4Q	2	34	ns
	t_{PLH2}		70 71 72 73	OUT	IN-X	IN-X	A A		IN-X	IN-X	OUT			OUT		A A	OUT			1D-1Q̄ 2D-2Q̄ 3D-3Q̄ 4D-4Q̄		44	
	t_{PLH3}	3003 (Fig 6)	74 75 76 77		IN	IN	IN IN		IN	IN		OUT	OUT			IN IN		OUT	OUT	CL (1-2) -1Q CL (1-2) -2Q CL (3-4) -3Q CL (3-4) -4Q		34	
	t_{PLH4}		78 79 80 81	OUT	IN	IN	IN IN		IN	IN	OUT			OUT		IN IN	OUT			CL (1-2) -1Q̄ CL (1-2) -2Q̄ CL (3-4) -3Q̄ CL (3-4) -4Q̄			
	t_{PHL1}	3003 (Fig 5)	82 83 84 85		IN-X	IN-X	A A		IN-X	IN-X		OUT	OUT			A A		OUT	OUT	1D-1Q 2D-2Q 3D-3Q 4D-4Q		29	
	t_{PHL2}		86 87 88 89	OUT	IN-W	IN-W	A A		IN-W	IN-W	OUT			OUT		A A	OUT			1D-1Q̄ 2D-2Q̄ 3D-3Q̄ 4D-4Q̄		19	

See notes at end of device type 01.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case E & F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	$1\overline{Q}$	1D	2D	Clock 3-4	V_{cc}	3D	4D	$4\overline{Q}$	4Q	3Q	$3\overline{Q}$	GND	Clock 1-2	$2\overline{Q}$	2Q	1Q		Min	Max	Unit
9 T_A = 25°C	t_{PHL3}	3003 (Fig 6)	90		IN			5.0 v							GND	IN			OUT	CL (1-2) -1Q	2	19	ns
			91			IN										IN		OUT		CL (1-2) -2Q			
			92				IN		IN				OUT							CL (3-4) -3Q			
			93				IN			IN		OUT								CL (3-4) -4Q			
	t_{PHL4}		94	OUT	IN											IN				CL (1-2) -1Q			
			95			IN										IN	OUT			CL (1-2) -2Q			
			96				IN		IN					OUT						CL (3-4) -3Q			
			97				IN			IN	OUT									CL (3-4) -4Q			
10 T_A = 125° C	t_{PLH1}	3003 (Fig 5)	98		IN-W											A			OUT	1D-1Q		44	
			99			IN-W										A		OUT		2D-2Q			
			100				A		IN-W				OUT							3D-3Q			
			101				A			IN-W		OUT								4D-4Q			
	t_{PLH2}		102	OUT	IN-X											A				1D-1Q		55	
			103			IN-X										A	OUT			2D-2Q			
			104				A		IN-X					OUT						3D-3Q			
			105				A			IN-X	OUT									4D-4Q			
	t_{PLH3}	3003 (Fig 6)	106		IN											IN			OUT	CL (1-2) -1Q		44	
			107			IN										IN		OUT		CL (1-2) -2Q			
			108				IN		IN				OUT							CL (3-4) -3Q			
			109				IN			IN		OUT								CL (3-4) -4Q			
	t_{PLH4}		110	OUT	IN											IN				CL (1-2) -1Q			
			111			IN										IN	OUT			CL (1-2) -2Q			
			112				IN		IN					OUT						CL (3-4) -3Q			
			113				IN			IN	OUT									CL (3-4) -4Q			
	t_{PHL1}	3003 (Fig 5)	114		IN-X											A			OUT	1D-1Q		38	
			115			IN-X										A		OUT		2D-2Q			
			116				A		IN-X				OUT							3D-3Q			
			117				A			IN-X		OUT								4D-4Q			
	t_{PHL2}		118	OUT	IN-W											A				1D-1Q		25	
			119			IN-W										A	OUT			2D-2Q			
			120				A		IN-W					OUT						3D-3Q			
			121				A			IN-W	OUT									4D-4Q			

See notes at end of device type 01.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case E & F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	$1\overline{Q}$	1D	2D	Clock 3-4	V_{cc}	3D	4D	$4\overline{Q}$	4Q	3Q	$3\overline{Q}$	GND	Clock 1-2	$2\overline{Q}$	2Q	1Q		Min	Max	Unit
10 T_A = 125° C	t_{PHL3}	3003 (Fig 6)	122		IN			5.0 v							GND	IN			OUT	CL (1-2) -1Q	2	25	ns
			123			IN										IN		OUT		CL (1-2) -2Q			
			124				IN		IN				OUT							CL (3-4) -3Q			
			125				IN			IN		OUT								CL (3-4) -4Q			
	t_{PHL4}		126	OUT	IN											IN				CL (1-2) -1$\overline{Q}$			
			127			IN										IN	OUT			CL (1-2) -2$\overline{Q}$			
			128				IN		IN					OUT						CL (3-4) -3$\overline{Q}$			
			129				IN			IN	OUT									CL (3-4) -4$\overline{Q}$			
11	Same tests, terminal conditions and limits as subgroup 10, except T_A = -55° C.																						

NOTES:
A = Clock pulse A, see figure 5.
W and X = Various D-input pulses, see figure 5.

1/ Only a summary of attributes data is required.
2/ Output voltages shall be either:
(a) H = 2.4 volts minimum and L=0.4 volt maximum when using a high speed checker double comparator, or
(b) H ≥ 1.5 volts and L ≤ 1.5 volts when using a high speed checker single comparator.

TABLE III. Group A inspection for device type 02.
Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case A,B,C,D Test No.	1 1D	2 2D	3 Clock 3-4	4 V_{cc}	5 3D	6 4D	7 NC	8 4Q	9 3Q	10 NC	11 GND	12 Clock 1-2	13 2Q	14 1Q	Meas. terminal	Test limits Min	Max	Unit
1 T_A=25°C	V_{OH}	3006	1	2.0 v	2.0 v		4.5 v							GND	2.0 v		-0.4mA	1Q	2.4		Vdc
			2												2.0 v	-0.4mA		2Q			
			3			2.0 v		2.0 v				-0.4mA						3Q			
			4			2.0 v			2.0 v		-0.4mA							4Q			
	V_{OL}	3007	5	0.8 v	0.8 v										2.0 v		16 mA	1Q		0.4	
			6												2.0 v	16 mA		2Q			
			7			2.0 v		0.8 v				16 mA						3Q			
			8			2.0 v			0.8 v		16 mA							4Q			
	I_{IL1}	3009	9	0.4 v	0.4 v		5.5 v								4.5 v			1D	-1.4	-3.2	mA
			10												4.5 v			2D			
			11			4.5 v		0.4 v										3D			
			12			4.5 v			0.4 v									4D			
	I_{IL2}		13	0.8 v	0.8 v										0.4 v			CL 1-2	-2.8	-6.4	
			14			0.4 v		0.8 v	0.8 v									CL 3-4	-2.8	-6.4	
	I_{IH1}	3010	15	2.4 v	2.4 v										GND			1D		80	µA
			16												GND			2D			
			17			GND		2.4 v										3D			
			18			GND			2.4 v									4D			
	I_{IH2}		19	5.5 v	5.5 v										GND			1D		200	
			20												GND			2D			
			21			GND		5.5 v										3D			
			22			GND			5.5 v									4D			
	I_{IH3}		23	GND	GND										2.4 v			CL 1-2		160	
			24			2.4 v		GND	GND									CL 3-4		160	
	I_{IH4}		25	GND	GND										5.5 v			CL 1-2		400	
			26			5.5 v		GND	GND									CL 3-4		400	
	I_{OS}	3011	27	4.5 v	4.5 v									GND	4.5 v	GND	GND	1Q	-20	-57	mA
			28												4.5 v			2Q			
			29			4.5 v		4.5 v				GND						3Q			
			30			4.5 v			4.5 v		GND							4Q			
	I_{CC}	3005	31	GND	GND	GND		GND	GND						GND			V_{cc}		46	
	V_{IC}		32	-12 mA	-12 mA		4.5 v											1D		-1.5	Vdc
			33															2D			
			34					-12 mA										3D			
			35						-12 mA									4D			
			36												-12 mA			CL 1-2			
			37			-12 mA												CL 3-4			
2	Same tests, terminal conditions and limits as for subgroup 1, except T_A = 125° C and V_{IC} tests are omitted.																				
3	Same tests, terminal conditions and limits as for subgroup 1, except T_A = -55° C and V_{IC} tests are omitted.																				

See notes at end of device type 02.

TABLE III. Group A inspection for device type 02. - Continued
Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Case A,B,C,D Test No.	1 1D	2 2D	3 Clock 3-4	4 V_{CC}	5 3D	6 4D	7 NC	8 4Q	9 3Q	10 NC	11 GND	12 Clock 1-2	13 2Q	14 1Q	Meas. terminal	Test limits Min	Max	Unit
7 1/ T_A = 25°C	VLT-H1	(See fig 5)	38	IN-W			5.0 V							GND	A		OUT	1D -1Q	2.4		V
	VLT-H1		39		IN-W										A	OUT		2D -2Q	2.4		
	VLT-H1		40			A		IN-W				OUT						3D -3Q	2.4		
	VLT-H1		41			A			IN-W		OUT							4D -4Q	2.4		
	VLT-L1		42	IN-X											A		OUT	1D -1Q		0.4	
	VLT-L1		43		IN-X										A	OUT		2D -2Q		0.4	
	VLT-L1		44			A		IN-X				OUT						3D -3Q		0.4	
	VLT-L1		45			A			IN-X		OUT							4D -4Q		0.4	
	VLT-H3	(See fig 6)	46	IN											IN-B		OUT	CL(1-2) -1Q	2.4		
	VLT-H3		47		IN										IN-B	OUT		CL(1-2) -2Q	2.4		
	VLT-H3		48			IN		IN				OUT						CL(3-4) -3Q	2.4		
	VLT-H3		49			IN			IN		OUT							CL(3-4) -4Q	2.4		
	VLT-L3		50	IN											IN-B		OUT	CL(1-2) -1Q		0.4	
	VLT-L3		51		IN										IN-B	OUT		CL(1-2) -3Q		0.4	
	VLT-L3		52			IN		IN				OUT						CL(3-4) -3Q		0.4	
	VLT-L3		53			IN			IN		OUT							CL(3-4) -4Q		0.4	
8 1/	Same tests, terminal conditions and limits as for subgroup 7, except T_A = 125° and -55°C.																				

TABLE III. Group A inspection for device type 02 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case A,B,C,D Test No.	1 1D	2 2D	3 Clock 3-4	4 V_{cc}	5 3D	6 4D	7 NC	8 4Q	9 3Q	10 NC	11 GND	12 Clock 1-2	13 2Q	14 1Q	Meas. terminal	Test limits Min	Max	Unit
9 T_A=25°C	t_{PLH1}	3003 (Fig 5-A)	54	IN-W			5.0 v							GND	A		OUT	1D-1Q	2	34	ns
			55		IN-W										A	OUT		2D-2Q			
			56			A		IN-W				OUT						3D-3Q			
			57			A			IN-W		OUT							4D-4Q		▼	
	t_{PHL1}	3003 (Fig 5-B)	58	IN-X											A		OUT	1D-1Q		29	
			59		IN-X										A	OUT		2D-2Q			
			60			A		IN-X				OUT						3D-3Q			
			61			A			IN-X		OUT							4D-4Q		▼	
	t_{PLH3}	3003 (Fig 6)	62	IN											IN		OUT	CL(1-2) -1Q		34	
			63		IN										IN	OUT		CL(1-2) -2Q			
			64			IN		IN				OUT						CL(3-4) -3Q			
			65			IN			IN		OUT							CL(3-4) -4Q		▼	
	t_{PHL3}		66	IN											IN		OUT	CL(1-2) -1Q		19	
			67		IN										IN	OUT		CL(1-2) -2Q			
			68			IN		IN				OUT						CL(3-4) -3Q			
			69			IN			IN		OUT							CL(3-4) -4Q	▼	▼	▼
10 T_A=125°C	t_{PLH1}	3003 (Fig 5-A)	70	IN-W											A		OUT	1D-1Q	2	44	ns
			71		IN-W										A	OUT		2D-2Q			
			72			A		IN-W				OUT						3D-3Q			
			73			A			IN-W		OUT							4D-4Q		▼	
	t_{PHL1}	3003 (Fig 5-B)	74	IN-X											A		OUT	1D-1Q		38	
			75		IN-X										A	OUT		2D-2Q			
			76			A		IN-X				OUT						3D-3Q			
			77			A			IN-X		OUT							4D-4Q		▼	
	t_{PLH3}	3003 (Fig 6)	78	IN											IN		OUT	CL(1-2) -1Q		44	
			79		IN										IN	OUT		CL(1-2) -2Q			
			80			IN		IN				OUT						CL(3-4) -3Q			
			81			IN			IN		OUT							CL(3-4) -4Q		▼	
	t_{PHL3}		82	IN											IN		OUT	CL(1-2) -1Q		25	
			83		IN										IN	OUT		CL(1-2) -2Q			
			84			IN		IN				OUT						CL(3-4) -3Q			
			85			IN	▼		IN		OUT			▼				CL(3-4) -4Q	▼	▼	▼
11	Same tests, terminal conditions and limits as subgroup 10, except T_A = -55°C.																				

NOTES:
A = Clock pulse A, see figure 5.
W and X = Various D-input pulses, see figure 5.
1/ Latch voltage, V_{LT}, shall be measured no sooner than 10 μs after switching transition occurs.

TABLE III. Group A inspection for device type 03.
Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.5 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case J,K,L,Z	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Meas. terminal	Test limits		
			Test No.	$1\overline{MR}$	$1\overline{E}_0$	$1\overline{E}_1$	$1D_0$	$1Q_0$	$1D_1$	$1Q_1$	$1D_2$	$1Q_2$	$1D_3$	$1Q_3$	GND	$2\overline{MR}$	$2\overline{E}_0$	$2\overline{E}_1$	$2D_0$	$2Q_0$	$2D_1$	$2Q_1$	$2D_2$	$2Q_2$	$2D_3$	$2Q_3$	V_{CC}		Min	Max	Unit
1 T_A=25°C	V_{OH}	3006	1	4.5 v	0.8 v	0.8 v	4.5 v	-0.8mA	4.5 v	-0.8mA	4.5 v	-0.8mA	4.5 v	-0.8mA	GND	4.5 v	0.8 v	0.8 v	4.5 v	-0.8mA	4.5 v	-0.8 mA	4.5 v	-0.8mA	4.5 v	-0.8mA	4.5 v	$1Q_0$	2.4		V
			2																									$1Q_1$			
			3																									$1Q_2$			
			4																									$1Q_3$			
			5																									$2Q_0$			
			6																									$2Q_1$			
			7																									$2Q_2$			
			8																									$2Q_3$			
	V_{OL}	3007	9				0.8 v	16 mA	0.8 v		0.8 v		0.8 v						0.8 v		0.8 v		0.8 v		0.8 v			$1Q_0$		0.4	
			10							16 mA																		$1Q_1$			
			11									16 mA		16 mA														$1Q_2$			
			12																	16 mA								$1Q_3$			
			13																			16 mA						$2Q_0$			
			14																					16 mA				$2Q_1$			
			15																									$2Q_2$			
			16																							16 mA		$2Q_3$			
	V_{IC}		17	-12 mA																								$1\overline{MR}$			
			18		-12 mA																							$1\overline{E}_0$			
			19			-12 mA																						$1\overline{E}_1$			
			20				-12 mA																					$1D_0$			
			21						-12 mA																			$1D_1$			
			22								-12 mA																	$1D_2$			
			23										-12 mA															$1D_3$			
			24													-12 mA												$2\overline{MR}$		-1.5	
			25														-12 mA											$2\overline{E}_0$			
			26															-12 mA										$2\overline{E}_1$			
			27																-12 mA									$2D_0$			
			28																		-12 mA							$2D_1$			
			29																				-12 mA					$2D_2$			
			30																						-12 mA			$2D_3$			
	I_{IL1}	3009	31 CKT A	GND	GND		0.4 v																			5.5 v	$1D_0$	-0.7	-2.4	mA
			31 CKT B				0.4 v																				$1D_0$	-0.7	-1.6	
			31 CKT C				0.4 v																				$1D_0$	-0.5	-1.4	
			32 CKT A						0.4 v																		$1D_1$	-0.7	-2.4	
			32 CKT B						0.4 v																		$1D_1$	-0.7	-1.6	
			32 CKT C						0.4 v																		$1D_1$	-0.5	-1.4	
			33 CKT A								0.4 v																$1D_2$	-0.7	-2.4	
			33CKT B								0.4 v																$1D_2$	-0.7	-1.6	
			33 CKT C								0.4 v																$1D_2$	-0.5	-1.4	
			34 CKT A										0.4 v														$1D_3$	-0.7	-2.4	
			34 CKT B										0.4 v														$1D_3$	-0.7	-1.6	
			34 CKT C										0.4 v														$1D_3$	-0.5	-1.4	
			35 CKT A													GND			0.4 v								$2D_0$	-0.7	-2.4	
			35 CKT B													GND			0.4 v								$2D_0$	-0.7	-1.6	
			35 CKT C													GND			0.4 v								$2D_0$	-0.5	-1.4	
			36 CKT A														GND				0.4 v						$2D_1$	-0.7	-2.4	
			36 CKT B														GND				0.4 v						$2D_1$	-0.7	-1.6	
			36 CKT C														GND				0.4 v						$2D_1$	-0.5	-1.4	
			37 CKT A															GND					0.4 v				$2D_2$	-0.7	-2.4	
			37 CKT B															GND					0.4 v				$2D_2$	-0.7	-1.6	
			37 CKT C															GND					0.4 v				$2D_2$	-0.5	-1.4	
			38 CKT A																GND					0.4 v			$2D_3$	-0.7	-2.4	
			38 CKT B																GND					0.4 v			$2D_3$	-0.7	-1.6	
			38 CKT C																GND					0.4 v			$2D_3$	-0.5	-1.4	

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated may be H $\geq$ 2.0 V, or L $\leq$ 0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Case J,K,L,Z Test No.	1 $1\overline{MR}$	2 $1\overline{E}_0$	3 $1\overline{E}_1$	4 $1D_0$	5 $1Q_0$	6 $1D_1$	7 $1Q_1$	8 $1D_2$	9 $1Q_2$	10 $1D_3$	11 $1Q_3$	12 GND	13 $2\overline{MR}$	14 $2\overline{E}_0$	15 $2\overline{E}_1$	16 $2D_0$	17 $2Q_0$	18 $2D_1$	19 $2Q_1$	20 $2D_2$	21 $2Q_2$	22 $2D_3$	23 $2Q_3$	24 V_{CC}	Meas. terminal	Test limits Min	Max	Unit
1 T_A=25°C	I_{IL2}	3009	39	0.4 V											GND													$1\overline{MR}$	-0.7	-1.6	mA
			40		0.4 V	5.5 V																						$1\overline{E}_0$			
			41		5.5 V	0.4 V										0.4 V												$1\overline{E}_1$			
			42														0.4 V	5.5 V										$2\overline{MR}$			
			43														5.5 V	0.4 V										$2\overline{E}_0$			
			44																									$2\overline{E}_1$			
	I_{IH1}	3010	45 CKT A			5.5 V	2.4 V																					$1D_0$		40	μA
			45 CKT B,C				2.4 V																					$1D_0$		80	
			46 CKT A						2.4 V																			$1D_1$		40	
			46 CKT B,C						2.4 V																			$1D_1$		80	
			47 CKT A								2.4 V																	$1D_2$		40	
			47 CKT B,C								2.4 V																	$1D_2$		80	
			48 CKT A										2.4 V															$1D_3$		40	
			48 CKT B,C			5.5 V							2.4 V															$1D_3$		80	
			49 CKT A															5.5 V	2.4 V									$2D_0$		40	
			49 CKT B,C																2.4 V									$2D_0$		80	
			50 CKT A																		2.4 V							$2D_1$		40	
			50 CKT B,C																		2.4 V							$2D_1$		80	
			51 CKT A																				2.4 V					$2D_2$		40	
			51 CKT B,C																				2.4 V					$2D_2$		80	
			52 CKT A																						2.4 V			$2D_3$		40	
			52 CKT B,C																						2.4 V			$2D_3$		80	
	I_{IH2}	3010	53 CKT A			5.5 V	5.5 V																					$1D_0$		100	
			53 CKT B,C				5.5 V																					$1D_0$		200	
			54 CKT A						5.5 V																			$1D_1$		100	
			54 CKT B,C						5.5 V																			$1D_1$		200	
			55 CKT A								5.5 V																	$1D_2$		100	
			55 CKT B,C								5.5 V																	$1D_2$		200	
			56 CKT A										5.5 V															$1D_3$		100	
			56 CKT B,C			5.5 V							5.5 V															$1D_3$		200	
			57 CKT A															5.5 V	5.5 V									$2D_0$		100	
			57 CKT B,C																5.5 V									$2D_0$		200	
			58 CKT A																		5.5 V							$2D_1$		100	
			58 CKT B,C																		5.5 V							$2D_1$		200	
			59 CKT A																				5.5 V					$2D_2$		100	
			59 CKT B,C																				5.5 V					$2D_2$		200	
			60 CKT A																						5.5 V			$2D_3$		100	
			60 CKT B,C																						5.5 V			$2D_3$		200	
	I_{IH3}	3010	61	2.4 V																								$1\overline{MR}$		40	
			62		2.4 V	GND																						$1\overline{E}_0$			
			63		GND	2.4 V										2.4 V												$1\overline{E}_1$			
			64														2.4 V	GND										$2\overline{MR}$			
			65														GND	2.4 V										$2\overline{E}_0$			
			66																									$2\overline{E}_1$			

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated may be H $\geq$ 2.0 V, or L $\leq$ 0.8 V, or open).

Subgroup	Symbol	MIL-STD-883 method	Case J,K,L,Z Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Meas. terminal	Test limits Min	Max	Unit
				$1\overline{MR}$	$1\overline{E}_0$	$1\overline{E}_1$	$1D_0$	$1Q_0$	$1D_1$	$1Q_1$	$1D_2$	$1Q_2$	$1D_3$	$1Q_3$	GND	$2\overline{MR}$	$2\overline{E}_0$	$2\overline{E}_1$	$2D_0$	$2Q_0$	$2D_1$	$2Q_1$	$2D_2$	$2Q_2$	$2D_3$	$2Q_3$	V_{CC}				
1 T_A =25°C	I_{IH4}	3010	67	5.5 V											GND											5.5 V	$1\overline{MR}$		100	µA
			68		5.5 V	GND																					$1\overline{E}_0$			
			69													5.5 V											$1\overline{E}_1$			
			70														5.5 V	GND									$2\overline{MR}$			
			71														GND	5.5 V									$2\overline{E}_0$			
			72																								$2\overline{E}_1$			
	I_{OS}	3011	73	4.5 V	GND	GND	4.5 V	GND	4.5 V	GND	4.5 V	GND	4.5 V	GND		4.5 V	GND	GND	4.5 V	GND	4.5 V	GND	4.5 V	GND	4.5 V	GND		$1Q_0$	-10	-70	mA
			74																								$1Q_1$	1/		
			75																								$1Q_2$			
			76																								$1Q_3$			
			77																								$2Q_0$			
			78																								$2Q_1$			
			79																								$2Q_2$			
			80																								$2Q_3$			
	I_{CC}	3005	81	4.5 V	4.5 V	4.5 V	4.5 V		4.5 V		4.5 V		4.5 V			4.5 V	4.5 V	4.5 V	4.5 V		4.5 V		4.5 V		4.5 V		V_{CC}		108	mA
2	Same tests, terminal conditions and limits as for subgroup 1, except T_A = 125°C and V_{IC} tests are omitted.																														
3	Same tests, terminal conditions and limits as for subgroup 1, except T_A = -55°C and V_{IC} tests are omitted.																														

1/ Circuit B and C limits for I_{OS} shall be -20, minimum and -57, maximum.

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case J,K, L,Z	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Meas. terminal	Test Limits		
			Test No.	$1\overline{MR}$	$1\overline{E}_0$	$1\overline{E}_1$	$1D_0$	$1Q_0$	$1D_1$	$1Q_1$	$1D_2$	$1Q_2$	$1D_3$	$1Q_3$	GND	$2\overline{MR}$	$2\overline{E}_0$	$2\overline{E}_1$	$2D_0$	$2Q_0$	$2D_1$	$2Q_1$	$2D_2$	$2Q_2$	$2D_3$	$2Q_3$	V_{CC}		Min	Max	Unit
9 T_A=25°C	t_{PLH1}	3003 (Fig 7-B)	82	5.0 v	IN	GND	IN	OUT	IN	OUT	IN	OUT	IN	OUT	GND	5.0 v	IN	GND	IN	OUT	IN	OUT	IN	OUT	IN	OUT	5.0 v	$1\overline{E}_0$-$1Q_0$	3	33	ns
			83																									$1E_1$-$1Q_1$			
			84																									$1\overline{E}_2$-$1Q_2$			
			85																									$1E_3$-$1Q_3$			
			86		GND	IN	IN	OUT	IN	OUT																		$1\overline{E}_0$-$1Q_0$			
			87								IN	OUT	IN	OUT														$1E_1$-$1Q_1$			
			88																									$1E_2$-$1Q_2$			
			89																									$1E_3$-$1Q_3$			
			90														IN	GND	IN	OUT								$2\overline{E}_0$-$2Q_0$			
			91																		IN	OUT						$2E_1$-$2Q_1$			
			92																				IN	OUT				$2\overline{E}_2$-$2Q_2$			
			93																						IN	OUT		$2E_3$-$2Q_3$			
			94														GND	IN	IN	OUT								$2\overline{E}_0$-$2Q_0$			
			95																		IN	OUT						$2E_1$-$2Q_1$			
			96																				IN	OUT				$2\overline{E}_2$-$2Q_2$			
			97																						IN	OUT		$2E_3$-$2Q_3$			
	t_{PHL1}	3003 (Fig 7-A)	98		IN	GND	IN	OUT	IN	OUT	IN	OUT	IN	OUT														$1\overline{E}_0$-$1Q_0$		25	
			99																									$1E_1$-$1Q_1$			
			100																									$1\overline{E}_2$-$1Q_2$			
			101																									$1E_3$-$1Q_3$			
			102		GND	IN	IN	OUT	IN	OUT																		$1\overline{E}_0$-$1Q_0$			
			103								IN	OUT	IN	OUT														$1E_1$-$1Q_1$			
			104																									$1E_2$-$1Q_2$			
			105																									$1E_3$-$1Q_3$			
			106														IN	GND	IN	OUT								$2\overline{E}_0$-$2Q_0$			
			107																		IN	OUT						$2E_1$-$2Q_1$			
			108																				IN	OUT				$2\overline{E}_2$-$2Q_2$			
			109																						IN	OUT		$2E_3$-$2Q_3$			
			110														GND	IN	IN	OUT								$2\overline{E}_0$-$2Q_0$			
			111																		IN	OUT						$2E_1$-$2Q_1$			
			112																				IN	OUT				$2\overline{E}_2$-$2Q_2$			
			113																						IN	OUT		$2E_3$-$2Q_3$			
	t_{PLH2}	3003 (Fig 7)	114		IN	GND	IN	OUT	IN	OUT	IN	OUT	IN	OUT														$1D_0$-$1Q_0$		33	
			115																									$1D_1$-$1Q_1$			
			116																									$1D_2$-$1Q_2$			
			117																									$1D_3$-$1Q_3$			
			118		GND	IN	IN	OUT	IN	OUT																		$1D_0$-$1Q_0$			
			119								IN	OUT	IN	OUT														$1D_1$-$1Q_1$			
			120																									$1D_2$-$1Q_2$			
			121																									$1D_3$-$1Q_3$			
			122														IN	GND	IN	OUT								$2D_0$-$2Q_0$			
			123																		IN	OUT						$2D_1$-$2Q_1$			
			124																				IN	OUT				$2D_2$-$2Q_2$			
			125																						IN	OUT		$2D_3$-$2Q_3$			
			126														GND	IN	IN	OUT								$2D_0$-$2Q_0$			
			127																		IN	OUT						$2D_1$-$2Q_1$			
			128																				IN	OUT				$2D_2$-$2Q_2$			
			129																						IN	OUT		$2D_3$-$2Q_3$			

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case J,K, L,Z	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24		Test limits		
			Test No.	$1\overline{MR}$	$1\overline{E}_0$	$1\overline{E}_1$	$1D_0$	$1Q_0$	$1D_1$	$1Q_1$	$1D_2$	$1Q_2$	$1D_3$	$1Q_3$	GND	$2\overline{MR}$	$2\overline{E}_0$	$2\overline{E}_1$	$2D_0$	$2Q_0$	$2D_1$	$2Q_1$	$2D_2$	$2Q_2$	$2D_3$	$2Q_3$	V_{CC}	Meas. terminal	Min	Max	Unit
9 T_A=25°C	t_{PHL2}	3003 (Fig 7)	130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145	5.0 v	IN GND	GND IN	IN IN	OUT OUT	IN IN	OUT OUT	IN IN	OUT OUT	IN IN	OUT OUT	GND	5.0 v	IN GND	GND IN	IN IN	OUT OUT	IN IN	OUT OUT	IN IN	OUT OUT	IN IN	OUT OUT	5.0 v	$1D_0$-$1Q_0$ $1D_1$-$1Q_1$ $1D_2$-$1Q_2$ $1D_3$-$1Q_3$ $1D_0$-$1Q_0$ $1D_1$-$1Q_1$ $1D_2$-$1Q_2$ $1D_3$-$1Q_3$ $2D_0$-$2Q_0$ $2D_1$-$2Q_1$ $2D_2$-$2Q_2$ $2D_3$-$2Q_3$ $2D_0$-$2Q_0$ $2D_1$-$2Q_1$ $2D_2$-$2Q_2$ $2D_3$-$2Q_3$	3	28	ns
	t_{PHL3}	3003 (Fig 7-C)	146 147 148 149 150 151 152 153 154 155 156 157 158 159 160 161	IN	IN GND	GND IN	5.0 v	OUT OUT	5.0 v	OUT OUT	5.0 v	OUT OUT	5.0 v	OUT OUT		IN	IN GND	GND IN	5.0 v	OUT OUT	5.0 v	OUT OUT	5.0 v	OUT OUT	5.0 v	OUT OUT		$1\overline{MR}$-$1Q_0$ $1\overline{MR}$-$1Q_1$ $1\overline{MR}$-$1Q_2$ $1\overline{MR}$-$1Q_3$ $1\overline{MR}$-$1Q_0$ $1\overline{MR}$-$1Q_1$ $1\overline{MR}$-$1Q_2$ $1\overline{MR}$-$1Q_3$ $2\overline{MR}$-$2Q_0$ $2\overline{MR}$-$2Q_1$ $2\overline{MR}$-$2Q_2$ $2\overline{MR}$-$2Q_3$ $2\overline{MR}$-$2Q_0$ $2\overline{MR}$-$2Q_1$ $2\overline{MR}$-$2Q_2$ $2\overline{MR}$-$2Q_3$		25	
10 T_A=125°C	t_{PLH1}	3003 (Fig 7-B)	162 163 164 165 166 167 168 169 170 171 172 173 174 175 176 177	5.0 v	IN GND	GND IN	IN IN	OUT OUT	IN IN	OUT OUT	IN IN	OUT OUT	IN IN	OUT OUT		5.0 v	IN GND	GND IN	IN IN	OUT OUT	IN IN	OUT OUT	IN IN	OUT OUT	IN IN	OUT OUT		$1\overline{E}_0$-$1Q_0$ $1\overline{E}_1$-$1Q_1$ $1\overline{E}_2$-$1Q_2$ $1\overline{E}_3$-$1Q_3$ $1\overline{E}_0$-$1Q_0$ $1\overline{E}_1$-$1Q_1$ $1\overline{E}_2$-$1Q_2$ $1\overline{E}_3$-$1Q_3$ $2\overline{E}_0$-$2Q_0$ $2\overline{E}_1$-$2Q_1$ $2\overline{E}_2$-$2Q_2$ $2\overline{E}_3$-$2Q_3$ $2\overline{E}_0$-$2Q_0$ $2\overline{E}_1$-$2Q_1$ $2\overline{E}_2$-$2Q_2$ $2\overline{E}_3$-$2Q_3$		60	

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case J,K, L,Z	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Meas. terminal	Test limits		
			Test No.	$1\overline{MR}$	$1\bar{E}_0$	$1\bar{E}_1$	$1D_0$	$1Q_0$	$1D_1$	$1Q_1$	$1D_2$	$1Q_2$	$1D_3$	$1Q_3$	GND	$2\overline{MR}$	$2\bar{E}_0$	$2\bar{E}_1$	$2D_0$	$2Q_0$	$2D_1$	$2Q_1$	$2D_2$	$2Q_2$	$2D_3$	$2Q_3$	V_{cc}		Min	Max	Unit
10 T_A=125°C	t_{PHL1}	3003 (Fig 7-A)	178 179 180 181 182 183 184 185 186 187 188 189 190 191 192 193	5.0 v	IN GND	GND IN	IN IN	OUT OUT	IN IN	OUT OUT	IN IN	OUT OUT	IN IN	OUT OUT	GND	5.0 v	IN GND	GND IN	IN IN	OUT OUT	IN IN	OUT OUT	IN IN	OUT OUT	IN IN	OUT OUT	5.0 v	$1\bar{E}_0$-$1Q_0$ $1\bar{E}_1$-$1Q_1$ $1\bar{E}_2$-$1Q_2$ $1\bar{E}_3$-$1Q_3$ $1\bar{E}_0$-$1Q_0$ $1\bar{E}_1$-$1Q_1$ $1\bar{E}_2$-$1Q_2$ $1\bar{E}_3$-$1Q_3$ $2\bar{E}_0$-$2Q_0$ $2\bar{E}_1$-$2Q_1$ $2\bar{E}_2$-$2Q_2$ $2\bar{E}_3$-$2Q_3$ $2\bar{E}_0$-$2Q_0$ $2\bar{E}_1$-$2Q_1$ $2\bar{E}_2$-$2Q_2$ $2\bar{E}_3$-$2Q_3$	3	40	ns
	t_{PLH2}	3003 (Fig 7)	194 195 196 197 198 199 200 201 202 203 204 205 206 207 208 209		IN GND	GND IN	IN IN	OUT OUT	IN IN	OUT OUT	IN IN	OUT OUT	IN IN	OUT OUT			IN GND	GND IN	IN IN	OUT OUT	IN IN	OUT OUT	IN IN	OUT OUT	IN IN	OUT OUT		$1D_0$-$1Q_0$ $1D_1$-$1Q_1$ $1D_2$-$1Q_2$ $1D_3$-$1Q_3$ $1D_0$-$1Q_0$ $1D_1$-$1Q_1$ $1D_2$-$1Q_2$ $1D_3$-$1Q_3$ $2D_0$-$2Q_0$ $2D_1$-$2Q_1$ $2D_2$-$2Q_2$ $2D_3$-$2Q_3$ $2D_0$-$2Q_0$ $2D_1$-$2Q_1$ $2D_2$-$2Q_2$ $2D_3$-$2Q_3$		49	
	t_{PHL2}		210 211 212 213 214 215 216 217 218 219 220 221 222 223 224 225		IN GND	GND IN	IN IN	OUT OUT	IN IN	OUT OUT	IN IN	OUT OUT	IN IN	OUT OUT			IN GND	GND IN	IN IN	OUT OUT	IN IN	OUT OUT	IN IN	OUT OUT	IN IN	OUT OUT		$1D_0$-$1Q_0$ $1D_1$-$1Q_1$ $1D_2$-$1Q_2$ $1D_3$-$1Q_3$ $1D_0$-$1Q_0$ $1D_1$-$1Q_1$ $1D_2$-$1Q_2$ $1D_3$-$1Q_3$ $2D_0$-$2Q_0$ $2D_1$-$2Q_1$ $2D_2$-$2Q_2$ $2D_3$-$2Q_3$ $2D_0$-$2Q_0$ $2D_1$-$2Q_1$ $2D_2$-$2Q_2$ $2D_3$-$2Q_3$		37	

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case J,K,L,2 Test No.	1 $1\overline{MR}$	2 $1\overline{E}_0$	3 $1\overline{E}_1$	4 $1D_0$	5 $1Q_0$	6 $1D_1$	7 $1Q_1$	8 $1D_2$	9 $1Q_2$	10 $1D_3$	11 $1Q_3$	12 GND	13 $2\overline{MR}$	14 $2\overline{E}_0$	15 $2\overline{E}_1$	16 $2D_0$	17 $2Q_0$	18 $2D_1$	19 $2Q_1$	20 $2D_2$	21 $2Q_2$	22 $2D_3$	23 $2Q_3$	24 V_{CC}	Meas. terminal	Test limits Min	Max	Unit
10 T_A = 125°C	t_{PHL3}	3003 (Fig 7-C)	226	IN	IN	GND	5.0 v	OUT	5.0 v	OUT	5.0 v	OUT	5.0 v	OUT	GND	IN	IN	GND	5.0 v	OUT	5.0 v	OUT	5.0 v	OUT	5.0 v	OUT	5.0 v	$1\overline{MR}$-$1Q_0$	3	37	ns
			227																									$1\overline{MR}$-$1Q_1$			
			228																									$1\overline{MR}$-$1Q_2$			
			229																									$1\overline{MR}$-$1Q_3$			
			230		GND	IN		OUT																				$1\overline{MR}$-$2Q_0$			
			231							OUT																		$1\overline{MR}$-$2Q_1$			
			232									OUT																$1\overline{MR}$-$2Q_2$			
			233											OUT														$1\overline{MR}$-$2Q_3$			
			234													IN	IN	GND	5.0 v	OUT	5.0 v		5.0 v		5.0 v			$2\overline{MR}$-$1Q_0$			
			235																			OUT						$2\overline{MR}$-$1Q_1$			
			236																					OUT				$2\overline{MR}$-$1Q_2$			
			237														GND	IN		OUT						OUT		$2\overline{MR}$-$1Q_3$			
			238																									$2\overline{MR}$-$2Q_0$			
			239																			OUT						$2\overline{MR}$-$2Q_1$			
			240																					OUT				$2\overline{MR}$-$2Q_2$			
			241																							OUT		$2\overline{MR}$-$2Q_3$			
11	Same tests, terminal conditions and limits as for subgroup 10, except T_A = -55°C.																														

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TABLE III. Group A inspection for device type 04.

Terminal conditions (pins not designated may be H $\geq$ 2.0 V, or L $\leq$ 0.8 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	1 E	2 $\overline{S}_0$	3 D_0	4 D_1	5 $\overline{S}_2$	6 D_2	7 D_3	8 GND	9 $\overline{MR}$	10 Q_3	11 $\overline{S}_3$	12 Q_2	13 Q_1	14 $\overline{S}_1$	15 Q_0	16 V_{CC}	Meas. terminal	Test limits Min	Max	Unit
1 $T_A = 25°C$	V_{OH}	3006	1	0.8 V	0.8 V	2.0 V	2.0 V	0.8 V	2.0 V	2.0 V	GND	2.0 V		0.8 V			0.8 V	-800μA	4.5 V	Q_0	2.4		V
			2													-800μA				Q_1			
			3												-800 μA					Q_2			
			4										-800 μA							Q_3			
	V_{OL}	3007	5			0.8 V	0.8 V		0.8 V	0.8 V								16 mA		Q_0		0.4	
			6													16 mA				Q_1			
			7												16 mA					Q_2			
			8										16 mA							Q_3			
	V_{IC}		9	-12mA																$\overline{E}$		-1.5	
			10		-12 mA															$\overline{S}_0$			
			11			-12mA														D_0			
			12				-12 mA													D_1			
			13					-12 mA												$\overline{S}_2$			
			14						-12 mA											D_2			
			15							-12 mA										D_3			
			16									-12 mA								$\overline{MR}$			
			17											-12 mA						$\overline{S}_3$			
			18														-12 mA			$\overline{S}_1$			
	I_{IL1}	3009	19	GND	GND	0.4 V		GND						GND			GND		5.5 V	D_0	-0.7	-2.7	mA
			20				0.4 V													D_1			
			21						0.4 V											D_2			
			22							0.4 V										D_3			
	I_{IL2}		23	0.4 V																$\overline{E}$		-1.6	
			24		0.4 V															$\overline{S}_0$			
			25					0.4 V												S_2			
			26									0.4 V								$\overline{MR}$			
			27											0.4 V						$\overline{S}_3$			
			28														0.4 V			S_1			
	I_{IH1}	3010	29	5.5 V	5.5 V	2.4 V		5.5 V				GND		5.5 V			5.5 V			D_0		80	μA
			30				2.4 V													D_1			
			31						2.4 V											D_2			
			32							2.4 V										D_3			
	I_{IH2}		33			5.5 V														D_0		200	
			34				5.5 V													D_1			
			35						5.5 V											D_2			
			36							5.5 V										D_3			
	I_{IH3}		37	2.4 V																$\overline{E}$		40	
			38		2.4 V															$\overline{S}_0$			
			39					2.4 V												S_2			
			40									2.4 V								$\overline{MR}$			
			41											2.4 V						$\overline{S}_3$			
			42														2.4 V			S_1			
	I_{IH4}		43	5.5 V																$\overline{E}$		100	
			44		5.5 V															$\overline{S}_0$			
			45					5.5 V												S_2			
			46									5.5 V								$\overline{MR}$			
			47											5.5 V						$\overline{S}_3$			
			48														5.5 V			S_1			

See note at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits Min	Max	Unit
				$\overline{E}$	$\overline{S}_0$	D_0	D_1	$\overline{S}_2$	D_2	D_3	GND	$\overline{MR}$	Q_3	$\overline{S}_3$	Q_2	Q_1	$\overline{S}_1$	Q_0	V_{CC}				
1 T_A = 25°C	I_{OS}	3011	49 50 51 52	GND	GND	4.5 v	4.5 v	GND	4.5 v	4.5 v	GND	5.5 v	GND	GND	GND	GND	GND	GND	5.5 v	Q_0 Q_1 Q_2 Q_3	-20	-100	mA
	I_{CC}	3005	53	4.5 v	GND			GND			GND	GND		GND			GND			V_{CC}		55	mA
2	Same tests, terminal conditions and limits as for subgroup 1, except T_A = 125°C and V_{IC} tests are omitted.																						
3	Same tests, terminal conditions and limits as for subgroup 1, except T_A = -55°C and V_{IC} tests are omitted.																						
9 T_A = 25°C	t_{PLH1}	3003 (Fig 8-A)	54 55 56 57	IN	GND	IN	IN	GND	IN	IN	GND	5.0 v	OUT	GND	OUT	OUT	GND	OUT	5.0 v	$\overline{E}$ -Q_0 $\overline{E}$ -Q_1 $\overline{E}$ -Q_2 $\overline{E}$ -Q_3	9	30	ns
	t_{PHL1}	3003 (Fig 8-B)	58 59 60 61		GND	IN	IN	GND	IN	IN			OUT	GND	OUT	OUT	GND	OUT		$\overline{E}$ -Q_0 $\overline{E}$ -Q_1 $\overline{E}$ -Q_2 $\overline{E}$ -Q_3		29	
	t_{PHL1}	3003 (Fig 8-C)	62 63 64 65		GND	IN	IN	GND	IN	IN			OUT	GND	OUT	OUT	GND	OUT		$\overline{E}_0$-Q_0 $\overline{E}_1$-Q_1 $\overline{E}_2$-Q_2 $\overline{E}_3$-Q_3			
	t_{PLH2}	3003 (Fig 8-B)	66 67 68 69		GND	IN	IN	GND	IN	IN			OUT	GND	OUT	OUT	GND	OUT		D_0-Q_0 D_1-Q_1 D_2-Q_2 D_3-Q_3		21	
	t_{PLH2}	3003 (Fig 8-C)	70 71 72 73		GND	IN	IN	GND	IN	IN			OUT	GND	OUT	OUT	GND	OUT		D_0-Q_0 D_1-Q_1 D_2-Q_2 D_3-Q_3			
	t_{PLH2}	3003 (Fig 8-D)	74 75 76 77	GND	GND	IN	IN	GND	IN	IN			OUT	GND	OUT	OUT	GND	OUT		D_0-Q_0 D_1-Q_1 D_2-Q_2 D_3-Q_3			
	t_{PHL2}	3003 (Fig 8-E)	78 79 80 81	GND	GND	IN	IN	GND	IN	IN			OUT	GND	OUT	OUT	GND	OUT		D_0-Q_0 D_1-Q_1 D_2-Q_2 D_3-Q_3	3	30	
	t_{PHL2}	3003 (Fig 8-A)	82 83 84 85	IN	GND	IN	IN	GND	IN	IN			OUT	GND	OUT	OUT	GND	OUT		D_0-Q_0 D_1-Q_1 D_2-Q_2 D_3-Q_3			

See note at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	1 $\overline{E}$	2 $\overline{S}_0$	3 D_0	4 D_1	5 $\overline{S}_2$	6 D_2	7 D_3	8 GND	9 $\overline{MR}$	10 Q_3	11 $\overline{S}_3$	12 Q_2	13 Q_1	14 $\overline{S}_1$	15 Q_0	16 V_{cc}	Meas. terminal	Test limits Min	Max	Unit
9 T_A = 25°C	t_{PHL3}	3003 (Fig 8-F)	86 87 88 89	IN	GND	5.0 v	5.0 v	GND	5.0 v	5.0 v	GND	IN	OUT	GND	OUT	OUT	GND	OUT	5.0 v	$\overline{MR}$-Q_0 $\overline{MR}$-Q_1 $\overline{MR}$-Q_2 $\overline{MR}$-Q_3	9	23	ns
	t_{PLH4}	3003 (Fig 8-E)	90 91 92 93	GND	IN	IN	IN	IN	IN	IN		5.0 v	OUT	IN	OUT	OUT	IN	OUT		$\overline{S}_0$-Q_0 $\overline{S}_1$-Q_1 $\overline{S}_2$-Q_2 $\overline{S}_3$-Q_3		29	
10 T_A = 125°C	t_{PLH1}	3003 (Fig 8-A)	94 95 96 97	IN	GND	IN	IN	GND	IN	IN			OUT	GND	OUT	OUT	GND	OUT		$\overline{E}$ -Q_0 $\overline{E}$ -Q_1 $\overline{E}$ -Q_2 $\overline{E}$ -Q_3		47	
	t_{PHL1}	3003 (Fig 8-B)	98 99 100 101		GND	IN	IN	GND	IN	IN			OUT	GND	OUT	OUT	GND	OUT		$\overline{E}$ -Q_0 $\overline{E}$ -Q_1 $\overline{E}$ -Q_2 $\overline{E}$ -Q_3		33	
	t_{PHL1}	3003 (Fig 8-C)	102 103 104 105		GND	IN	IN	GND	IN	IN			OUT	GND	OUT	OUT	GND	OUT		$\overline{E}_0$-Q_0 $\overline{E}_1$-Q_1 $\overline{E}_2$-Q_2 $\overline{E}_3$-Q_3			
	t_{PLH2}	3003 (Fig 8-B)	106 107 108 109		GND	IN	IN	GND	IN	IN			OUT	GND	OUT	OUT	GND	OUT		D_0-Q_0 D_1-Q_1 D_2-Q_2 D_3-Q_3		37	
	t_{PLH2}	3003 (Fig 8-C)	110 111 112 113		GND	IN	IN	GND	IN	IN			OUT	GND	OUT	OUT	GND	OUT		D_0-Q_0 D_1-Q_1 D_2-Q_2 D_3-Q_3			
	t_{PLH2}	3003 (Fig 8-D)	114 115 116 117	GND	IN	IN	IN	IN	IN	IN			OUT	IN	OUT	OUT	IN	OUT		D_0-Q_0 D_1-Q_1 D_2-Q_2 D_3-Q_3			
	t_{PHL2}	3003 (Fig 8-E)	118 119 120 121	GND	IN	IN	IN	IN	IN	IN			OUT	IN	OUT	OUT	IN	OUT		D_0-Q_0 D_1-Q_1 D_2-Q_2 D_3-Q_3	3		
	t_{PHL2}	3003 (Fig 8-A)	122 123 124 125	IN	GND	IN	IN	GND	IN	IN			OUT	GND	OUT	OUT	GND	OUT		D_0-Q_0 D_1-Q_1 D_2-Q_2 D_3-Q_3			

See note at end of device type 04.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits Min	Max	Unit
				$\overline{E}$	$\overline{S}_0$	D_0	D_1	$\overline{S}_2$	D_2	D_3	GND	$\overline{MR}$	Q_3	$\overline{S}_3$	Q_2	Q_1	$\overline{S}_1$	Q_0	V_{cc}				
10 T_A = 125 °C	t_{PHL3}	3003 (Fig 8-F)	126 127 128 129	IN	GND	5.0 v	5.0 v	GND	5.0 v	5.0 v	GND	IN	OUT	GND	OUT	OUT	GND	OUT	5.0 v	$\overline{MR}$-Q_0 $\overline{MR}$-Q_1 $\overline{MR}$-Q_2 $\overline{MR}$-Q_3	9	30	ns
	t_{PLH4}	3003 (Fig 8-E)	130 131 132 133	GND	IN	IN	IN	IN	IN	IN		5.0 v	OUT	IN	OUT	OUT	IN	OUT		$\overline{S}_0$-Q_0 $\overline{S}_1$-Q_1 $\overline{S}_2$-Q_2 $\overline{S}_3$-Q_3		47	
11	Same tests, terminal conditions and limits as subgroup 10, except T_A = -55 °C.																						

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type
01	5475, 7475 (circuit A)
01	SN5475, SN7475 (circuit B)
02	5477, 7477 (circuit A)
02	SN5477, SN7477 (circuit B)
03	9308 (circuit A)
03	54116, 74116 and SN74116 (circuit B)
03	S54116 (circuit C)
04	9314 (circuit A)
04	AM9314 (circuit B)

Custodians:
Army - ER
Navy - EC
Air Force - 17

Review activities:
Army - AR, MI
Air Force - 11, 80, 85
NASA - NA
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC, OS, SH
Air Force - 19

Preparing activity:
Air Force - 17

Agent:
DLA - ES

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