µPC834, 4064

Low Power Consumption J-FET Input Quad Operational Amplifier

R03DS0153EJ0100
Rev.1.00
2019.11.12

DESCRIPTION

The µPC834 and 4064 are low power consumption versions operational amplifier of µPC804 and 4084 series with the general-purpose J-FET input. This revolutionary J-FET input operational amplifier realizes low power consumption of I_{CC} 800 µA TYP. and low voltage operation from ± 2 V. Owing to its J-FET input, the input impedance is high. The AC characteristics are also greatly improved compared to the conventional low power consumption operational amplifier. Therefore, it is ideal for application circuits such as amplifier circuits and active filters in various battery-operated electronic devices.

Depending on the operating ambient temperature, µPC834 is suitable for communication application while µPC4064 is suitable for general-purpose usage.

Along with this series of lineup, the dual type op-amp µPC832 and 4062 with same circuit configuration are also available.

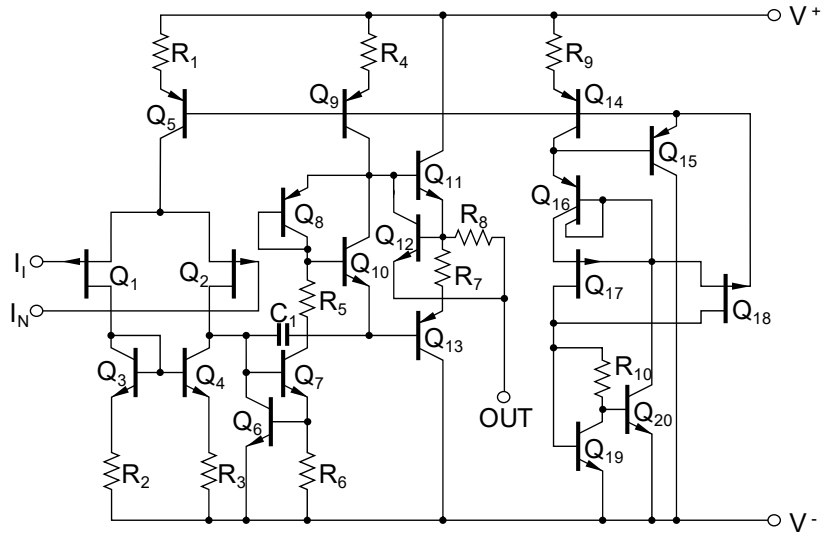
FEATURES

- Input Offset Voltage ±2 mV (TYP.)
- Input Bias Current 10 pA (TYP.)
- Slew Rate 3 V/µs (TYP.)
- Unity Gain Frequency 1 MHz (TYP.)
- Circuit Current 800 µA (TYP.)
- Operate from ±2 V
- Built-In Phase Compensation Circuit
- Built-In Output Short Circuit Protection
- Standard Quad Op-Amp terminal connection (pin compatible)

ORDERING INFORMATION

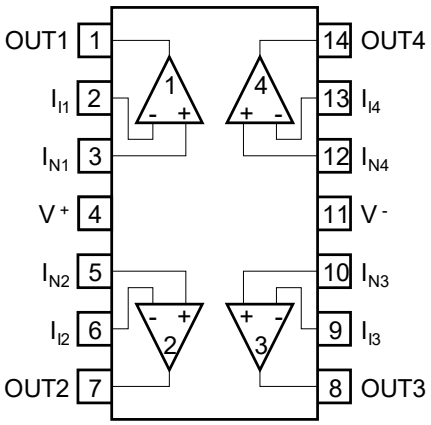
Ordering Name	Package
µPC834G2-A	14 pin plastic SOP (5.72 mm (225 mil))
µPC4064G2-A	14 pin plastic SOP (5.72 mm (225 mil))

EQUIVALENT CIRCUIT (1/4 Circuit)



PIN CONFIGURATION (Top View)

µPC834G2, µPC4064G2



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

PARAMETER	SYMBOL	μPC834G2	μPC4064G2	UNIT
Supply Voltage Note1	V^+ to V^-	-0.3 to +36		V
Differential Input Voltage	V_{ID}	±30		V
Input Voltage Note2	V_I	V^- -0.3 to V^+ +0.3		V
Output Applied Voltage Note3	V_O	V^- -0.3 to V^+ +0.3		V
Total Power Dissipation Note4	P_T	550		mW
Output Short Circuit Duration Note5		indefinite		s
Operating Ambient Temperature	T_A	-40 to +85	-20 to +80	°C
Storage Temperature	T_{stg}	-55 to +125		°C

[Note] 1. Note that reverse connections of the power supply may damage the ICs.

2. The input terminal must be applied within the input voltage range to avoid deteriorating or damaging the device characteristic. Do not exceed the ratings including during transition state such as ON/OFF, etc. The Op-Amp input voltage must operate within the electrical characteristics range of input common-mode voltage.

3. The output terminal must be applied within the output voltage range to avoid deteriorating or damaging the device characteristic. Do not exceed the ratings including during transition state such as ON/OFF, etc. The Op-Amp output voltage must operate within the electrical characteristics range of maximum output voltage.

4. This is the value at $T_A \leq +25$ °C. De-rate value at -5.5 mW/°C when $T_A > 25$ °C.

5. Please use the total loss and the de-rating value from Note 4.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power Supply Voltage	$V^\pm$	±2		±16	V
Output Current (SOURCE)	$I_{O\ SOURCE}$			5	mA
Output Current (SINK)	$I_{O\ SINK}$			3.5	mA
Load Capacitance (When A_V = +1)	C_L			100	pF

ELECTRICAL CHARACTERISTICS (T_A = 25 °C, $V^{\pm}$ = ±15 V)

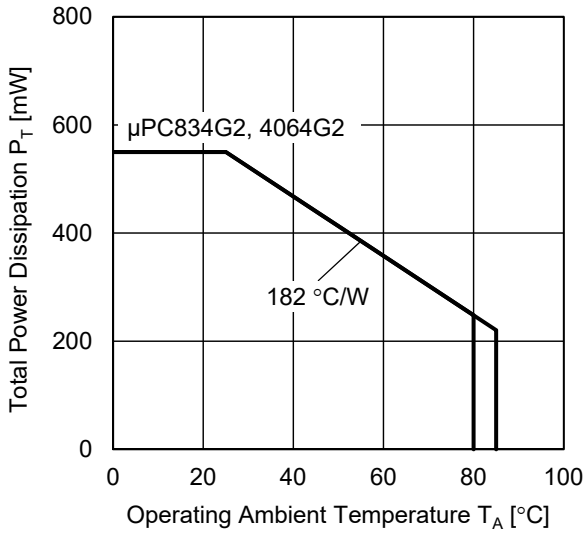
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input Offset Voltage	V_{IO}		±2	±10	mV	R_S ≤ 50 Ω
Input Offset Current	I_{IO}		±5	±50	pA	
Input Bias Current Note6	I_B		10	100	pA	
Large Signal Voltage Gain	A_V	3000	9000			R_L ≥ 10 kΩ, V_O = ±10 V
Circuit Current Note7	I_{CC}		800	1000	μA	I_O = 0 A
Common Mode Rejection Ratio	CMR	70	90		dB	
Supply Voltage Rejection Ratio	SVR	70	90		dB	
Voltage Output Swing	V_{om}	±12	+14.0 -13.6		V	R_L ≥ 10 kΩ
Input Common-Mode Voltage Range	V_{ICM}	±12	+15 -13		V	
Slew Rate	SR		3		V/μs	A_V = 1
Unity Gain Frequency	f_{unity}		1		MHz	
Input Referred Noise Voltage Density	e_n		30		nV/$\sqrt{Hz}$	R_S = 100 Ω, f = 1 kHz
Channel Separation			120		dB	
Input Offset Voltage	V_{IO}			±15	mV	R_S ≤ 50 Ω, T_A = -20 to +70 °C
Average V_{IO} Temperature Drift	$\Delta V_{IO}/\Delta T$		±10		μV/°C	T_A = -20 to +70 °C
Input Offset Current	I_{IO}			±2	nA	T_A = -20 to +70 °C
Input Bias Current Note6	I_B			3.5	nA	T_A = -20 to +70 °C

[Note] 6. The direction of the input bias current is the same direction that flows into the IC because the first stage is comprised of Pch J-FET. When T_J = 25 °C or higher, it increases exponentially with increase in temperature (please see I_B vs. T_A characteristics). During measurement, please kindly take care of $T_J \fallingdotseq T_A$

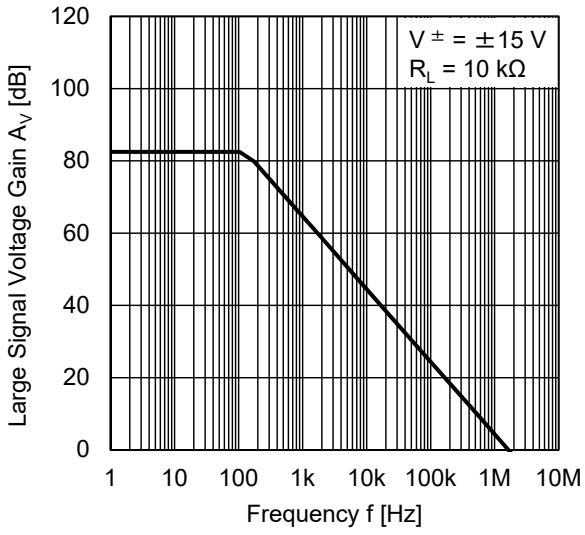
7. It is the current that flows into the internal circuit. This current flow is irrespective of the channel usage.

ELECTRICAL CHARACTERISTICS CURVE (T_A = 25 °C, TYP.) (REFERENCE VALUE)

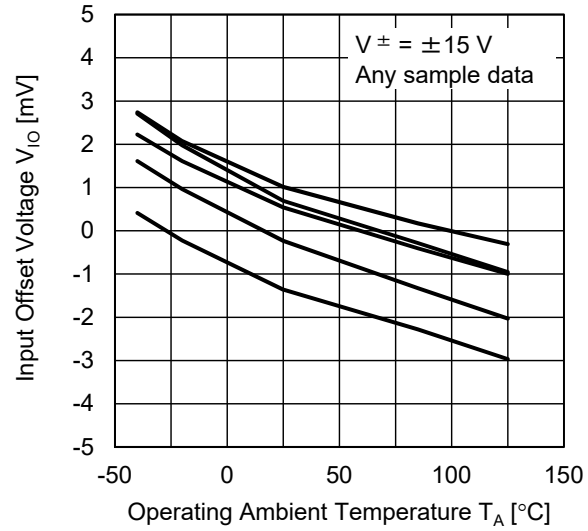
P_T vs. T_A (Absolute maximum rating)



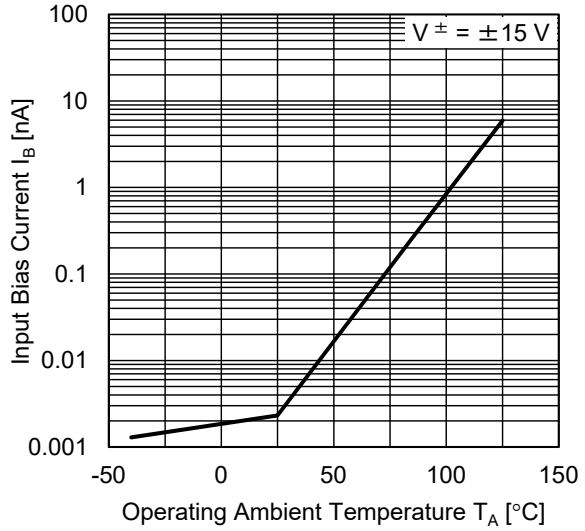
A_V vs. f



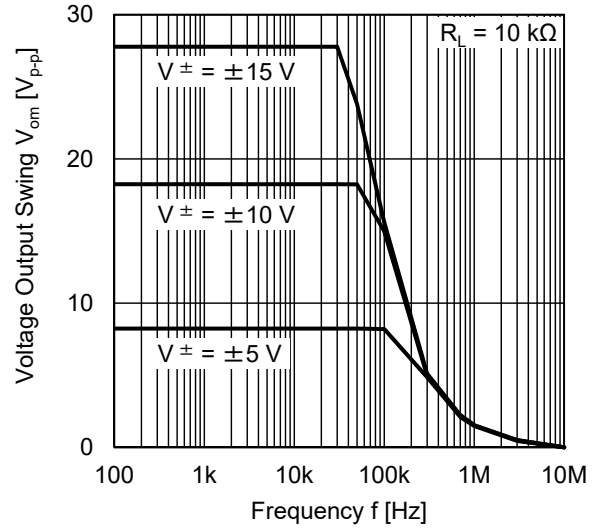
V_{IO} vs. T_A



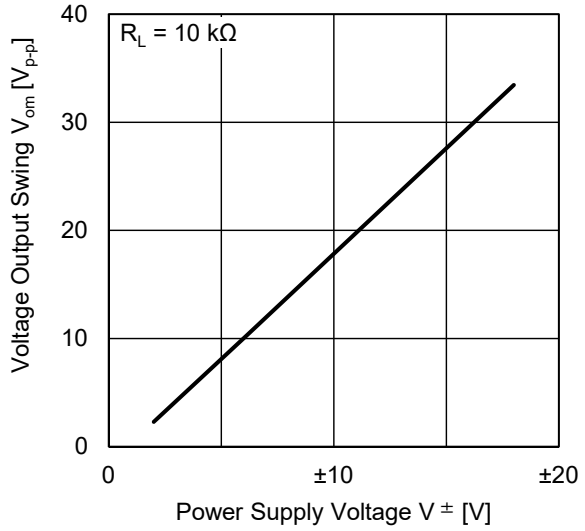
I_B vs. T_A



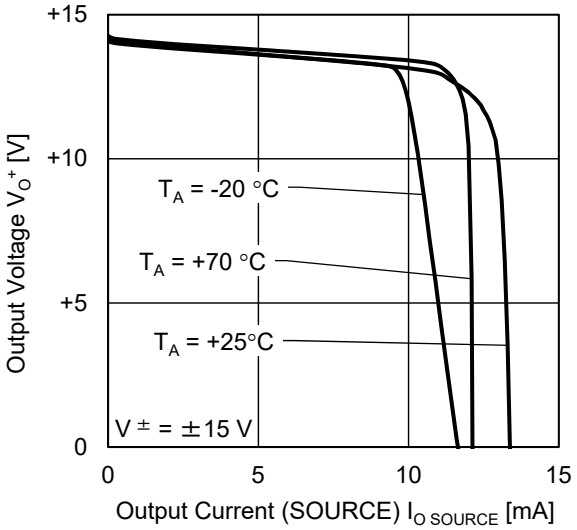
V_{om} vs. f



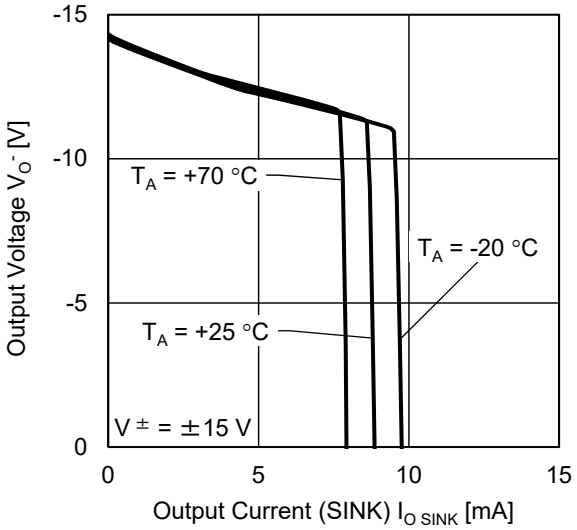
V_{om} vs. $V^{\pm}$



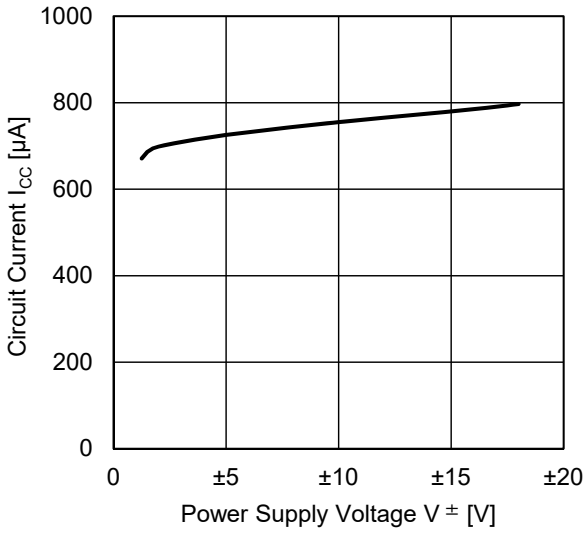
V_O^+ vs. $I_{O\ SOURCE}$



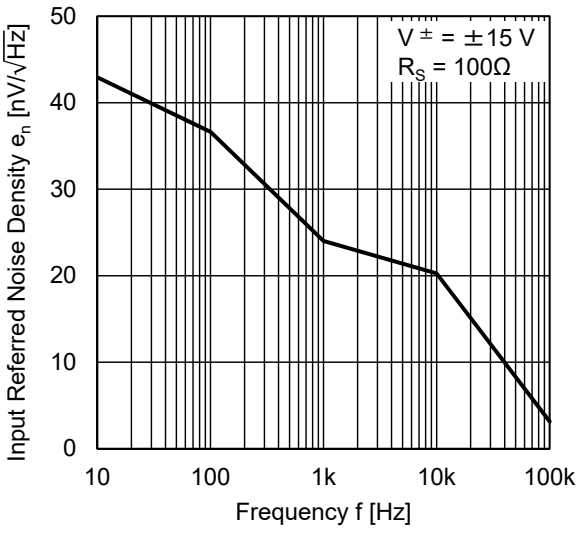
V_O^- vs. $I_{O\ SINK}$



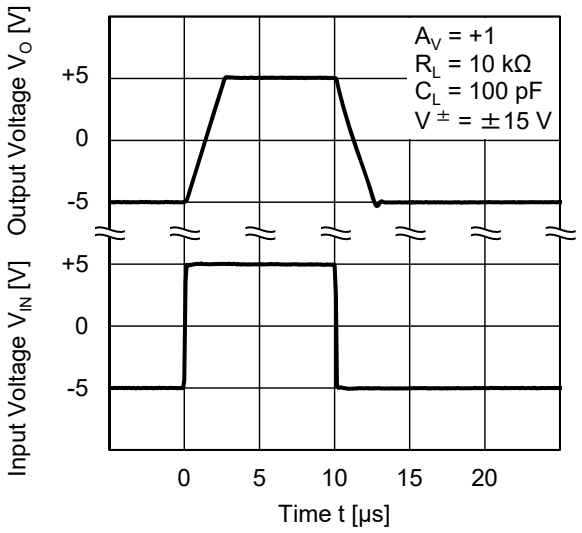
I_{CC} vs. V ±



e_n vs. f



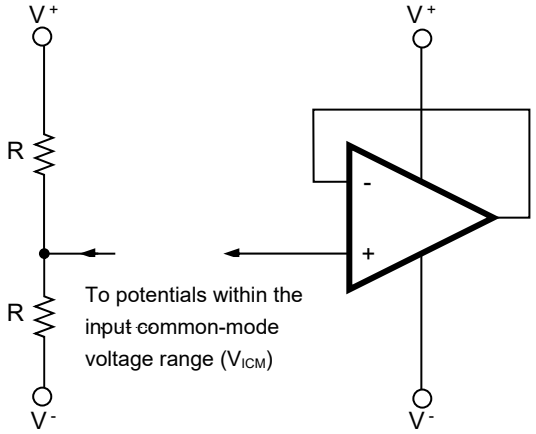
Pulse Response Characteristics



USE WITH PRECAUTIONS

- Managing unused circuits
  If there is an unused circuit, the following connection is recommended.

Example of handling unused circuit



Note in this example, an intermediate voltage of V^+ and V^- is applied.

- **Power Supply (Dual Power Supply / Single Power Supply)**
  The op-amp operates when a predetermine voltage is applied between V^+ to V^-. Therefore, while it operates from a single power supply (V^- = GND), it is not possible to operate the input and output near GND. So please be careful of the common-mode input voltage range and maximum output voltage.

- **Ratings of input/output pin voltage**
  When the voltage of input/output pin exceeds the absolute maximum rating, the parasitic diode within the IC may conduct, causing characteristics degradation or damage. In addition, if the voltage of input pin is lower than V^-, or the voltage of output pin exceeds the power supply voltage, it is recommended to make a clamping circuit using a diode with low forward voltage (e.g.: Schottky diode) as protection.

- **Input common-mode voltage range**
  When the supply voltage does not meet the condition of electrical characteristics, the input common-mode voltage range is as follows.
  V_{ICM} (TYP.): V^- +2 to V^+ [V] (T_A = 25 °C)

  During designing, do include some margin by considering characteristic variations, temperature characteristics etc.

- **Maximum Output Voltage**
  When the supply voltage does not meet the condition of electrical characteristics, the TYP. value range of the maximum output voltage is as follows:
  $V_{om}{}^+$ (TYP.): V^+ -1 [V] (T_A = 25 °C), $V_{om}{}^-$ (TYP.): V^- +1.4 [V] (T_A = 25 °C)

  During designing, do include some margin by considering characteristic variations, temperature characteristics and so on. In addition, also note that the output voltage range ($V_{om}{}^+$ to $V_{om}{}^-$) will become narrow when the output current increases.

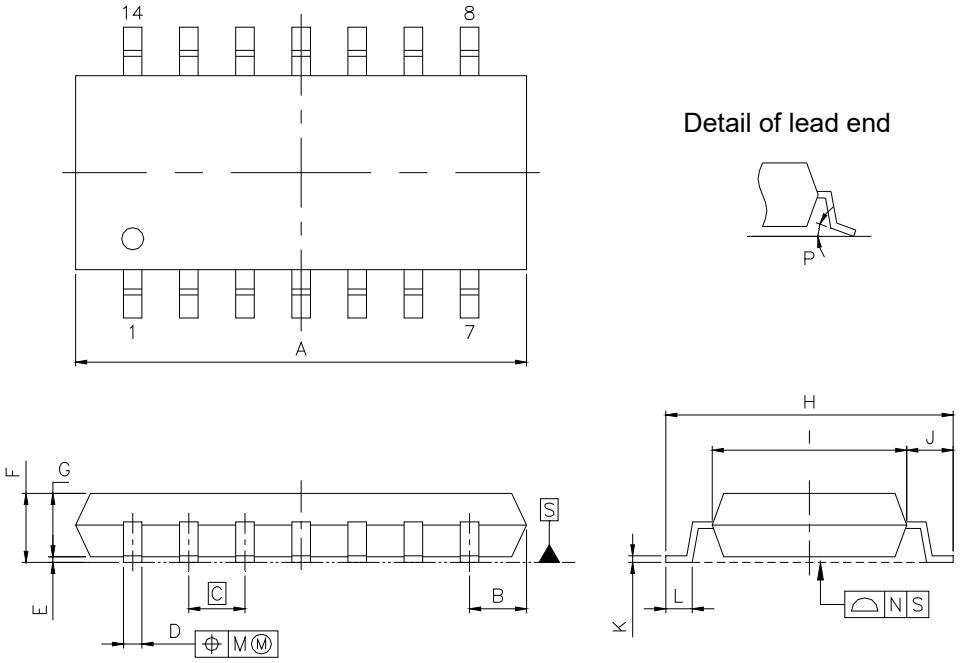
- **Handling of ICs**
  When stress is added to the ICs due to warpage or bending of a board, the characteristic may fluctuate due to piezoelectric (piezo) effect. Therefore, pay attention to warpage or bending of a board.

PACKAGE DRAWINGS

14-PIN PLASTIC SOP

JEITA Package code	RENESAS code	Previous code	MASS (TYP.) [g]
P-SOP14-0225-1.27	PRSP0014DI-A	P14GR-50-225B	0.14

Unit: mm



NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	10.2 ±0.26
B	1.42 MAX
C	1.27 (T.P)
D	0.42 +0.08 -0.07
E	0.1 ±0.1
F	1.59 +0.21 -0.2
G	1.49
H	6.5 ±0.2
I	4.4 ±0.1
J	1.1 ±0.16
K	0.17 +0.08 -0.07
L	0.6 ±0.2
M	0.1
N	0.10
P	3° +7° -3°

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9. 不可将瑞萨电子产品和技术用于或者嵌入日本国内或海外相应的法律法规所禁止生产、使用及销售的任何产品或系统中。也不可将瑞萨电子产品或技术用于(1)与大规模杀伤性武器（例如核武器、化学武器、生物武器或运送此等武器的导弹，包括无人机(UAV)）的开发、设计、制造、使用、存储等相关的任何目的；(2)与常规武器的开发、设计、制造或使用相关的任何目的；(3)扰乱国际和平与安全的任何其他目的，并且不可向任何第三方销售、出口、租赁、转让、或让与瑞萨电子产品或技术，无论直接或间接知悉或者有理由知悉该第三方或任何其他方将从事上述活动。用户必须遵守对各方或交易行使司法管辖权的任意国家/地区政府所公布和管理的任何适用出口管制法律法规。
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