

PART NUMBER

54F74BCA-ROCS

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

54F/74F74

Dual D-Type Positive Edge-Triggered Flip-Flop

General Description

The 'F74 is a dual D-type flip-flop with Direct Clear and Set inputs and complementary (Q , \bar{Q}) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

LOW input to \bar{S}_D sets Q to HIGH level
 LOW input to \bar{C}_D sets Q to LOW level
 Clear and Set are independent of clock
 Simultaneous LOW on \bar{C}_D and \bar{S}_D
 makes both Q and \bar{Q} HIGH

Features

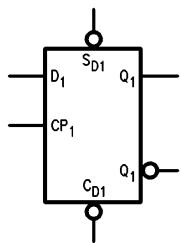
- Guaranteed 4000V minimum ESD protection

Commercial	Military	Package Number	Package Description
74F74PC		N14A	14-Lead (0.300" Wide) Molded Dual-In-Line
	54F74DM (Note 2)	J14A	14-Lead Ceramic Dual-In-Line
74F74SC (Note 1)		M14A	14-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F74SJ (Note 1)		M14D	14-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F74FM (Note 2)	W14B	14-Lead Cerpak
	54F74LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

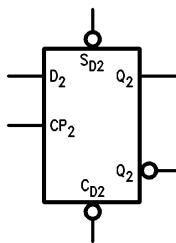
Note 1: Devices also available in 13" reel. Use Suffix = SCX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

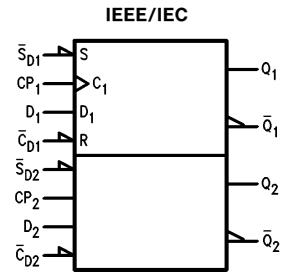
Logic Symbols



TL/F/9469-3



TL/F/9469-4

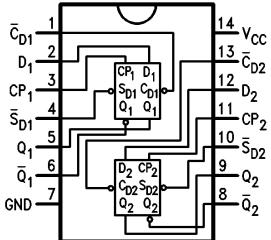


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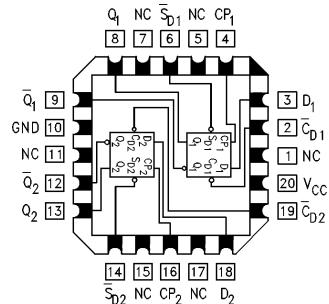
Connection Diagrams

Pin Assignment
for DIP, SOIC, and Flatpak



TL/F/9469-1

Pin Assignment
for LCC



TL/F/9469-2

Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_1, D_2	Data Inputs	1.0/1.0	$20 \mu A/ -0.6 mA$
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	1.0/1.0	$20 \mu A/ -0.6 mA$
$\bar{C}_{D1}, \bar{C}_{D2}$	Direct Clear Inputs (Active LOW)	1.0/3.0	$20 \mu A/ -1.8 mA$
$\bar{S}_{D1}, \bar{S}_{D2}$	Direct Set Inputs (Active LOW)	1.0/3.0	$20 \mu A/ -1.8 mA$
$Q_1, \bar{Q}_1, Q_2, \bar{Q}_2$	Outputs	50/33.3	$-1 mA/20 mA$

Truth Table

Inputs				Outputs	
\bar{S}_D	\bar{C}_D	CP	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	—	h	H	L
H	H	—	l	L	H
H	H	L	X	Q_0	\bar{Q}_0

H (h) = HIGH Voltage Level

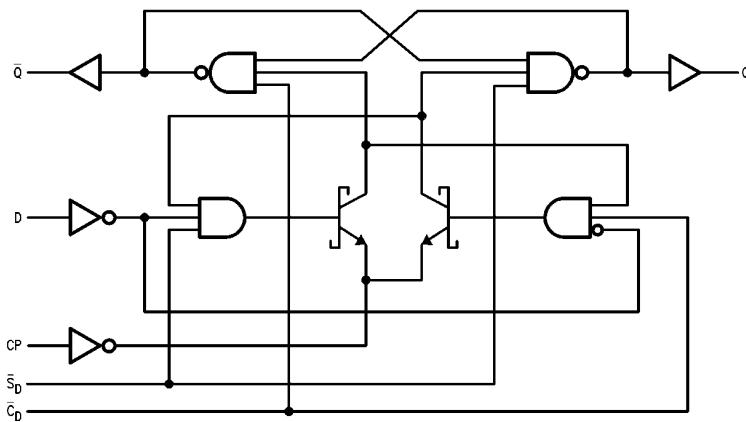
L (l) = LOW Voltage Level

X = Immaterial

Q_0 = Previous Q (\bar{Q}) before LOW-to-HIGH Clock Transition

Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias Plastic	−55°C to +175°C −55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with $V_{CC} = 0V$)	−0.5V to V_{CC}
Standard Output	−0.5V to +5.5V
TRI-STATE® Output	−0.5V to +5.5V

Current Applied to Output
in LOW State (Max) twice the rated I_{OL} (mA)

ESD Last Passing Voltage (Min) 4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage		0.8		V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage		−1.2		V	Min	$I_{IN} = −18\text{ mA}$
V_{OH}	Output HIGH Voltage	54F 10% V_{CC} 74F 10% V_{CC} 74F 5% V_{CC}	2.5 2.5 2.7		V	Min	$I_{OH} = −1\text{ mA}$ $I_{OH} = −1\text{ mA}$ $I_{OH} = −1\text{ mA}$
V_{OL}	Output LOW Voltage	54F 10% V_{CC} 74F 10% V_{CC}		0.5 0.5	V	Min	$I_{OL} = 20\text{ mA}$ $I_{OL} = 20\text{ mA}$
I_{IH}	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	$V_{IN} = 2.7\text{ V}$
I_{BVI}	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	$V_{IN} = 7.0\text{ V}$
I_{CEX}	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	$V_{OUT} = V_{CC}$
V_{ID}	Input Leakage Test	74F	4.75		V	0.0	$I_{ID} = 1.9\text{ }\mu\text{A}$ All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	$V_{IOD} = 150\text{ mV}$ All Other Pins Grounded
I_{IL}	Input LOW Current			−0.6 −1.8	mA	Max	$V_{IN} = 0.5\text{ V (D, CP)}$ $V_{IN} = 0.5\text{ V }(\bar{C}_D, \bar{S}_D)$
I_{OS}	Output Short-Circuit Current	−60	−150		mA	Max	$V_{OUT} = 0\text{ V}$
I_{CC}	Power Supply Current		10.5	16.0	mA	Max	

AC Electrical Characteristics

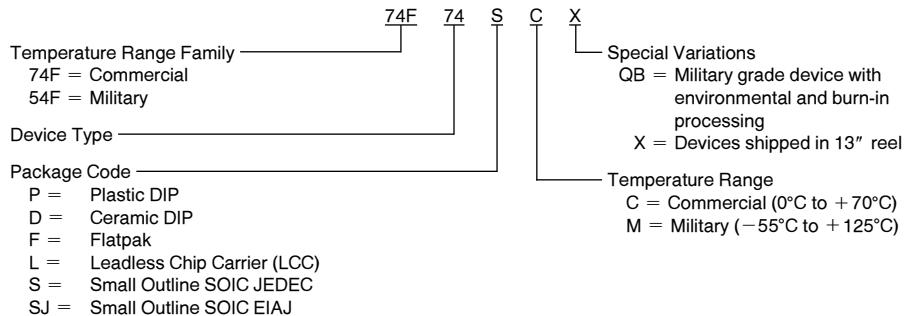
Symbol	Parameter	74F			54F		74F		Units	
		$T_A = +25^\circ C$ $V_{CC} = +5.0V$ $C_L = 50 pF$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50 pF$		$T_A, V_{CC} = \text{Com}$ $C_L = 50 pF$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	125		80		100		MHz	
t_{PLH}	Propagation Delay CP_n to Q_n or \bar{Q}_n	3.8	5.3	6.8	3.8	8.5	3.8	7.8	ns	
t_{PHL}	Propagation Delay \bar{C}_{Dn} or \bar{S}_{Dn} to Q_n or \bar{Q}_n	4.4	6.2	8.0	4.4	10.5	4.4	9.2	ns	
t_{PLH}	Propagation Delay \bar{C}_{Dn} or \bar{S}_{Dn} to Q_n or \bar{Q}_n	3.2	4.6	6.1	3.2	8.0	3.2	7.1	ns	
t_{PHL}	Propagation Delay \bar{C}_{Dn} or \bar{S}_{Dn} to Q_n or \bar{Q}_n	3.5	7.0	9.0	3.5	11.5	3.5	10.5	ns	

AC Operating Requirements

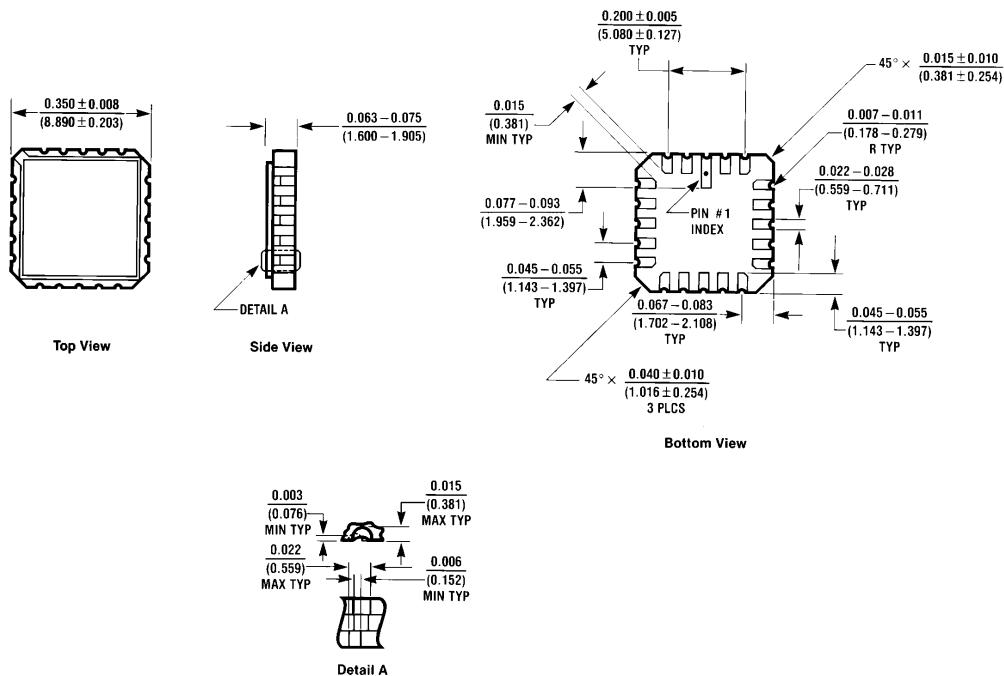
Symbol	Parameter	74F		54F		74F		Units	
		$T_A = +25^\circ C$ $V_{CC} = +5.0V$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(H)$	Setup Time, HIGH or LOW D_n to CP_n	2.0		3.0		2.0		ns	
$t_s(L)$		3.0		4.0		3.0			
$t_h(H)$	Hold Time, HIGH or LOW D_n to CP_n	1.0		2.0		1.0		ns	
$t_h(L)$		1.0		2.0		1.0			
$t_w(H)$	CP_n Pulse Width HIGH or LOW	4.0		4.0		4.0		ns	
$t_w(L)$		5.0		6.0		5.0			
$t_w(L)$	\bar{C}_{Dn} or \bar{S}_{Dn} Pulse Width LOW	4.0		4.0		4.0		ns	
t_{rec}	Recovery Time \bar{C}_{Dn} or \bar{S}_{Dn} to CP	2.0		3.0		2.0		ns	

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



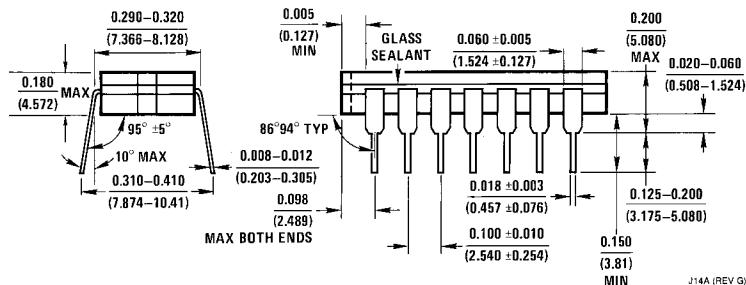
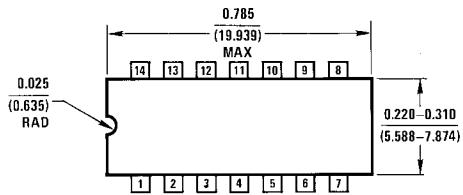
Physical Dimensions inches (millimeters)



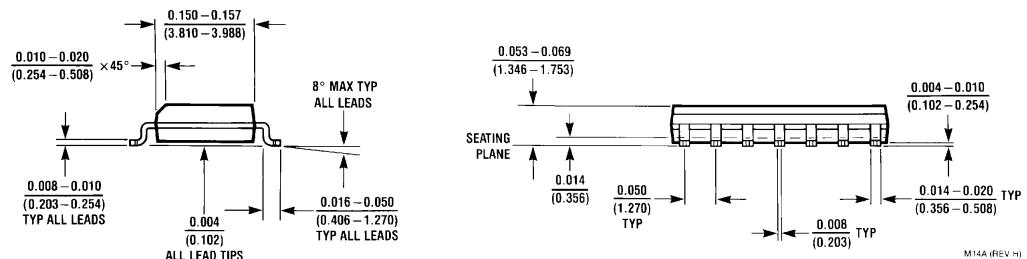
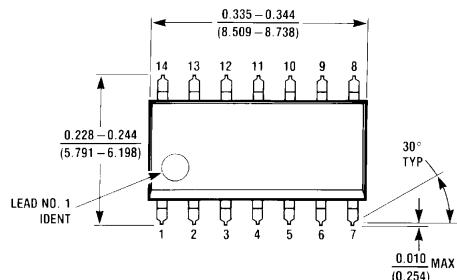
20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

E20A (REV D)

Physical Dimensions inches (millimeters) (Continued)

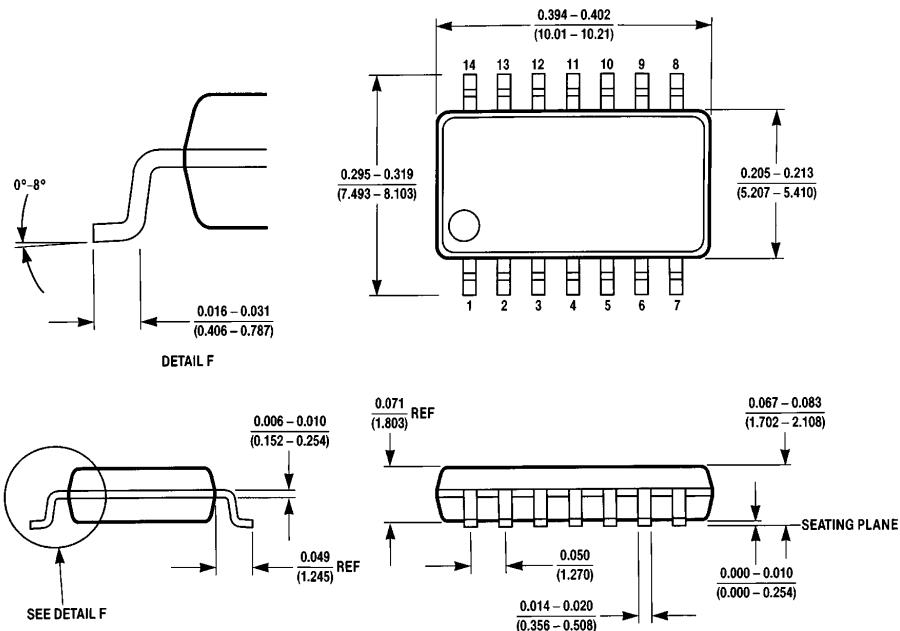


**14-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J14A**

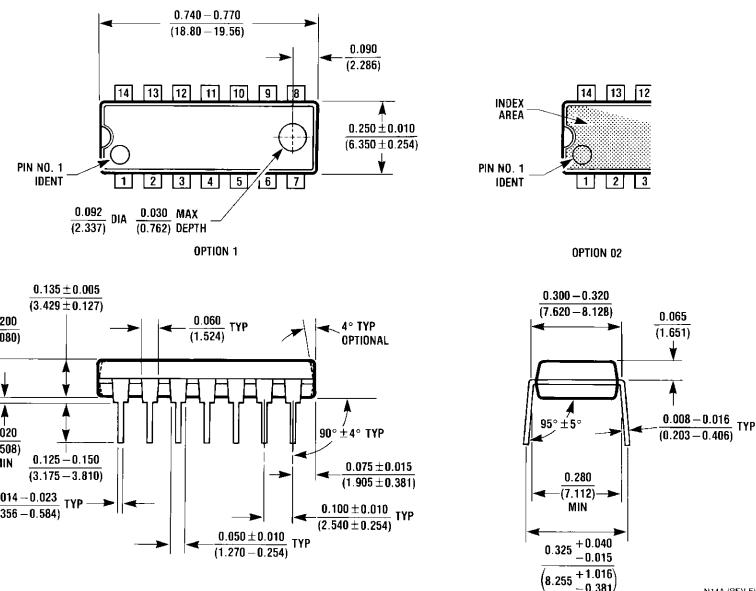


**14-Lead (0.150" Wide) Molded Small Outline, JEDEC (S)
NS Package Number M14A**

Physical Dimensions inches (millimeters) (Continued)



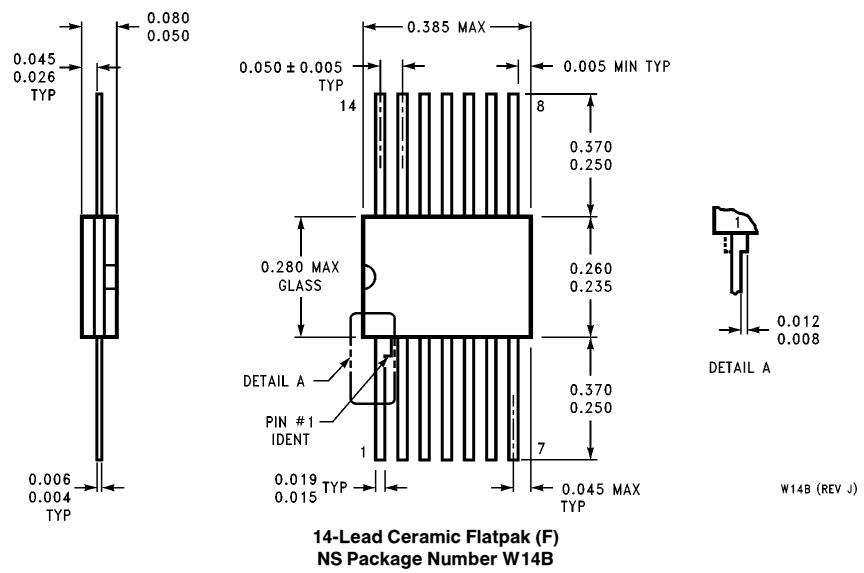
**14-Lead (0.300" Wide) Molded Small Outline, EIAJ (SJ)
NS Package Number M14D**



**14-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N14A**

54F/74F74 Dual D-Type Positive Edge-Triggered Flip-Flop

Physical Dimensions inches (millimeters) (Continued)



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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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