

**MC2126 • MC2176
MC2026 • MC2076**

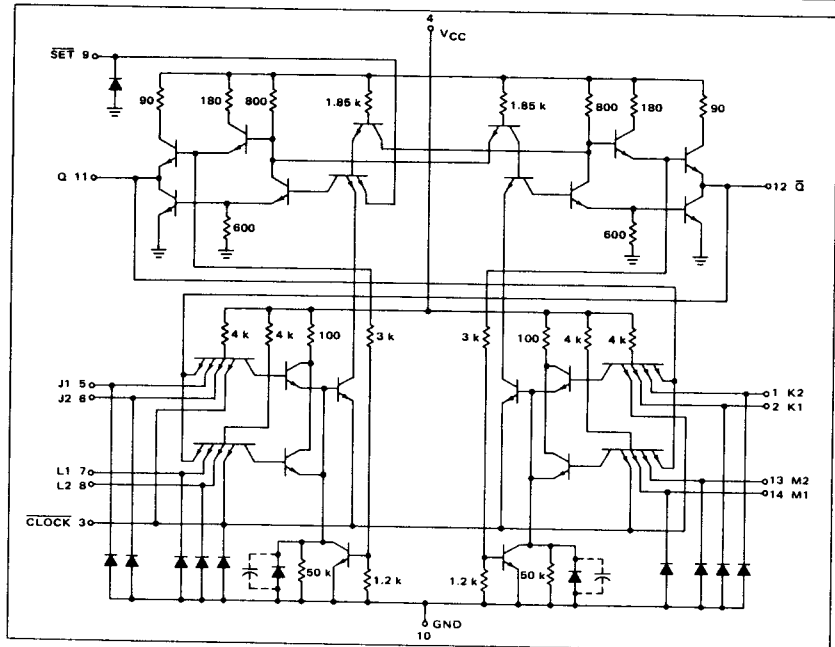
The MC2026, MC2076, MC2126, and MC2176 are clocked flip-flops that toggle at 50 MHz, trigger on the negative edge of the clock input pulse, and perform the J-K logic function. Each flip-flop has a positive logic AND-OR input gating configuration that consists of two clocked J inputs ANDed together, two clocked K inputs ANDed together, two clocked L inputs ANDed together, and two clocked M inputs ANDed together. The J and L inputs are ORed together and the K and M inputs are ORed together. A direct SET input is also available. These devices are pin compatible with the MC2110 series of devices. Electrical differences include the input loading factor for the SET input, which is approximately twice that of the MC2110 series.

Information is changed on the clocked inputs while the clock is in the low state, since the inputs are inhibited in this condition. Information is transferred into a temporary memory through the AND-OR input gating when the clock goes to the high state. When the clock returns low, the information in the temporary memory is transferred to the bistable section and the Q and $\bar{Q}$ outputs respond accordingly. The information on the clocked inputs should not be changed while the clock is high.

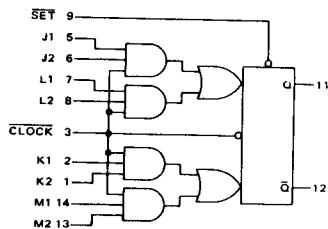
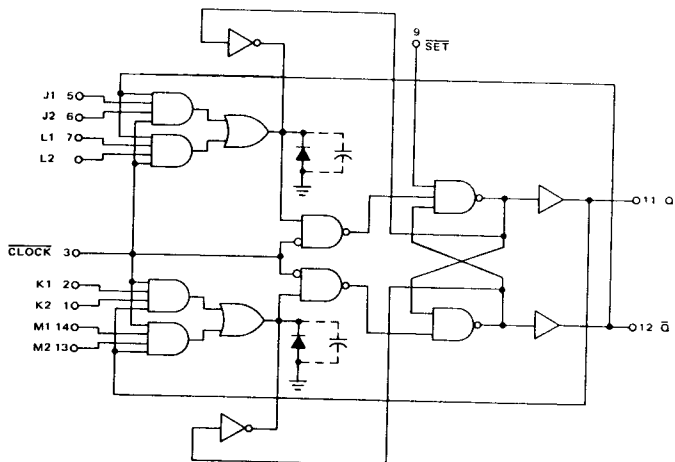
Each flip-flop can be set directly by applying a low state to the direct SET input. Since these flip-flops are charge-storage devices, there is a restriction on the clock fall time that must be observed.

The AND-OR input configuration of each flip-flop makes it useful for shift right/shift left registers and for up/down counters.

TYPE NO.	INPUT LOADING FACTOR (ip)						OUTPUT DRIVE	(IOL)	TEMPERATURE RANGE
	CLOCK	SET	J, K, L, M	CLOCK	SET	J, K, L, M			
MC2126 MC2176	2.0	1.2	0.67	(-2.66 mA)	(-2.4 mA)	(-1.33 mA)	11 MC2100 series Gates 6 MC2100 series Gates	(22.0 mA) (12.0 mA)	-55°C to +125°C
MC2026 MC2076	2.0	1.2	0.67	(-3.32 mA)	(-2.8 mA)	(-1.66 mA)	9 MC2000 series Gates 5 MC2000 series Gates	(22.5 mA) (12.5 mA)	0°C to +75°C



LOGIC DIAGRAM



J	L	K	M	Q_n	Q_{n+1}
0	0	X	X	0	0
1	X	X	X	0	1
X	1	X	X	0	1
X	X	0	0	1	1
X	X	1	X	1	0
X	X	X	1	1	0

X = Don't Care

Where $J = J1 + J2$
 $L = L1 + L2$
 $K = K1 + K2$
 $M = M1 + M2$

Total Power Dissipation - 60 mW typ/pkg

Switching Times:

$t_{pd} = 11$ ns typ

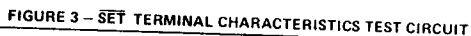
$t_{pd1} = 9.0$ ns typ

Operating Frequency - 70 MHz typ

The maximum allowable clock skew time is 9.0 ns. This is the total of the minimum time to recognize a "0" to "1" logic state change (4.0 ns) and the minimum propagation delay (5.0 ns).

Timing diagram for the input pulse conditions of the 74VHC00. The diagram shows three waveforms: TP_{in} , $Q (\bar{Q})$ OUTPUT, and $\bar{Q} (Q)$ OUTPUT. The input pulse TP_{in} has a period of 10 ns, high time of 5 ns, and low time of 5 ns. The high level is 1.5 V and the low level is 0 V. The output $Q (\bar{Q})$ is inverted and has a propagation delay t_{pd} of 1.5 ns. The output $\bar{Q} (Q)$ is non-inverted and has a propagation delay t_{pd} of 1.5 ns. The output levels are 2.0 V for high and 1.0 V for low. The maximum output voltage is 2.0 V and the minimum output voltage is 1.0 V. The input pulse width is 1.5 V and the input pulse height is 0.2 V max.

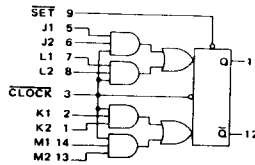
INPUT PULSE CONDITIONS							
SYMBOL	V	W	X	Y	Z	UNIT	
PRF	5.0	50	5.0	5.0	1.0	MHz	
PW	≤ 5.0	10	10	10	200	ns	
t_r	≤ 5.0	2.0	≤ 5.0	≤ 5.0	50	ns	
t_f	≤ 5.0	2.0	≤ 5.0	≤ 5.0	100	ns	
V_{IH}	3.0	3.0	3.0	2.4	3.0	Volt	



MC2126, MC2176/MC2026, MC2076 (continued)

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J and one K input, as well as the SET and CLOCK inputs. The remaining J, K, L, and M inputs are tested in the same manner.



Characteristic	Symbol	Pin Under Test	MC2126, MC2176 Test Limits						MC2026, MC2076 Test Limits						Unit	
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C			
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Input																
Forward Current	I_F	J	5	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc
		K	1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc
		Set	9	-	-2.4	-	-2.4	-	-2.4	-	-2.8	-	-2.8	-	-2.8	mAdc
		Clock	3	-	-2.66	-	-2.66	-	-2.66	-	-3.32	-	-3.32	-	-3.32	mAdc
Leakage Current	I_N	J	5	-	70	-	70	-	70	-	70	-	70	-	70	μ Adc
		K	1	-	70	-	70	-	70	-	70	-	70	-	70	μ Adc
		Set	9	-	280	-	280	-	280	-	280	-	280	-	280	μ Adc
		Clock	3	-	280	-	280	-	280	-	280	-	280	-	280	μ Adc
Inverse Beta Current	I_L	J	5	-	70	-	70	-	70	-	70	-	70	-	70	μ Adc
		K	1	-	70	-	70	-	70	-	70	-	70	-	70	μ Adc
		Set	9	-	280	-	280	-	280	-	280	-	280	-	280	μ Adc
		Clock	3	-	280	-	280	-	280	-	280	-	280	-	280	μ Adc
Breakdown Voltage	$BV_{in}^{(0)}$	J	5	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	Vdc	
		K	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	Vdc	
		Set	9	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	Vdc	
		Clock	3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	Vdc	
	$BV_{in}^{(1)}$	J	5	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	Vdc	
		K	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	Vdc	
		Set	9	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	Vdc	
		Clock	3	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	Vdc	
Output																
Output Voltage	$V_{out}^{(0)}$	11	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	
	$V_{out}^{(1)}$	11	2.5	-	2.4	-	2.5	-	2.5	-	2.4	-	2.5	Vdc		
Leakage Current	I_{OLK}	11	-	1.25	-	1.25	-	1.25	-	1.25	-	1.25	-	1.25	mAdc	
		12	-	1.25	-	1.25	-	1.25	-	1.25	-	1.25	-	1.25	mAdc	
Short-Circuit Current	I_{SC}	11	-30	-90	-30	-90	-30	-90	-30	-90	-30	-90	-30	-90	mAdc	
		12	-30	-90	-30	-90	-30	-90	-30	-90	-30	-90	-30	-90	mAdc	
Output Voltage	V_{OL}	11	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	
		12	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	
	V_{OH}	11	2.8	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0	-	Vdc	
		12	2.8	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0	-	Vdc	
Power Requirements																
Power Supply Drain	I_{PD}	4	-	16	-	16	-	16	-	19	-	19	-	19	mAdc	
		4	-	16	-	16	-	16	-	19	-	19	-	19	mAdc	

*Prime Fan-Out.

**Momentarily apply -0.5 V prior to taking measurement to set flip-flop in desired state.

†Momentarily ground pin prior to taking measurement to set flip-flop in desired state. Return pin to specified voltage or current for measurement.

‡Release ground on pin 9 prior to taking measurement.

		TEST CURRENT / VOLTAGE VALUES																						
		mA							Volts															
		I_{OL}		I_{OH}		I_{in}		$2I_{in}$		$4I_{in}$		V_R		V_R		V_{in1}		V_{in0}		V_{out}		V_{CC}		
@ Test Temperature		Pr*	Std	Pr*	Std	I_{in}	$2I_{in}$	$4I_{in}$	V_R	V_R	V_R	V_{in1}	V_{in0}	V_{out}	V_{CC}									
MC2126*, MC2176		-55°C	22.0	12.0	-2.2	-1.1	1.0	2.0	4.0	0.45	2.8	4.5	2.0	0.9	5.5	5.0								
		+25°C	22.0	12.0	-2.2	-1.1	1.0	2.0	4.0	0.45	2.8	4.5	1.8	1.1	5.5	5.0								
		+125°C	22.0	12.0	-2.2	-1.1	1.0	2.0	4.0	0.45	2.8	4.5	1.5	0.9	5.5	5.0								
MC2026*, MC2076		0°C	22.5	12.5	-1.8	-1.0	1.0	2.0	4.0	0.45	3.0	4.5	1.9	1.0	5.5	5.0								
		+25°C	22.5	12.5	-1.8	-1.0	1.0	2.0	4.0	0.45	3.0	4.5	1.8	1.1	5.5	5.0								
		+75°C	22.5	12.5	-1.8	-1.0	1.0	2.0	4.0	0.45	3.0	4.5	1.7	1.0	5.5	5.0								
		TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:																						
Characteristic	Symbol	Pin Under Test	I_{OL}	I_{OH}	I_{in}	$2I_{in}$	$4I_{in}$	V_R	V_R	V_R	V_{in1}	V_{in0}	V_{out}	V_{CC}	**	Gnd								
Input																								
Forward Current	I_P	5	-	-	-	-	-	-	-	1, 2, 3, 6, 7, 8, 13, 14	-	-	-	4	11	3, 10								
		1	-	-	-	-	-	-	-	2, 3, 5, 6, 7, 8, 13, 14	-	-	-	-	-	4, 9, 10								
		9	-	-	-	-	-	-	-	1, 2, 3, 5, 6, 7, 8, 13, 14	-	-	-	-	-	9, 10								
		3	-	-	-	-	-	3	-	1, 2, 5, 6, 7, 8, 13, 14	-	-	-	-	-	10								
Leakage Current	I_R	5	-	-	-	-	-	-	-	5	-	-	-	4	11	3, 6, 7, 8, 9, 10								
		1	-	-	-	-	-	-	-	1	-	-	-	-	-	2, 3, 10, 13, 14								
		9	-	-	-	-	-	-	-	9†	-	-	-	-	-	1, 10								
		3	-	-	-	-	-	-	-	3	-	-	-	-	-	1, 2, 10, 13, 14								
Inverse Beta Current	I_L	5	-	-	-	-	-	-	-	5	-	-	-	4	11	10								
		1	-	-	-	-	-	-	-	1	-	-	-	-	-	-								
		9	-	-	-	-	-	9	-	9	-	-	-	-	-	-								
		3	-	-	-	-	-	-	-	3	-	-	-	-	-	-								
		3	-	-	-	-	-	-	-	8	-	-	-	-	-	-								
Breakdown Voltage	BV_{in-0}	5	-	-	5	-	-	-	-	-	-	-	-	4	11	10								
		1	-	-	1	-	-	9	-	-	-	-	-	-	-	-								
		9	-	-	9	-	-	-	-	-	-	-	-	-	-	-								
		3	-	-	3	-	-	9	-	-	-	-	-	-	-	-								
		3	-	-	-	-	-	9	-	-	-	-	-	-	-	-								
	BV_{in-1}	5	-	-	5	-	-	-	-	-	-	-	-	4	11	-								
		1	-	-	1	-	-	-	-	-	-	-	-	-	-	3, 8, 9, 10								
		9	-	-	9†	-	-	-	-	-	-	-	-	-	-	2, 3, 10, 13, 14								
		3	-	-	-	-	3	-	-	-	-	-	-	-	-	1, 10								
Output																								
Output Voltage	V_{out-0}	11	11	-	-	-	-	-	-	-	9	-	-	4	11	3, 10								
	V_{out-1}	11	-	11	-	-	-	-	-	-	-	9	-	4	-	3, 10								
Leakage Current	I_{OLK}	11	-	-	-	-	-	-	-	-	-	-	11	8	-	1, 2, 3, 5, 6, 7, 8, 9, 10, 13, 14								
		12	-	-	-	-	-	-	-	9	-	-	-	12	4	1, 2, 3, 5, 6, 7, 8, 10, 13, 14								
Short-Circuit Current	I_{SC}	11	-	-	-	-	-	-	-	-	-	-	-	4	11	1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 13, 14								
		12	-	-	-	-	-	-	-	9	-	-	-	-	-	1, 2, 3, 5, 6, 7, 8, 10, 12, 13, 14								
Output Voltage	V_{OL}	11	11	-	-	-	-	-	-	-	-	-	-	4	11	3, 10								
		12	12	-	-	-	-	9	9	-	-	-	-	-	-	3, 10								
	V_{OH}	11	-	11	-	-	-	-	9	-	-	-	-	-	-	3, 10								
		12	-	12	-	-	-	-	-	-	-	-	-	-	-	3, 10								
Power Requirements																								
Power Supply Drain	I_{PD}	4	-	-	-	-	-	-	-	-	-	-	-	4	-	3, 9, 10								
		4	-	-	-	-	-	-	-	-	-	-	-	4	11	3, 10								

Pin-out and Package Information

Table 3-4 DSP56001A Identification by Signal Name (Continued)

Signal Name	132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.	Signal Name	132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.
WT	45	L13	nc	103	
X/Y	48	N13	nc	107	
XTAL	126	A6	nc	110	
nc	3		nc	116	
nc	4		nc	117	
nc	7		nc	122	
nc	17		nc	125	
nc	18		nc	132	
nc	21				

Power and ground pins have special considerations for noise immunity. See the section **Design Considerations**.

Table 3-5 DSP56001A Power Supply Pins

132 pin “FC” PQFP or “FE” CQFP Pin No.	88 pin “RC” PGA Pin No.	Power Supply	Circuit Supplied
63	L8	VCCN	Address Bus Buffers
64			
55	L6	GNDN	
56	L9		
73			
74			