MPQ6533

Three-Channel Automotive Pre-Driver, AEC-100 Qualified

DESCRIPTION

The MPQ6533 is a gate driver IC designed for automotive DC motor driver applications. The device drives six N-channel power MOSFETs to drive DC motors or other loads.

The MPQ6533 integrates an LDO regulator to generate gate drive voltages for the low-side MOSFETs. The device also provides a charge pump that generates a voltage to drive an external N-channel MOSFET for reverse battery protection. The high-side gate drive is generated by the bootstrap capacitors and an internal charge pump, which allows for 100% duty cycle operation.

An internal amplifier measures the voltage drop across the low-side MOSFETs. This allows the current to be measured without using shunt resistors.

Internal safety features include configurable over-current protection (OCP), adjustable dead time control, under-voltage lockout (UVLO), and thermal shutdown.

The MPQ6533 is available in a QFN-32 (5mmx5mm) package with an exposed thermal pad.

FEATURES

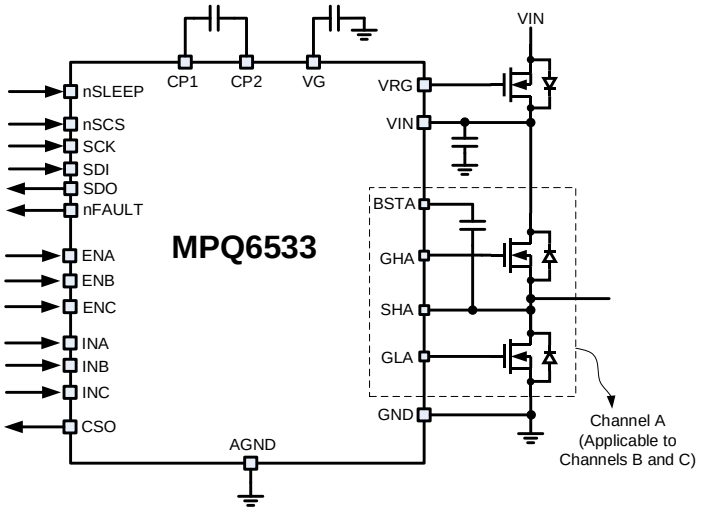
- Integrated LDO Regulator for Gate Drive
- Charge Pump for External N-Channel MOSFET Reverse Battery Protection
- Current-Sense Amplifier that Measures the Drop Across the Low-Side MOSFETs
- Low-Power Sleep Mode
- Configurable Short-Circuit Protection
- Adjustable Slew Rate Control
- Adjustable Dead Time Control
- Over-Temperature Shutdown
- Under-Voltage Warning and Shutdown
- Open and Short Load Detection
- Serial Peripheral Interface (SPI)
- Fault Indication Output
- Available in a QFN-32 (5mmx5mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Actuators
- Brushed DC Motor Drivers

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ6533GUE-AEC1	QFN-32 (5mmx5mm)	*See Below*	3

* For Tape & Reel, add suffix -Z (e.g. MPQ6533GUE-AEC1-Z).

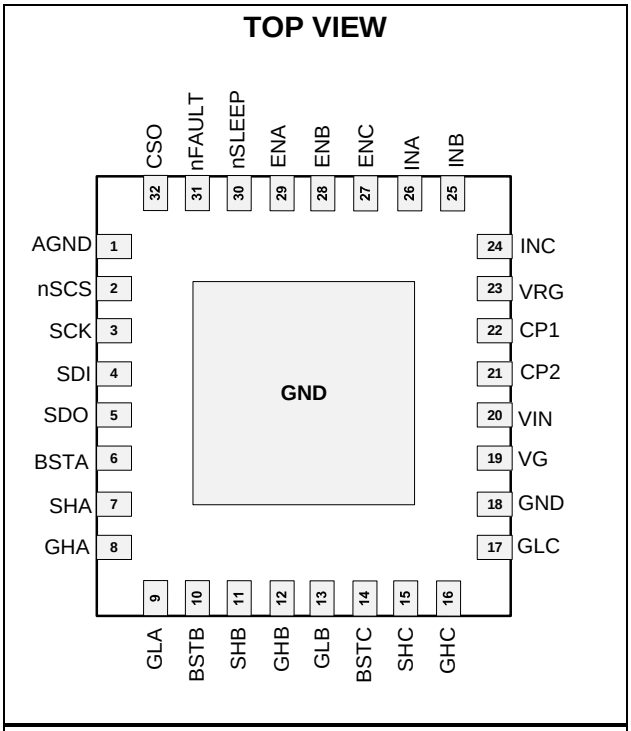
TOP MARKING

MPSYYWW
MP6533
LLLLLLL
E

MPS: MPS prefix
YY: Year code
WW: Week code
MP6533: Product code of MPQ6533GUE-AEC1
LLLLLLL: Lot number
E: Wettable lead flank

PACKAGE REFERENCE

TOP VIEW



QFN-32 (5mmx5mm)

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PIN FUNCTIONS

Pin #	Name	Description
18	GND	**Power ground.**
1	AGND	**Analog ground.**
20	VIN	**Input supply voltage.** Bypass VIN with a minimum 1μF, X7R ceramic capacitor connected to ground. Additional bulk capacitance may be required.
22	CP1	**Reverse battery gate drive charge pump capacitor.** Connect a 220nF, X7R ceramic capacitor between the CP1 and CP2 pins.
21	CP2	
19	VG	**Gate drive LDO output voltage.** Connect a 10μF, 10V, X7R ceramic capacitor from VG to ground.
23	VRG	**Reverse battery MOSFET gate drive output.**
6	BSTA	**Channel A bootstrap capacitor.** Place a ceramic capacitor between BSTA and SHA.
7	SHA	**Channel A output (drain of the low-side MOSFET, source of the high-side MOSFET).**
8	GHA	**Channel A high-side gate drive output.**
9	GLA	**Channel A low-side gate drive output.**
10	BSTB	**Channel B bootstrap capacitor.** Place a ceramic capacitor between BSTB and SHB.
11	SHB	**Channel B output (drain of the low-side MOSFET, source of the high-side MOSFET).**
12	GHB	**Channel B high-side gate drive output.**
13	GLB	**Channel B low-side gate drive output.**
13	BSTC	**Channel C bootstrap capacitor.** Place a ceramic capacitor between BSTC and SHC.
15	SHC	**Channel C output (drain of the low-side MOSFET, source of the high-side MOSFET).**
16	GHC	**Channel C high-side gate drive output.**
17	GLC	**Channel C low-side gate drive output.**
29	ENA	**Channel A enable input.** The ENA pin is pulled down internally.
28	ENB	**Channel B enable input.** The ENB pin is pulled down internally.
29	ENC	**Channel C enable input.** The ENC pin is pulled down internally.
26	INA	**Channel A input.** The INA pin is pulled down internally.
25	INB	**Channel B input.** The INB pin is pulled down internally.
24	INC	**Channel C input.** The INC pin is pulled down internally.
32	CSO	**Current-sense output.** The channel is selected by the SPI register
31	nFAULT	**Fault Indication.** The nFAULT pin pulls logic low if a fault occurs. nFAULT has an open-drain output.
5	SDO	**Serial data output.** SDO has a high impedance when nSCS = 1.
4	SDI	**Serial data input.** SDI is pulled down internally.
3	SCK	**Serial clock input.** Data is captured on the rising edge of SCK. SCK is pulled down internally.
2	nSCS	**Serial chip selection.** The nSCS pin pulls active low to enable serial data transfers. nSCS is pulled down internally.
30	nSLEEP	**Sleep mode input.** nSLEEP pulls logic low to enter low-power sleep mode. nSLEEP is pulled down internally.

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ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (V_{IN}) ..... -0.3V to +45V
VRG..... -40V to +59V
VG ..... -0.3V to +14V
CP1 ..... -0.3V to +14V
CP1 (transient <2μs) .....-1V to +15V
CP2..... V_{IN} - 1V to V_{IN} + 14V
GHA/B/C, BSTA/B/C.....
.....SHA/B/C to SHA/B/C + 14V
GHA/B/C (transient <2μs).....-8V to 59V
GLA/B/C ..... -0.3V to +14V
GLA/B/C (transient <2μs).....-5V to +15V
SHA/B/C ..... -0.3V to +45V
SHA/B/C (transient <2μs) ..... -8V to +45V
All other pins to GND ..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
QFN-32 (5mmx5mm)..... 3.4W
Storage temperature..... -55°C to +150°C
Junction temperature ..... 165°C
Lead temperature (solder) ..... 260°C

ESD Ratings

Human body model (HBM) 2kV
Charged device model (CDM) 750V

Recommended Operating Conditions (3)

Input voltage (V_{IN}) ..... 6V to 40V
Operating junction temp (T_J) .... -40°C to +150°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-32 (5mmx5mm).....36 ..... 8.... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 14V, T_A = -40° to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		6		40	V
VG LDO output voltage	V_G	I_{LDO} ≤ 5mA, V_{IN} > 13V	11	12	13	V
VG LDO resistance	R_{LDO}	V_{IN} < V_G		80		Ω
Quiescent current	I_Q	nSLEEP = 1, not switching		6	10	mA
	I_{SLEEP}	nSLEEP = 0			10	μA
Control Logic						
Input logic low threshold	V_{IL}				0.6	V
Input logic high threshold	V_{IH}		2.2			V
Logic input current	$I_{IN(H)}$	V_{IH} = 5V	-20		+20	μA
	$I_{IN(L)}$	V_{IL} = 0.8V	-20		+20	μA
Internal pull-down resistance	R_{PD}			500		kΩ
Fault Output (Open-Drain Output)						
Output low voltage	V_{OL}	I_{OUT} = 5mA			0.5	V
Output high leakage current	I_{OH}	V_{OUT} = 3.3V			1	μA
Protection Circuits						
VIN UVLO falling threshold	V_{IN_UVLO}		3.9	4.45	5	V
VIN UVLO hysteresis	V_{UV_HYS}			150		mV
VIN UV warning	V_{UV_WARN}		7.3	8	8.7	V
VBST UVLO threshold	V_{BST_UVLO}	Voltage between SHx and BSTx	1.8	2.95	4	V
VG UVLO threshold	V_{G_UVLO}		5.1	5.4	5.7	V
Short circuit threshold voltage (external low-side MOSFET V_{DS})	V_{SCP_LS}	xSC2~xSC0 = 000	80	110	140	mV
		xSC2~xSC0 = 100	450	510	570	
		xSC2~xSC0 = 111	730	810	890	
Short circuit threshold voltage (external high-side MOSFET V_{DS})	V_{SCP_HS}	xSC2~xSC0 = 000	90	120	150	mV
		xSC2~xSC0 = 100	460	520	580	
		xSC2~xSC0 = 111	740	820	900	
Open load detection threshold	V_{OLD}	Lower threshold	0.45	0.5	0.55	V
		Upper threshold	1.15	1.25	1.35	
SLEEP Wake Up Time	t_{SLEEP}		0.8	1.2	1.6	ms
Over-temperature warning	T_{OTW}			125		°C
Thermal shutdown	T_{TSD}			165		°C
Gate Drive						
Bootstrap diode forward voltage	V_{FBOOT}	I_D = 10mA		0.77	0.9	V
		I_D = 50mA		1	1.3	V
Gate drive pull up resistance	DS_O	xSR1~xSR0 = 00		175	350	Ω
		xSR1~xSR0 = 11		7.5	15	
Gate drive pull down resistance	DS_I	xSR1~xSR0 = 00		90	190	Ω
		xSR1~xSR0 = 11		2.5	6	
Dead time	t_{DEAD}	xDT2~xDT0 = 000		50		ns
		xDT2~xDT0 = 100		800		ns
		xDT2~xDT0 = 111		6.4		μs

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 14V, T_A = -40° to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Current-Sense Amplifier						
Amplifier output offset	V_{OFS}	V_{SHx} = 0V, A = 100	-10	0	+10	mV
Input voltage range	V_{IN}	LS-FET is on, A = 100	0		2	V
Amplifier gain	A_{CS}	xGN2~xGN0 = 000	18	20	22	V/V
		xGN2~xGN0 = 100	93	100	107	
		xGN2~xGN0 = 111	233	250	267	
Settling time	t_S	From LS-FET turn on, V = 100mV		3		µS

Notes:

5) Not subject to production testing; specified by design.

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TIMING CHARACTERISTICS

V_{IN} = 14V, T_A = -40° to +125°C, unless otherwise noted.

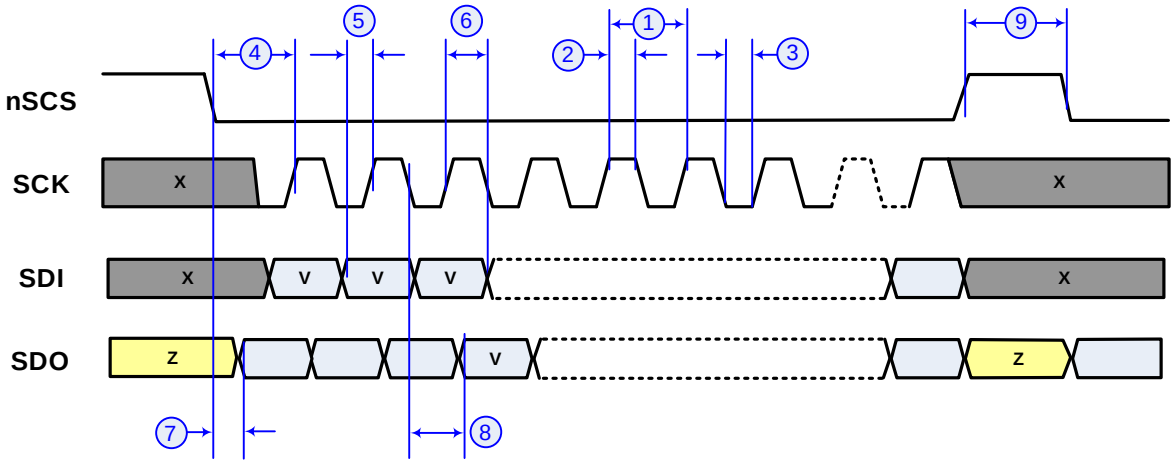


Figure 1: Serial Interface Timing Diagram

Table 1: Timing Characteristics

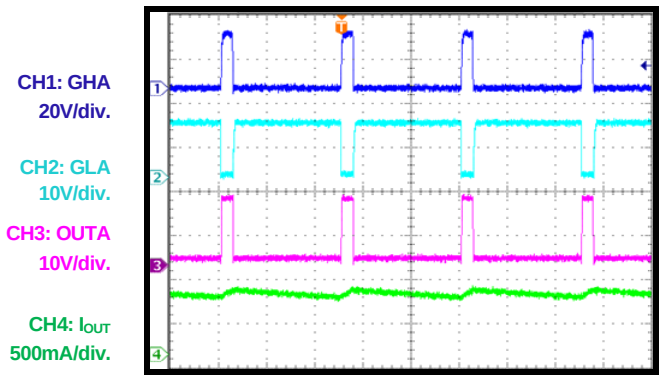
Parameter	Symbol	Condition	Min	Typ	Max	Units
SCK cycle time	t1		100			ns
SCK frequency			0.1		10	MHz
SCK high time	t2		50			ns
SCK low time	t3		50			ns
SCK rising/falling time					50	ns
Set-up time (nSCS low to SCK rising)	t4		30			ns
Set-up time (SDI valid to SCK rising)	t5		15			ns
Holding time (SCK rising to SDI invalid)	t6		10			ns
nSCS low to SDO enabled	t7		40			ns
SCK falling to SDO valid	t8	C_L < 100pF			10	ns
nSCS inactive time	t9		100			ns

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TYPICAL PERFORMANCE CHARACTERISTICS

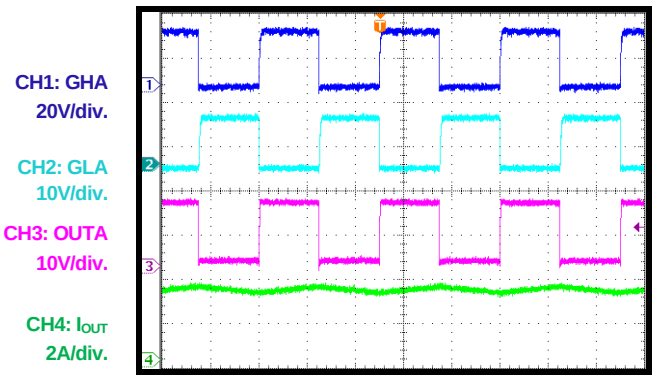
V_{IN} = 14V, T_A = 25°C, resistor + inductor load: R = 2Ω, L = 700μH, unless otherwise noted.

Normal Operation
20kHz, 10% duty cycle



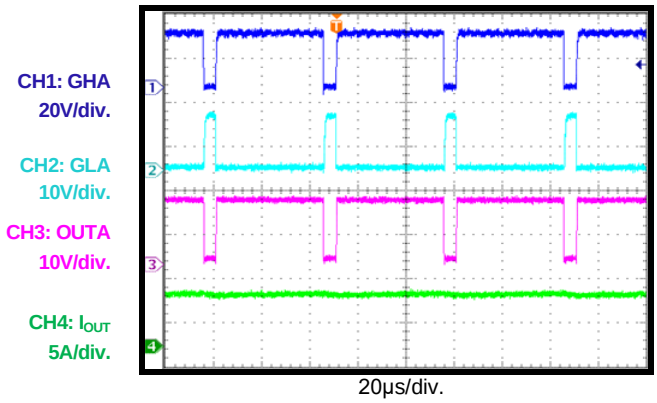
20μs/div.

Normal Operation
20kHz, 50% duty cycle



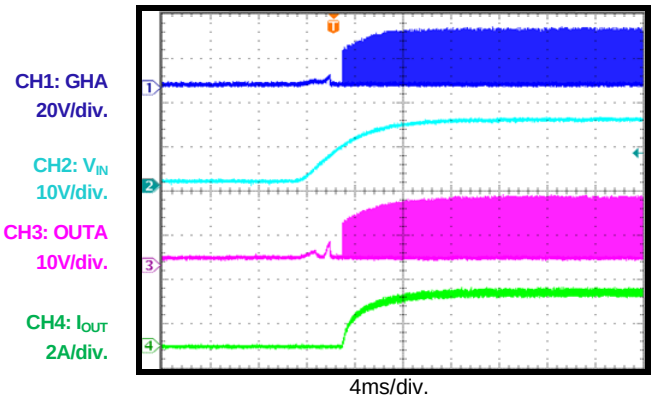
20μs/div.

Normal Operation
20kHz, 90% duty cycle



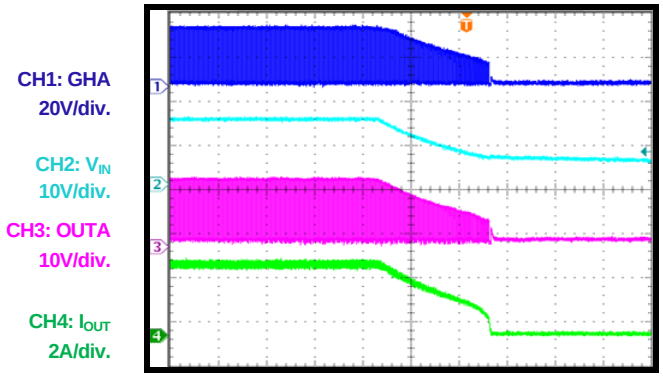
20μs/div.

Start-Up through VIN
20kHz, 50% duty cycle



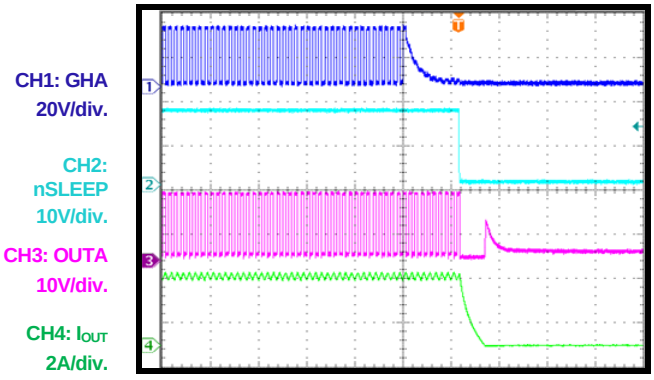
4ms/div.

Shutdown through VIN
20kHz, 50% duty cycle



4ms/div.

Sleep Mode Entry
20kHz, 50% duty cycle



400μs/div.

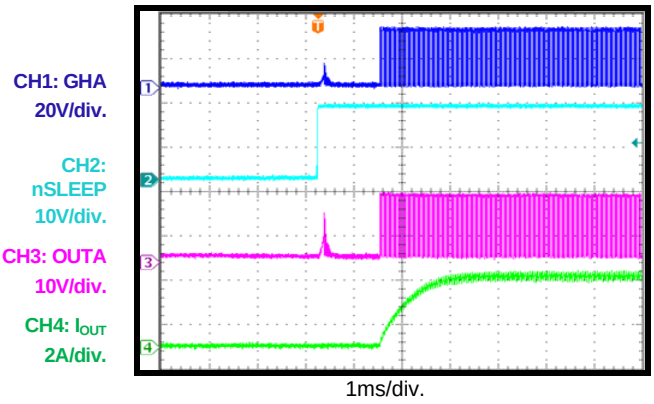
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 14V, T_A = 25°C, resistor + inductor load: R = 2Ω, L = 700μH, unless otherwise noted.

Sleep Mode Exit

20kHz, 50% duty cycle



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FUNCTIONAL BLOCK DIAGRAM

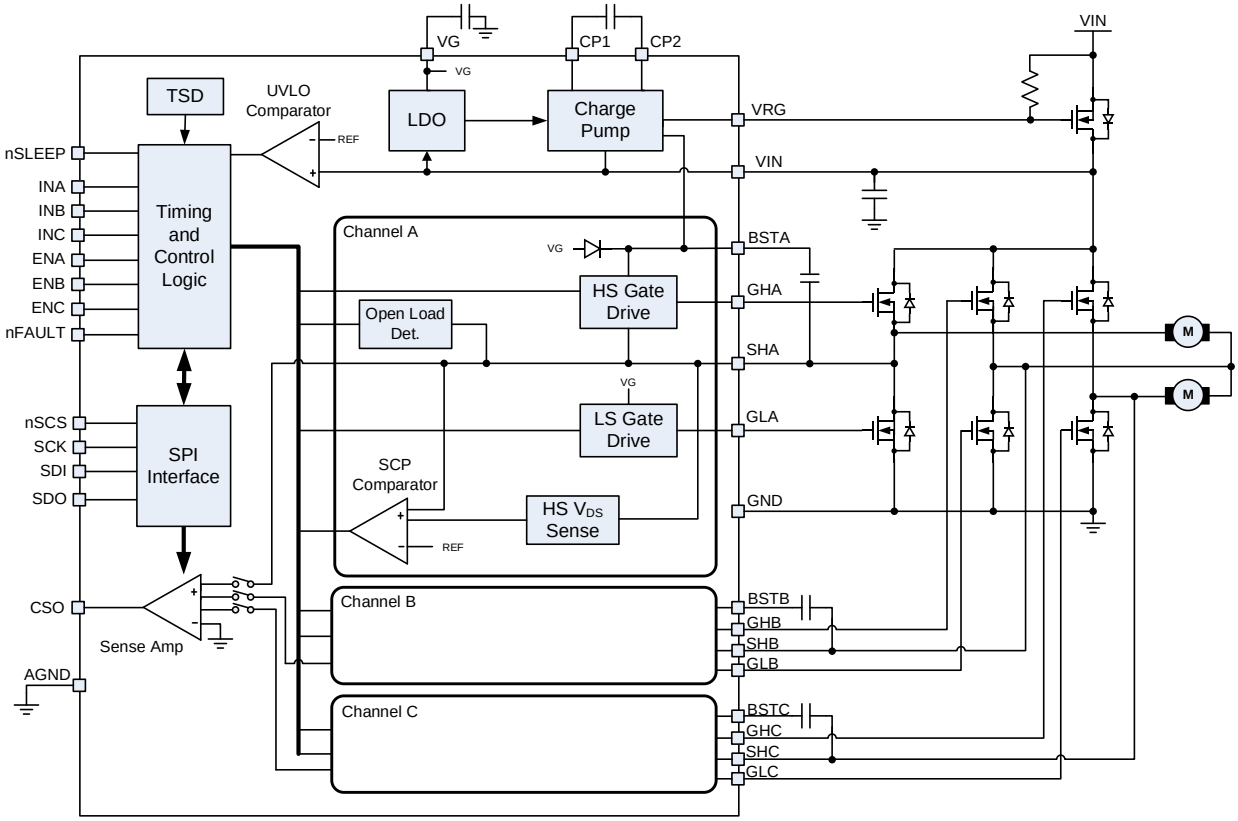


Figure 2: Functional Block Diagram

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OPERATION

The MPQ6533 is a three-channel motor pre-driver that can drive six N-channel MOSFETs with a 0.8A source and 1A sink current capability. The device can operate up to 40V. The MPQ6533 is typically used to drive DC motors or other loads in automotive applications.

Start-Up Sequence

To initiate the start-up sequence, V_{IN} must be above its under-voltage lockout (UVLO) threshold, and the VG voltage (V_G) must be above its UVLO threshold.

After V_{IN} and V_G are valid, the MPQ6533 sequentially turns on each LS-FET in succession to charge the bootstrap capacitors.

The start-up sequence takes between 1ms and 2ms. After this sequence, the MPQ6533 responds to logic inputs and drives the outputs.

If V_{IN} or V_G drop below their UVLO thresholds, the start-up sequence is re-initiated.

Sleep Mode

Driving the nSLEEP pin low forces the device into a low-power sleep state. In this state, all the internal circuits are disabled, including the reverse battery protection charge pump. All inputs are ignored when nSLEEP is active low. When the device wakes up from sleep mode, wait 1ms before issuing a PWM command. This allows the internal circuitry to stabilize.

Input Logic

The MPQ6533 may be controlled by using the input pins (ENx and INx), writing to the BENx and BINx bits in the OUT register via the SPI, or a combination of both methods.

The enable function uses the level on the input pins, or it works with the state of the corresponding register bits in the OUT register. This allows enable control to be accomplished with either the SPI or the ENx and INx pins. Additionally, set the BENx or BINx bit to 1 to invert the input state.

The ENx pin or BENx bit enables the gate drive outputs of each channel. When both the pin and bit are the same level (both low or high), the gate drive outputs are disabled, and the INx pin and the BINx bit on that channel are ignored.

When enabled, and the INx input pin and BINx bit are recognized. Table 1 shows the logic truth table.

Table 1: Input Logic Truth Table

ENx	BENx	INx	BINx	SHx
Low	Low	-	-	Hi-Z
Low	High	Low	Low	Ground
Low	High	Low	High	V_{IN}
Low	High	High	Low	V_{IN}
Low	High	High	High	Ground
High	Low	Low	Low	Ground
High	Low	L	High	V_{IN}
High	Low	High	Low	V_{IN}
High	Low	High	High	Ground
High	High	-	-	Hi-Z

To control the MPQ6533 using only the SPI, connect the INx and ENx pins to ground. Then the BENx bit enables the output, and the BINx bit controls the device, even if the output is high or low.

Gate Drive Voltage Regulator

To generate a voltage to drive the external MOSFET gates, a linear regulator is integrated into the MPQ6533. This voltage is supplied to the VG pin.

A 10µF ceramic capacitor must be connected from the VG pin to ground.

Charge Pump and Bootstrap

Generally, the high-side gate drive voltage is generated from bootstrap capacitors that are connected between the SHx and BSTx pins. When the low-side MOSFET (LS-FET) turns on, the bootstrap capacitor is charged.

If the output is held in a high state for a long period of time, the bootstrap capacitor slowly discharges. This results in a gate drive loss for the high-side MOSFET (HS-FET).

The bootstrap voltage (V_{BST}) is monitored by an under-voltage detection circuit. If any of the bootstrap voltages fall below their UVLO threshold, the part initiates a new start-up sequence.

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Reverse Battery Protection Charge Pump

An internal charge pump generates a voltage on the VRG pin that is about 12V above the voltage supplied to VIN. This voltage drives the gate of an external N-channel MOSFET to provide reverse battery protection (see Figure 1 on page 10).

A resistor must be connected between the gate and source of the external MOSFET to maintain the reverse battery conditions. A 100kΩ resistor is recommended.

The charge pump uses an external capacitor connected between the CP1 and CP2 pins. It is recommended to use a 0.22μF ceramic capacitor.

The charge pump is disabled during the initial start-up sequence, and when the MPQ6533 is in sleep mode. In these scenarios, the input current flows through the MOSFET body diode.

After start-up, the charge pump is enabled by writing 1 to the ENVRG bit in the FAULT register. Note that this register bit is toggled each time it is set to 1, and writing a 0 to this bit has no effect. If the ENVRG bit is set to 1, the charge pump is enabled.

Dead Time Adjustment

To prevent shoot through (simultaneous conduction through the high-side and low-side MOSFETs), a dead time (t_{DEAD}) is inserted between the HS-FET turn-off period and LS-FET turn-on period, and vice versa.

The dead time for all three channels is set by the xDT2~xDT0 bits in the CTRLA, CTRLB, and CTRLC registers (for channels A, B, and C, respectively). Table 2 lists the dead time configurations.

Table 2: Dead Time Adjustment

xDT2	xDT1	xDT0	Dead Time
0	0	0	50ns
0	0	1	100ns
0	1	0	200ns
0	1	1	400ns
1	0	0	800ns
1	0	1	1.6μs
1	1	0	3.2μs
1	1	1	6.4μs

Slew Rate Adjustment

To minimize EMI, the output slew rate can be controlled by changing the resistance of the gate drive's pull-up and pull-down switches. This resistance, and the resulting slew rate, are set by the xSR1~xSR0 bits in the CTRLx registers. Table 3 shows the gate drive resistance.

Table 3: Slew Rate Adjustment

xSR1	xSR0	Pull-Up Resistance	Pull-Down Resistance
0	0	200Ω	100Ω
0	1	100Ω	50Ω
1	0	50Ω	20Ω
1	1	10Ω	5Ω

When one MOSFET turns on, the other MOSFET remains off with a strong Miller clamp to prevent any parasitic turn-on caused by the gate-drain capacitance.

Current-Sense Amplifiers

An integrated current-sense amplifier amplifies the voltage present across the LS-FETs when they are turned on. This voltage is output to the CSO pin. The MUX1~MUX0 bits in the CTRLD register select which of the three channels are measured and output to the CSO pin (see Table 4).

Table 4: CSO MUX Settings

MUX1	MUX0	Channel
0	0	A
0	1	B
1	0	C
1	1	None

The current-sense amplifier is only active when the LS-FET is turned on.

The current-sense amplifier gain for each channel can be configured by writing to the xGN2~xGN0 bits in the CTRLx registers. Table 5 defines the gain.

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Table 5: Current-Sense Amplifier Gain

xGN2	xGN1	xGN0	Amplifier Gain
0	0	0	20
0	0	1	40
0	1	0	60
0	1	1	80
1	0	0	100
1	0	1	150
1	1	0	200
1	1	1	250

nFAULT

The nFAULT pin reports if a fault, such as over-current protection (OCP) or over-temperature protection (OTP), is detected. This pin is an open-drain output that is driven low when a fault condition occurs. If the fault condition is cleared, the nFAULT pin is pulled high by an external pull-up resistor.

Short-Circuit Protection (SCP)

To protect the MPQ6533 from excessive currents thought the MOSFETs due to a short circuit, the voltage across each MOSFET (V_{DS}) is monitored when the MOSFET turns on.

If the voltage across an HS-FET exceeds V_{SCP}, a short to ground condition is recognized, and the corresponding SCHx bit in the FAULT register is set.

If the voltage across an LS-FET exceeds V_{SCP}, a short to supply condition is recognized, and the SCLx bit in the FAULT register is set.

Short-circuit protection (SCP) can be disabled or enabled using the ENSCx bits in the CTRLx registers.

V_{SCP} can be adjusted using the xCS2~xCS0 bits in the CTRLD register for each channel. Table 6 shows the short-circuit thresholds for the low-side MOSFET (LS-FET).

Table 6: Short-Circuit Thresholds for the LS-FET

xSC2	xSC1	xSC0	V_{SCP}
0	0	0	110mV
0	0	1	210mV
0	1	0	310mV
0	1	1	410mV
1	0	0	510mV
1	0	1	610mV
1	1	0	710mV
1	1	1	810mV

Table 7 shows the short-circuit thresholds for the high-side MOSFET (HS-FET).

Table 7: Short-Circuit Thresholds for the HS-FET

xSC2	xSC1	xSC0	V_{SCP}
0	0	0	120mV
0	0	1	220mV
0	1	0	320mV
0	1	1	420mV
1	0	0	520mV
1	0	1	620mV
1	1	0	720mV
1	1	1	820mV

It takes a MOSFET time to fully turn on. To prevent the device from falsely detecting a short-circuit condition, an adjustable blanking time is used from when switching starts until the VDS voltage is measured. This time is controlled by the xBT2~xBT0 bits in the CTRLx registers (see Table 8).

Table 8: Blanking Time

xBT2	xBT1	xBT0	Blanking Time
0	0	0	1µs
0	0	1	2µs
0	1	0	5µs
0	1	1	10µs
1	0	0	25µs
1	0	1	100µs
1	1	0	500µs
1	1	1	1ms

If a short circuit occurs, the FAULT bit is set, and the nFAULT pin is driven active low. The OCLx or OCHx bit is set. The bit is not cleared until it is set to 0.

If the OCMD bit in the FAULT register is set to 0, then the channel is automatically re-enabled after a delay of about 1ms. If the OCMD bit is set to 1, the channel remains latched off until the corresponding OCHx or OCLx bit is cleared.

Open and Short Load Detection

The MPQ6533 integrates a circuit to detect open loads, and shorts to ground or VIN. Figure 3 shows the detection circuit.

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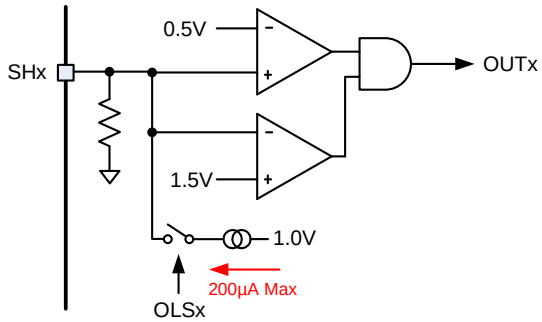


Figure 3: Open/Short Load Detection

To detect shorts to the ground or supply, all three outputs are first disabled (ENx = 0). Then a limited current voltage source (1V) is enabled on one output by setting the corresponding OLSx bit in the OUTPUT register to 1.

By reading the corresponding OUTx bit in the OUT register, it can be determined if the output is shorted to ground or VIN. If there is no short, the driven output is weakly biased to 1V, and the OUTx bit is set to 1.

If there is a load connected between two of the outputs, the OUTx bit that corresponds to the other side of the load is set to 1, since it is biased to 1V through the connected load. If there is no load, or if the load is open, the OUTx bit is read as 0, since it is pulled to ground through a weak pull-down resistor.

If a load is connected from an output directly to VIN or ground after setting the OLSx bit, the corresponding OUTx bit is read as 0 unless the load is open.

Input Under-Voltage Warning and Lockout

If the voltage on the VIN pin (V_{IN}) falls below the under-voltage warning threshold, the UVWARN bit in the FAULT register is set, and the nFAULT pin is driven active low.

If V_{IN} falls below its UVLO threshold, all circuitry in the device is disabled, and the internal logic is reset. Operation resumes when V_{IN} rises above the UVLO threshold.

VG and Bootstrap Under-Voltage Conditions

If the voltage on the VG pin falls below the VG UVLO threshold, the VGUV bit in the FAULT2 register is set, and nFAULT is driven low.

If any of the three bootstrap supplies fall below the BSTUV threshold, the corresponding BSUVx bit in the FAULT2 register is set, and nFAULT is driven active low. Then the part initiates a bootstrap refresh cycle (see the Start-Up Sequence section on page 11).

Thermal Shutdown and Warning

If the die temperature exceeds its safe limits, the MPQ6533 enters fault state. The OTS and FAULT bits are set, and the nFAULT pin is driven active low. The device remains disabled until the temperature has fallen to a safe level, and 0 is written to the OTS bit.

If the die temperature exceeds the over-temperature warning threshold, the OTW bit in the FAULT register is set. The bit remains set until the temperature falls below the OTW threshold.

Serial Peripheral Interface (SPI)

The SPI configures the MPQ6533's parameters, and reads status and fault information.

The SPI uses a standard 16-bit serial data packet, composed of 3 address bits, one read/write bit (1 = write, 0 = read), and 12 data bits.

Serial data is clocked in to the SDI pin by the rising edges on the SCK pin, while the nSCS pin is held active low. SDO is driven to a value according to the last SDI while nSCS is active low. SDO has a high impedance when nSCS is high.

The first 3 bits that are sent are the address bits, which address one of the registers inside the MPQ6533. These bits select both the source of data to be shifted out the SDO pin, as well as the destination of the new data.

Figure 4 shows the SPI serial interface logic diagram.

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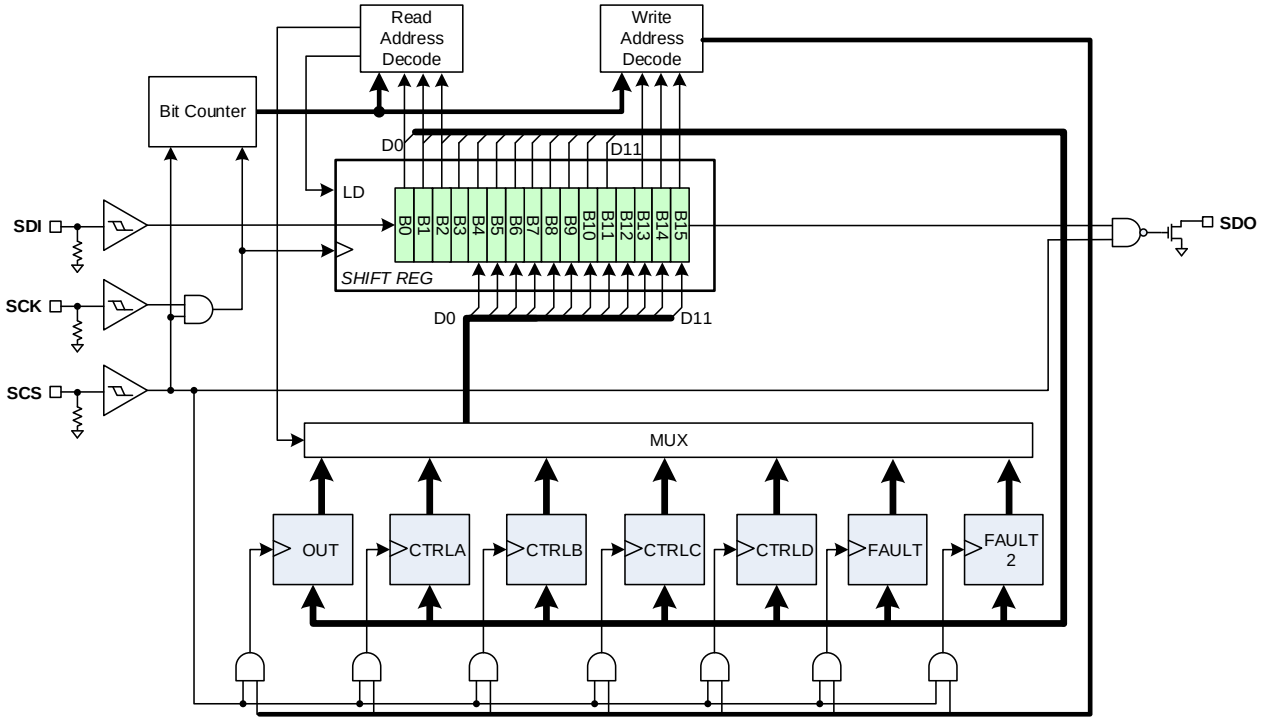


Figure 4: SPI Serial Interface Logic

Figure 5 shows the waveform for SPI data transfers.

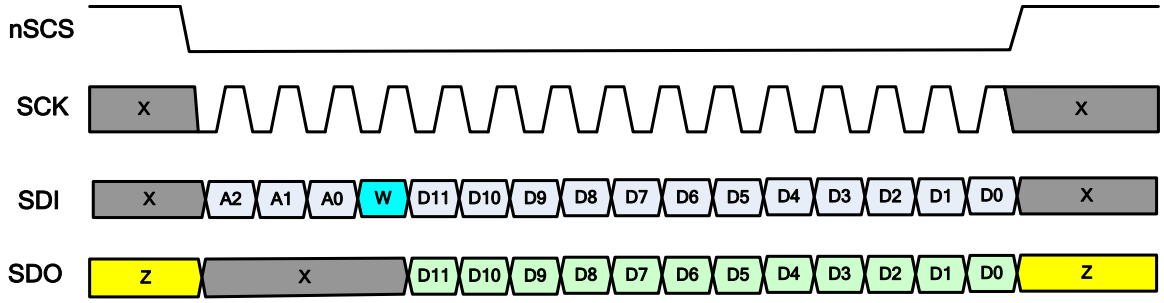


Figure 5: SPI Timing

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DIAGNOSTIC AND FAULT SUMMARY TABLE

Fault	Device Action	Bits Set	Bits Cleared By	nFAULT Active
Short circuit	If OCMD = 1, the output with the over-current condition latches off	SCxx, FAULT	Write 1 to SCxx	Until SCxx is cleared
	If OCMD = 0, the output with the over-current condition turns off for 1ms before being re-enabled	SCxx, FAULT	Write 1 to SCxx	Until SCxx is cleared
V_{IN} under-voltage warning	N/A	UVW, FAULT	Write 1 to UVW	Until UVW is cleared
V_{IN} under-voltage shutdown	Outputs are disabled until V_{IN} exceeds the under-voltage lockout (UVLO) threshold.	UVLO, FAULT	Write 1 to UVLO	Until UVLO is cleared
Thermal shutdown	The output latches off, and stepping is disabled	TSD, FAULT	Write 1 to TSD	Until TSD is cleared
Over-temperature warning	N/A	OTW	The temperature falls below T_{OTW}	Never
VG under-voltage	Bootstrap refresh	VGUV, FAULT	Write 1 to VGUV	Until VGUV is cleared
VBST under-voltage	Bootstrap refresh	BSUVx, FAULT	Write 1 to BSUVx	Until BSUVx is cleared

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REGISTER DESCRIPTIONS

OUT

Address: 0x00

Bit	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	OUTC	OUTB	OUTA	OLSC	OLSB	OLSA	BINC	BENC	BINB	BENB	BINA	BENA
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0	0	0	0	0

BENx: Enables SPI control to enable for the corresponding channel. XOR'd with the ENx pin value.
BINx: Enables SPI control for the input of the corresponding channel. XOR'd with the INx pin value.
OLSx: Enables open load detection for the voltage source on the respective channel.
OUTx: Indicates an open load condition on the corresponding output. This bit is set to 1 if VOUT is between 0.5V and 1.5V.

CTRLA

Address: 0x01

Bit	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ENSCA	AGN2	AGN1	AGN0	ABT2	ABT1	ABT0	ADT2	ADT1	ADT0	ASR1	ASR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	1	1	1	0	0

ASR1~ASR0: Adjusts the channel A slew rate.
ADT2~ADT0: Adjusts the channel A dead time.
ABT2~ABT0: Adjusts the channel A blanking time.
AGN1~AGN0: Sets the channel A current-sense amplifier gain.
ENSCA: Enables short-circuit protection for channel A.

CTRLB

Address: 0x02

Bit	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ENSCB	BGN2	BGN1	BGN0	BBT2	BBT1	BBT0	BDT2	BDT1	BDT0	BSR1	BSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	1	1	1	0	0

BSR1~BSR0: Adjusts the channel B slew rate.
BDT2~BDT0: Adjusts the channel B dead time.
BBT2~BBT0: Adjusts the channel B blanking time.
BGN1~BGN0: Sets the channel B current-sense amplifier gain.
ENSCB: Enables short-circuit protection for channel B.

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CTRLC
Address: 0x03

Bit	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ENSCC	CGN2	CGN1	CGN0	CBT2	CBT1	CBT0	CDT2	CDT1	CDT0	CSR1	CSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	1	1	1	0	0

CSR1~CSR0: Adjusts the channel C slew rate.
CDT2~CDT0: Adjusts the channel C dead time.
CBT2~CBT0: Adjusts the channel C blanking time.
CGN1~CGN0: Sets the channel C current-sense amplifier gain.
ENSCC: Enables short-circuit protection for channel C.

CTRLD
Address: 0x04

Bit	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	CSC2	CSC1	CSC0	BSC2	BSC1	BSC0	ASC2	ASC1	ASC0	OCMD	MUX1	MUX0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0	0	0	0	0

MUX1~MUX0: Selects the CSO multiplexor, and sets which channel is sensed and outputted to the CSO pin.
ASC2~ASC0: Sets the short-circuit threshold for channel A.
BSC2~BSC0: Sets the short-circuit threshold for channel B.
CSC2~CSC0: Sets the short-circuit threshold for channel C.
OCMD: Sets the over-current protection (OCP) mode. If this bit is set to 1, the device latches off. If this bit is set to 0, the MPQ6533 automatically tries to restart.

FAULT
Address: 0x05

Bit	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ENVRG	OTW	UVLO	UVW	SCHC	SCHB	SCHA	SCLC	SCLB	SCLA	OTS	FAULT
R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Reset Value	0	0	0	0	0	0	0	0	0	0	0	0

FAULT: Logical ‘OR’ of other fault bits.
OTS: This bit is set to 1 if over-temperature shutdown has occurred.
SCLx: This bit is set to 1 if a low-side short circuit occurs on the respective channel.
SCHx: This bit is set to 1 if a high-side short circuit occurs on the respective channel.
UVW: Indicates if there is an under-voltage warning.
UVLO: Indicates if under-voltage lockout (UVLO) has occurred.
OTW: If this bit is set to 1, an over-temperature warning has been issued.
ENVRG: If this bit is set to 1, the charge pump is enabled. Write 1 to ENVRG to toggle this bit.

Write a 1 to the bits in the FAULT register to clear them. Writing a 0 to these bits has no effect.

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FAULT2
Address: 0x06

Bit	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	-	BSUVA	BSUVB	BSUVC	VGUV
R/W	-	-	-	-	-	-	-	-	R/W	R/W	R/W	R
Reset Value	-	-	-	-	-	-	-	-	0	0	0	0

VGUV: If this bit is set to 1, there is an under-voltage condition on the VG pin.
BSUVC: This bit is set to 1 if channel C's bootstrap falls below the under-voltage threshold.
BSUVB: This bit is set to 1 if channel B's bootstrap falls below the under-voltage threshold.
BSUVA: This bit is set to 1 if channel A's bootstrap falls below the under-voltage threshold.

Write a 1 to the bits in the FAULT2 register to clear them. Writing a 0 to these bits has no effect.

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APPLICATION INFORMATION

VIN Input Voltage

The VIN pin supplies all power to the device. VIN must be properly bypassed with a capacitor connected to ground.

The normal operating range for V_{IN} is between 6V and 40V.

To protect the device, V_{IN} should never exceed the absolute maximum ratings, even for short-term transient conditions. In scenarios where mechanical energy can turn a motor into a generator, it is recommended to use additional over-voltage protection, such as a TVS diode placed between VIN and ground.

Reverse Battery Protection

The MPQ6533 integrates a charge pump that can be used to implement reverse battery protection using an external N-channel MOSFET. Note that a gate-to-source resistor is required to ensure that the MOSFET stays off during reverse battery conditions.

COMPONENT SELECTION

Selecting the MOSFET

It is crucial to select the correct power MOSFETs to drive the motor.

First, the MOSFET must have a V_{DS} breakdown voltage that exceeds the supply voltage. It is recommended to add a 10V to 15V margin to prevent the MOSFET from being damaged by transient voltages, which are caused by parasitic inductance in the PCB layout and wiring.

For example, for a 24V power supply application, it is recommended for the MOSFET to have a 40V to 60V breakdown voltage. High-current applications should have a higher margin since the transients caused by the parasitic inductance may be larger. Conditions such as regenerative braking can inject current back into the power supply. Ensure that these conditions do not force the power supply voltage high enough that it damages components.

The MOSFETs must be able to safely handle the current required to run the motor. The highest current condition, which is normally when the motor is first started or stalled, must be supported by the MOSFET. This high current is called the stall current.

Also consider the on resistance ($R_{DS(ON)}$) This is the MOSFET's resistance when it is fully on. The MOSFET dissipates power (P) that is proportional to $R_{DS(ON)}$ and the motor current. P can be calculated with Equation (1):

$$P = I^2 \times R \quad (1)$$

Select $R_{DS(ON)}$ such that the heat generated by the power can be safely dissipated. In some cases, this may require special PCB design considerations and external heatsinks for the MOSFETs.

Consider the safe operating area (SOA) of the MOSFETs under fault conditions, such as a short circuit. The MPQ6533 acts quickly in the event of a short condition, but there is still a very short time (about 3µs) during which large currents can flow in the MOSFETs while the protection circuits recognize the fault and disable the outputs.

Selecting the External Capacitor

Connect the charge pump flying capacitor (C_{CP}) to the CP1 and CP2 pins. C_{CP} should have a capacitance of 220nF, and it must be rated to withstand the maximum V_{IN} power supply voltage. A X7R or X5R ceramic capacitor is recommended.

Use bootstrap capacitors to provide the large peak currents required to turn on the HS-FET. These capacitors are charged when the output is driven low. The charge in the bootstrap capacitor turns on the HS-FET when the output is driven high. Note that an internal charge pump keeps the bootstrap capacitor charged when the output is held high for an extended period.

The bootstrap capacitors are selected depending on the MOSFET's total gate charge. When the HS-FET turns on, the charge stored in the bootstrap capacitor is transferred to the HS-FET's gate. As a simplified approximation, the minimum bootstrap capacitance can be estimated as $C_{BOOT} > 8 \times Q_G$, where Q_G is the total gate charge of the MOSFET (in nC), and C_{BOOT} is in nF. The bootstrap capacitors should

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not exceed 1µF, or the MPQ6533 may not start up properly.

For most applications, it is recommended to use ceramic bootstrap capacitors with X5R or X7R dielectrics. They should be between 0.1µF and 1µF, and rated for at least 25V.

The VREG pin is the output of the gate drive's voltage regulator. Connect a 10µF bypass capacitor from VREG to ground. It is recommended to use a X7R or X5R ceramic capacitor rated for at least 16V.

Connect a bypass capacitor from VIN to ground, and place it as close as possible to the device. It is recommended to use a minimum 0.1µF ceramic capacitor with X5R or X7R dielectrics. The capacitor should be rated for the VIN voltage.

Depending on the power supply impedance, the distance between the MOSFETs, and the power supply, additional bulk capacitance may be required. Generally, low-ESR electrolytic capacitors between 47µF and 470µF are recommended.

GATE DRIVE CONSIDERATIONS

The gate characteristics of the selected MOSFETs affect how quickly the MOSFETs switch on and off. The gate drive outputs of the device should be connected directly to the gates of the power MOSFETs.

Slew Rate Selection

The strength of the gate drive outputs can be set by the xSR bits in the CTRLx registers. A fast slew rate reduces switching loss but may result in more EMI. This tradeoff is also affected by the external MOSFET, which means that the slew rate must be optimized via experiments.

Figure 6 shows the LS-FET and HS-FET gates, as well as the phase node (output) with the fastest slew rate setting and minimum gate drive resistance. Note the scale of 100ns/div. The gates transition quickly, so the rising time on the phase node is fast.

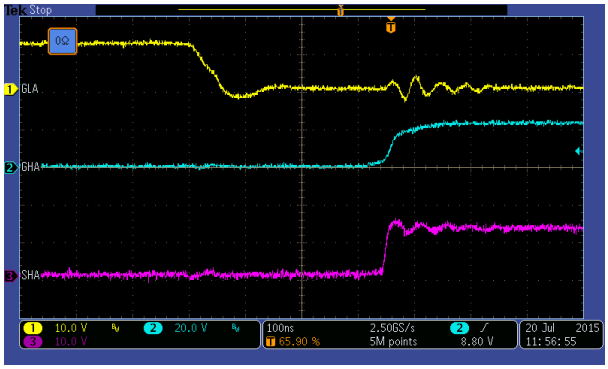


Figure 6: LS-FET and HS-FET Gates

Figure 7 shows when the slew rate is set such that the gate drive resistance is 100Ω. The rising time on the phase node is slowed significantly. Note the scale of 200ns/div.

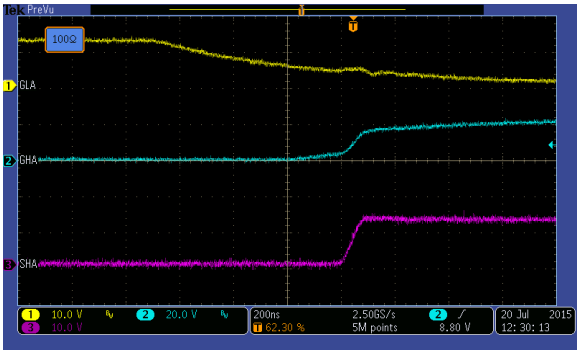


Figure 7: 100Ω Gate Drive Resistance

Dead Time Selection

During the transition between driving an output low and high, there is a short period when neither the HS-FET nor LS-FET turn on. This is called dead time. The dead time prevents the HS-FET and LS-FET from being on simultaneously, which could result in a short-circuit condition between the power supply and ground. This short condition, called shoot through, can cause large transient currents and damage the MOSFETs.

Since motors are inductive by nature, the motor cannot stop immediately after current stops flowing, even if the MOSFETs are turned off. This recirculation current continues to flow in its original direction until the magnetic field has decayed. When the MOSFETs are turned off, this current flows through the MOSFET's integrated body diode.

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MOSFET body diodes have a much higher voltage drop than the MOSFET has during conduction, so more power dissipates during body diode conduction than during the on time. Minimize the dead time while ensuring it is long enough to guarantee that the HS-FET and LS-FET are never on at the same time.

The dead time is selected by the xDT bits in the CTRLx registers. It is recommended to set the dead time to about 1µs. If faster switching or a high PWM frequency (exceeding 30kHz) is used, a shorter dead time may be required.

Figure 8 shows a 300ns dead time between when the LS-FET gate turns off and the HS-FET gate turns on.

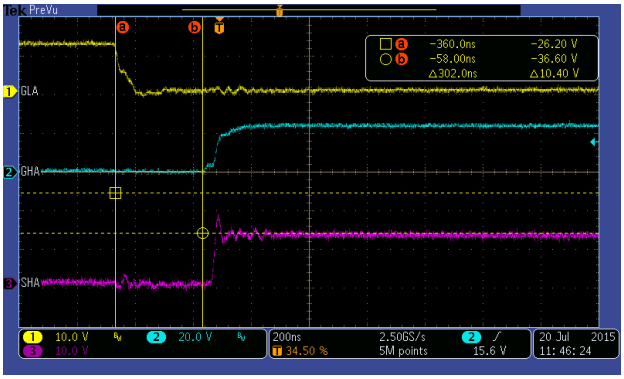


Figure 8: 200ns Dead Time

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PCB Layout Guidelines

Proper PCB layout is critical for MOSFET gate driver performance. In particular, the connection between the HS-FET source and LS-FET drain must be as direct as possible to avoid negative undershoot on the phase node due to parasitic inductance. The MPQ6533 is designed to accommodate a negative undershoot, but an excessive undershoot can damage the device.

Using Surface-Mounted, Dual N-Channel MOSFETs

The first example for the PCB layout uses surface-mounted, dual N-channel MOSFETs, which allows for a short connection between the HS-FET and LS-FET. For the best results, refer to Figure 9 and follow the guidelines below:

1. Use wide copper areas for the high-current paths.
2. Place the charge pump and supply bypass capacitors (C5, C6, and C8) close to the IC.
3. The grounded side of these capacitors (C5, C6, and C8) should be connected to a ground plane, which is connected to the device's ground pin and exposed pad.

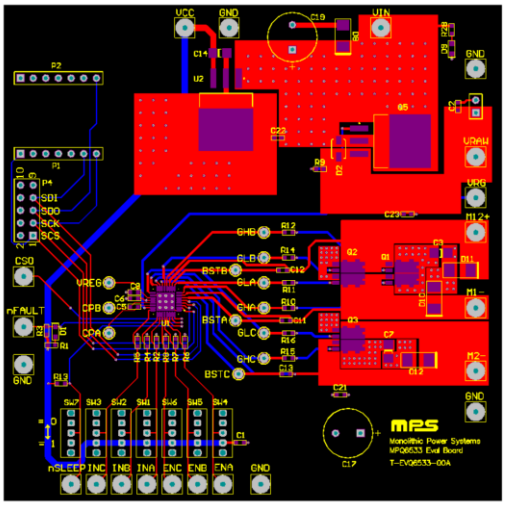


Figure 9: Recommended PCB Layout with Dual N-Channel MOSFETs

Using a Power Plane

A second example for the PCB layout uses a power plane. Four layers are used to provide solid planes for the ground and supply voltage. For the best results, refer to Figure 10 and Figure 11, and follow the guidelines below:

1. Route VIN on the right portion of the plane, and connect it to the MOSFET's input power and bulk capacitors (C17 and C19). The left portion of the plane is used as a redundant ground plane (see Figure 10).

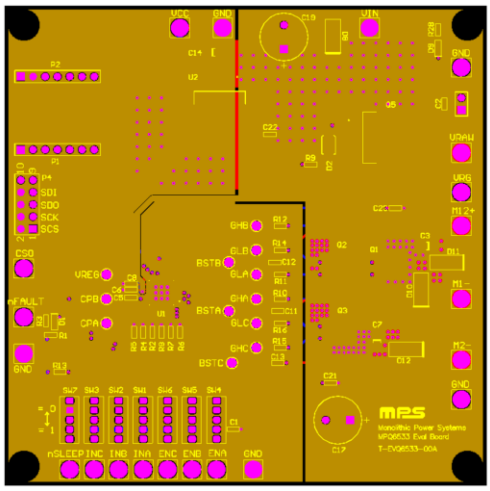


Figure 10: Recommended PCB Layout with a Power Plane

2. Use a split solid ground plane for the high-current path between the bulk capacitors.
3. Route the MOSFETs away from the rest of the circuitry. The two planes meet underneath the MPQ6533 (see Figure 11).

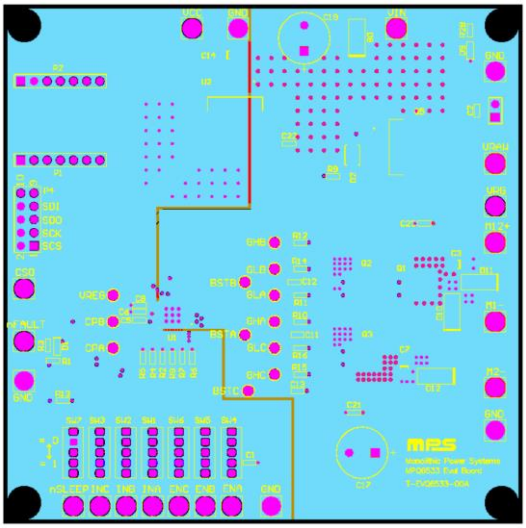


Figure 11: Recommended PCB Layout with a Power Plane

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TYPICAL APPLICATION CIRCUIT

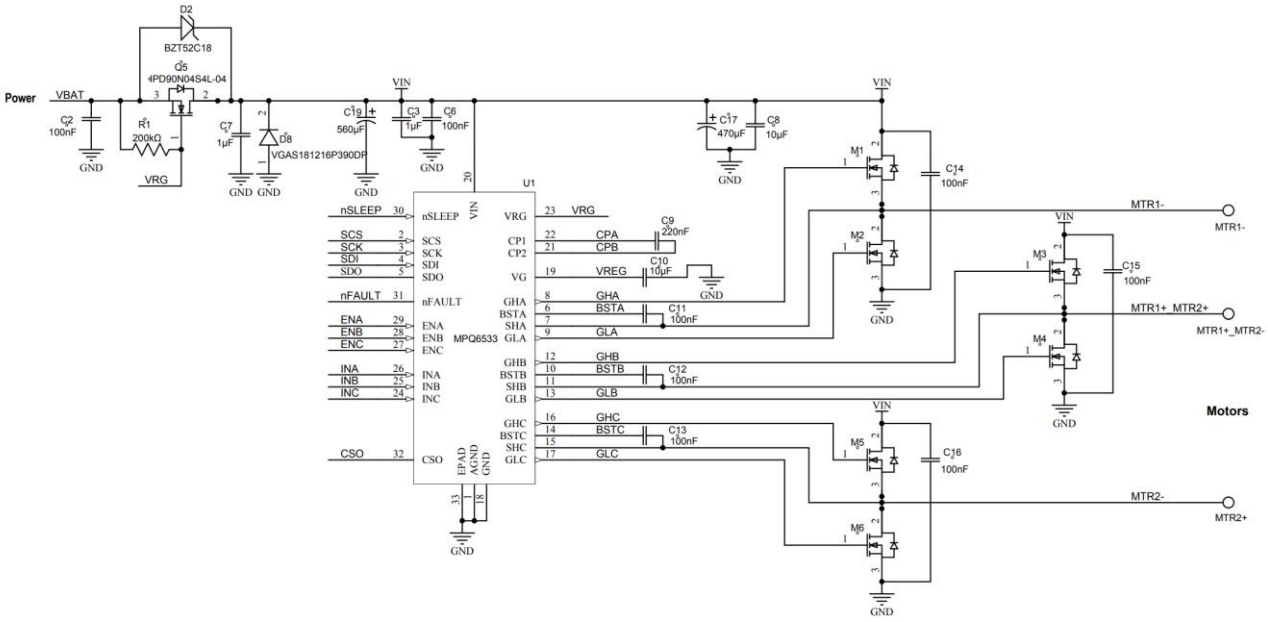
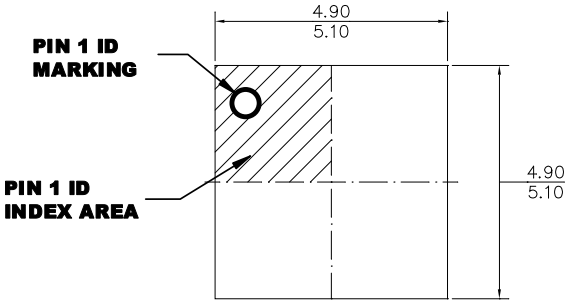


Figure 12: Typical Application Circuit

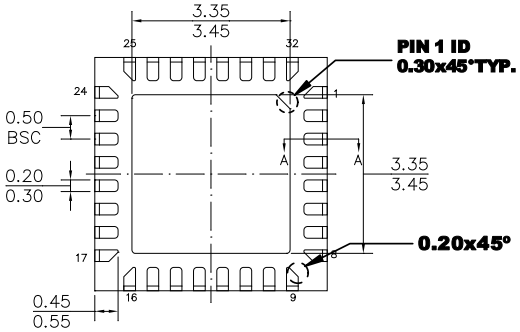
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PACKAGE INFORMATION

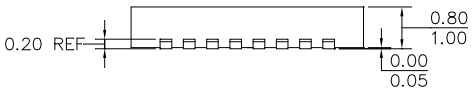
QFN-32 (5mmx5mm)



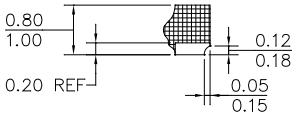
TOP VIEW



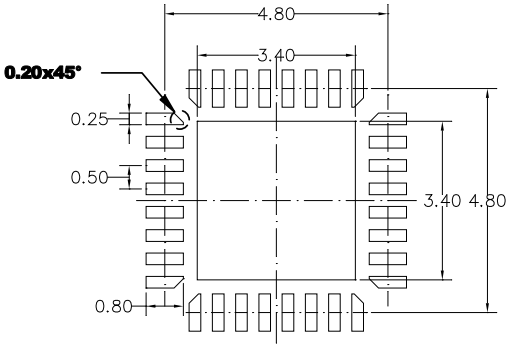
BOTTOM VIEW



SIDE VIEW



SECTION A-A



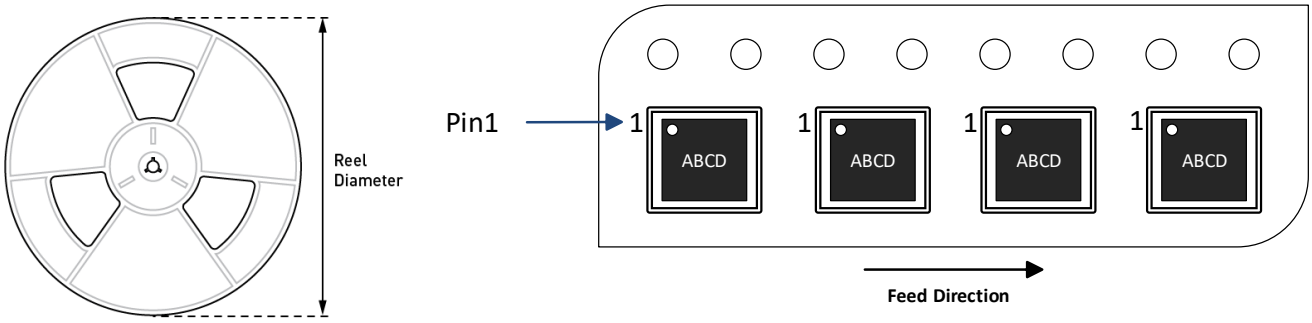
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) DRAWING REFERENCE TO JEDEC MO-220.
5) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ6533GUE-AEC1-Z	QFN-32 (5mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	08/25/2021	Initial Release	-

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Monolithic Power Systems (MPS):

MPQ6533GUE-AEC1-Z MPQ6533GUE-AEC1-P