Dual Mode Microphone with High SNR Digital Output (Bottom Port)

DESCRIPTION

The ZTS6872SE is a high quality, high performance, low power digital output bottom-ported omni-directional MEMS microphone. ZTS6872SE consists of a MEMS microphone element and an analog-to-digital converter. ZTS6872SE has a high SNR and flat wideband frequency response, resulting in natural sound with high intelligibility. Due to built-in filter, ZTS6872SE shows high immunity to EMI.

The ZTS6872SE is available in a thin 3.50mm × 2.65mm × 0.98mm surface-mount package. It is reflow solder compatible with no sensitivity degradation. The ZTS6872SE is Halogen and Lead free.

APPLICATIONS

- Mobile telephones
- PDAs
- Digital video cameras
- Portable media devices with audio input

ORDERING INFORMATION

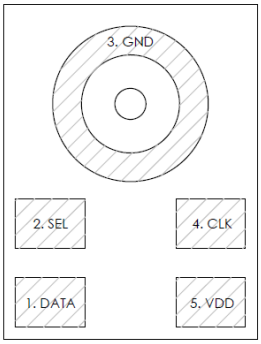
PART	RoHS	Ship, Quantity
ZTS6872SE	Yes	Tape and Reel, 5.2K

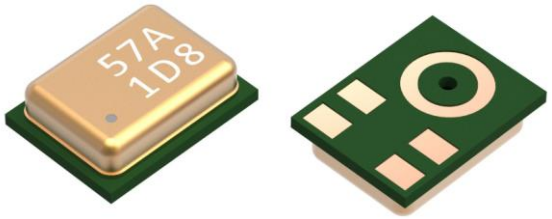
FEATURES

- 3.50mm×2.65mm×0.98mm surface-mount package
- Stable sensitivity over power supply range of 1.60V-3.60V
- SNR of 68 dB(A)
- Sensitivity of −26dB FS
- Multi Chip Module (MCM) Package

Pins Configuration and Description

Bottom View

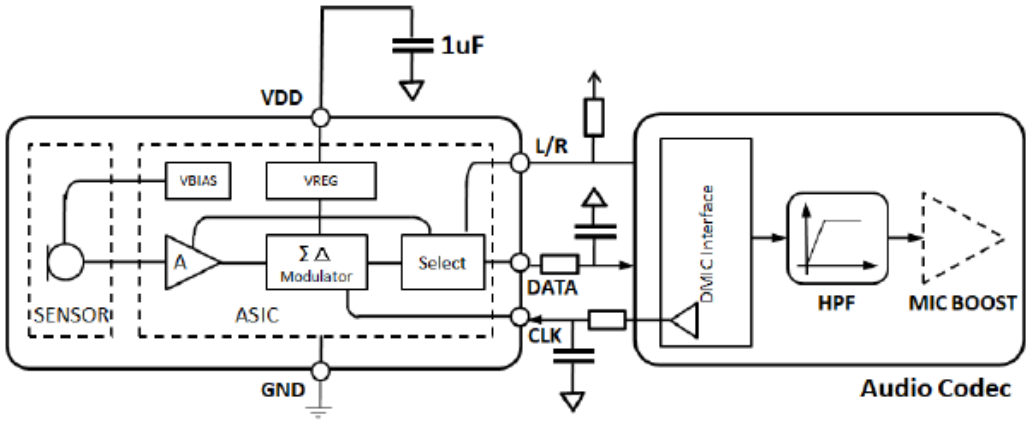




Top Bottom

Isometric Views of ZTS6872SE Microphone Package

Typical Applications



Label	Select	Drives Data After	High-Z After
Data_H	High	Rising Clock Edge	Falling Clock Edge
Data_L	Low (default)	Falling Clock Edge	Rising Clock Edge

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Absolute Maximum Ratings

CLOCK to Ground ..... –0.3V to +5.0V
SELECT, V_{DD}, DATA to Ground ..... –0.3V to +5.0V
Input Current ..... ±5mA
Data Output Short Circuit ..... Indefinite to Ground or V_{DD}
Operating Temperature Range ..... –40°C to +125°C
Storage Temperature Range ..... –40°C to +125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

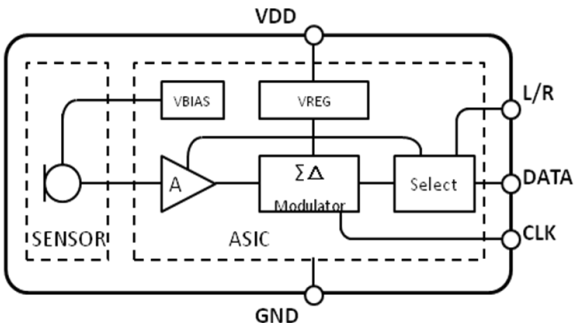
Electro-Static Discharge Sensitivity

This integrated circuit can be damaged by ESD. It is recommended that all integrated circuits be handled with proper precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure.

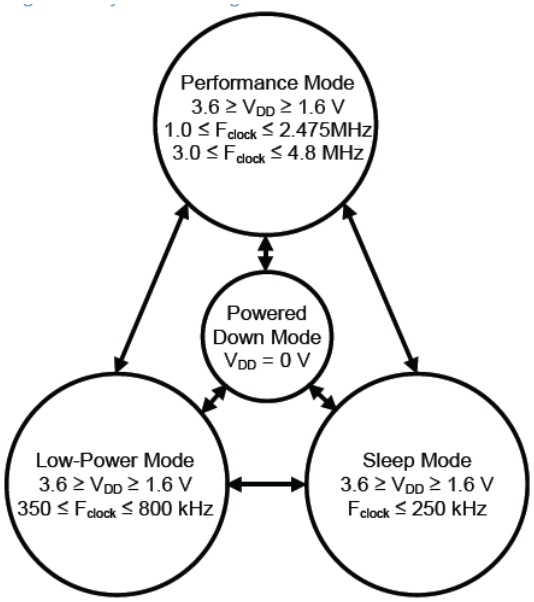
Pins Description

Pin	Symbol	Description
1	DATA	Output.
2	SELECT	Select.
3	GND	Ground
4	CLOCK	Clock.
5	VDD	Power Supply (V_{DD}).

Microphone Block Diagram



Microphone State Diagram



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Specifications

(TA = +23°C, VDD = +1.8V, fclock = 2.4MHz, R.H. = 60%~70%, no load, VDD Decoupling cap=1.0uF unless otherwise noted.)

PARAMETER	Symbol	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Supply Voltage (Note 1)	V_{DD}				1.60		3.60	V
Clock Frequency	Fclock				1		4.8	MHz
Current Consumption (Note 1,6)	I_{DD}					800	1000	µA
Standby Current (Sleep Mode) (Note 5,6)	$I_{STANDBY}$	f_{clock} < 250KHz				50		µA
Directivity					Omni-directional			
Sensitivity (Note 1)	S	94dB SPL @ 1KHz			−27	−26	−25	dB FS
Signal to Noise Ratio	SNR	94dB SPL @ 1KHz, A-weighted				68		dB(A)
Total Harmonic Distortion	THD	114dB SPL @ 1KHz					1	%
		120dB SPL @ 1KHz					10	%
Acoustic Overload Point	AOP	10% THD @ 1KHz				122		dBSPL
Power Supply Rejection Ratio	PSRR	1KHz, 200mV Vp-p, sine wave on V_{DD}	V_{DD} =1.8V			60		dB
			V_{DD} =3.3V			60		dB
Power Supply Rejection	PSR	217Hz, 100mV Vp-p, square wave on V_{DD}	V_{DD} =1.8V			-90		dB FS
			V_{DD} =3.3V			-90		
Polarity		Increasing sound pressure			Increasing density of 1's			
Fall-Asleep Time (Note 2,3)		V_{DD} = On, f_{clock} < 1KHz					10	ms
Wake-Up Time (Note 2,4)		V_{DD} = On, f_{clock} ≥ 1MHz					10	ms
Short Circuit Output Current	I_{SC}	Grounded output pin				1	10	mA
Output Load	C_{LOAD}						500	pF
Data Format					1/2 cycle PDM			
Clock Duty Cycle					40		60	%
Logic Input/Output Low	V_{IOL}	I_{out} = 1mA			−0.3		0.35×V_{DD}	V
Logic Input/Output High	V_{IOH}	I_{out} = 1mA			0.65×V_{DD}		V_{DD}+0.3	V
Delay Time for Valid Data	t_{dv}	CLK = 3.072MHz Oscilloscope: APx525 (probe Cin = 24pF)	Data Trans High	1.8V	30		180	ns
				3.3V	24		119	
			Data Tran Low	1.8V	30		180	
				3.3V	22		118	
Delay Time for High Z	t_{dz}	CLK = 3.072MHz, Oscilloscope: APx525 (probe Cin = 24pF)	Data Trans High	1.8V	1		14	ns
				3.3V	1		10	
			Data Trans Low	1.8V	1		14	
				3.3V	1		10	
Settling time	t_s			1.8V		13.5	25	ms
				3.3V				
Startup Time		Powered Down →Active Mode		1.8V		13.5	25	ms
				3.3V				

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(TA = +23°C, VDD = +1.8V, fclock = 768KHz, R.H. = 60%~70%, no load, VDD Decoupling cap=1.0uF unless otherwise noted.)

PARAMETER	Symbol	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Supply Voltage (Note 1)	V_{DD}				1.60		3.60	V
Clock Frequency	Fclock				350		800	KHz
Current Consumption (Note 1,6)	I_{DD}					300	400	µA
Standby Current (Sleep Mode) (Note 5,6)	$I_{STANDBY}$	f_{clock} < 250KHz				50		µA
Directivity					Omni-directional			
Sensitivity (Note 1)	S	94dB SPL @ 1KHz			−27	−26	−25	dB FS
Signal to Noise Ratio	SNR	94dB SPL @ 1KHz, A-weighted				68		dB(A)
Total Harmonic Distortion	THD	114dB SPL @ 1KHz					1	%
		120dB SPL @ 1KHz					10	%
Acoustic Overload Point	AOP	10% THD @ 1KHz				122		dBSPL
Power Supply Rejection Ratio	PSRR	1KHz, 200mV Vp-p, sine wave on V_{DD}	V_{DD} =1.8V			60		dB
			V_{DD} =3.3V			60		dB
Power Supply Rejection	PSR	217Hz, 100mV Vp-p, square wave on V_{DD}	V_{DD} =1.8V			-90		dB FS
			V_{DD} =3.3V			-90		
Polarity		Increasing sound pressure			Increasing density of 1's			
Fall-Asleep Time (Note 2,3)		V_{DD} = On, f_{clock} < 1KHz					10	ms
Wake-Up Time (Note 2,4)		V_{DD} = On, f_{clock} ≥ 1MHz					10	ms
Short Circuit Output Current	I_{SC}	Grounded output pin				1	10	mA
Output Load	C_{LOAD}						500	pF
Data Format					1/2 cycle PDM			
Clock Duty Cycle					40		60	%
Logic Input/Output Low	V_{IOL}	I_{out} = 1mA			−0.3		0.35×V_{DD}	V
Logic Input/Output High	V_{IOH}	I_{out} = 1mA			0.65×V_{DD}		V_{DD}+0.3	V
Delay Time for Valid Data	t_{dv}	CLK = 3.072MHz Oscilloscope: APx525 (probe Cin = 24pF)	Data Trans High	1.8V	30		180	ns
				3.3V	24		119	
			Data Tran Low	1.8V	30		180	
				3.3V	22		118	
Delay Time for High Z	t_{dz}	CLK = 3.072MHz, Oscilloscope: APx525 (probe Cin = 24pF)	Data Trans High	1.8V	1		14	ns
				3.3V	1		10	
			Data Trans Low	1.8V	1		14	
				3.3V	1		10	
Settling time	t_s			1.8V		13.5	25	ms
				3.3V				
Startup Time		Powered Down →Active Mode		1.8V		13.5	25	ms
				3.3V				

Note 1: 100% tested.
Note 2: Valid microphone states are: Power Down Mode (mic off), Sleep Mode (low current, no output, fast start-up), and Active Mode (normal operation).
Note 3: Time from f_{clock} < 1KHz to sleep current specification is met when transitioning from Active to Sleep Mode.
Note 4: Time from f_{clock} ≥ 1MHz to all applicable specifications when transitioning from Sleep to Active Mode.
Note 5: $\Delta I_{DD} = 0.5 \times V_{DD} \times C_{LOAD} \times f_{clock}$
Note 6: Specified max values are measured at V_{DD} = +3.6V.

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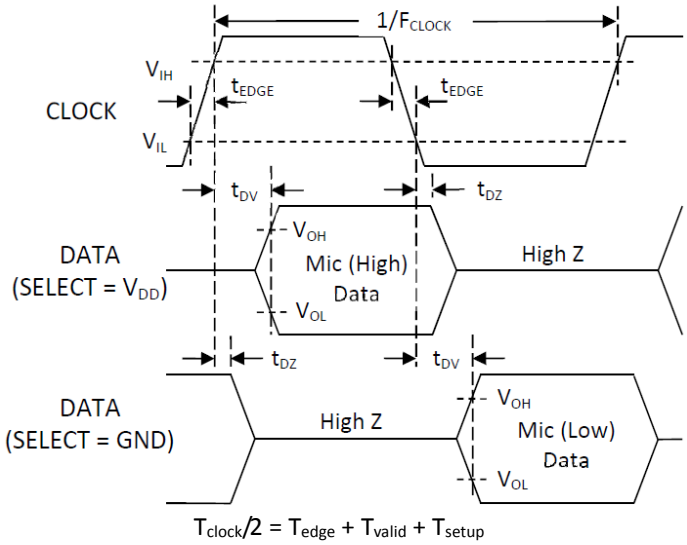
Timing Diagram



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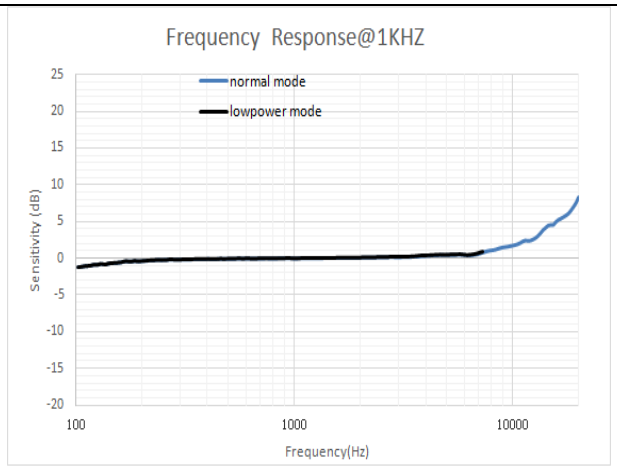
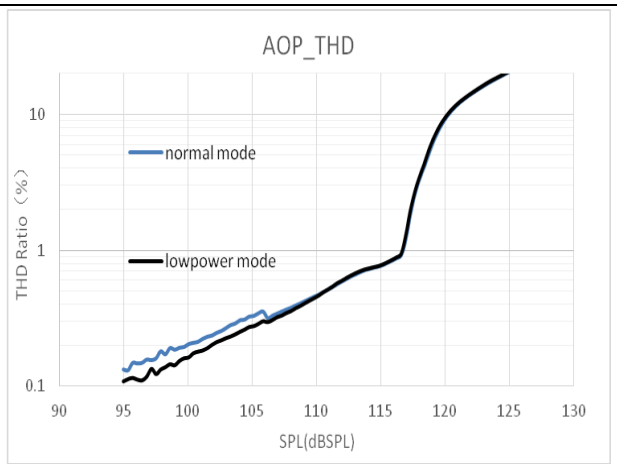
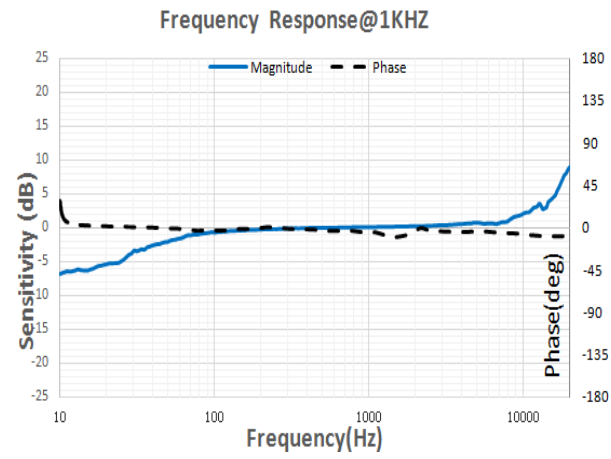
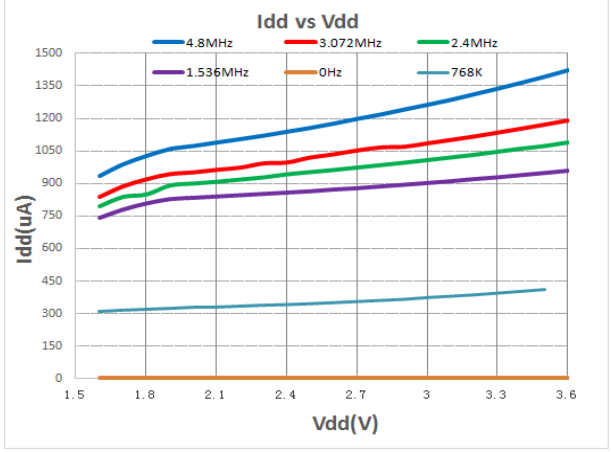
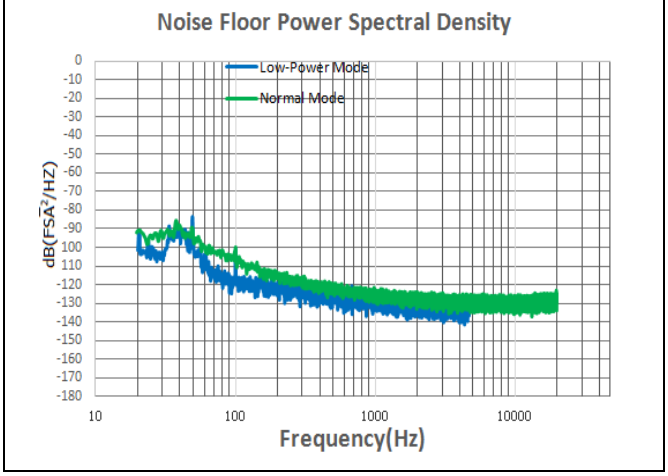
Typical Performance Characteristics











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Reliability Specifications

The microphone sensitivity after stress must deviate by no more than ±3dB from the initial value.

1. Heat Test, Operational	Temperature: 125±3 °C Duration: 1000 hours Voltage: Applied
2. Cold Test, Operational	Temperature: -40±3°C Duration: 1000 hours Voltage: Applied
3. Heat Test, Non-Operational	Temperature: 125±3°C Duration: 1000 hours Voltage: Not Applied
4. Cold Test, Non-Operational	Temperature: -40±3°C Duration:1000 hours Voltage: Not Applied
5. Thermal Shock Test, Non-Operational	Temperature: -40±3°C and 125±3°C Duration: 30 minutes each, during 5 minutes ramp, 256 cycles Voltage: Not applied
6. Temperature humidity storage	Temperature: 85±3°C Humidity: 85±3%RH Duration: 1000 hours
	Temperature: 65±3°C Humidity: 95±3%RH Duration: 168 hours
7. Free Fall Test 1.5m	Placed inside test fixture and dropped on concrete from height 1.5m. 4 times by each surface and corner
8. Vibration	4 cycles of 20 to 2000 Hz sinusoidal sweep with 20G peak acceleration lasting 12 minutes in X, Y, and Z directions
9. Mechanical Shock	5 pulses of 10000g in each of the ±X, ±Y, and ±Z directions
10. Electrostatic Discharge Test	Capacitance: 150pF Resistance: 330Ω Duration: 10 times Air Discharge: Level 4(+/-15kV) Direct contact discharge: Level 4 (+/-8kV)
11. Human Body Mode	±5000 Volt
12. Charged-Device Model	±500 Volt
13. Reflow	5 reflow cycles with peak temperature of 260℃
14. Solderability	245±5 °C ,5sec, 95% Tin on pad surface
15. Tumble test	300 tumbles from a height of 1m onto a steel base.
16. HAST	Temperature: 130±3°C Humidity: 85±3%RH Duration: 96 hours Voltage: Applied
17. Air Blow	0.45MPa, distance 3cm, time 10s

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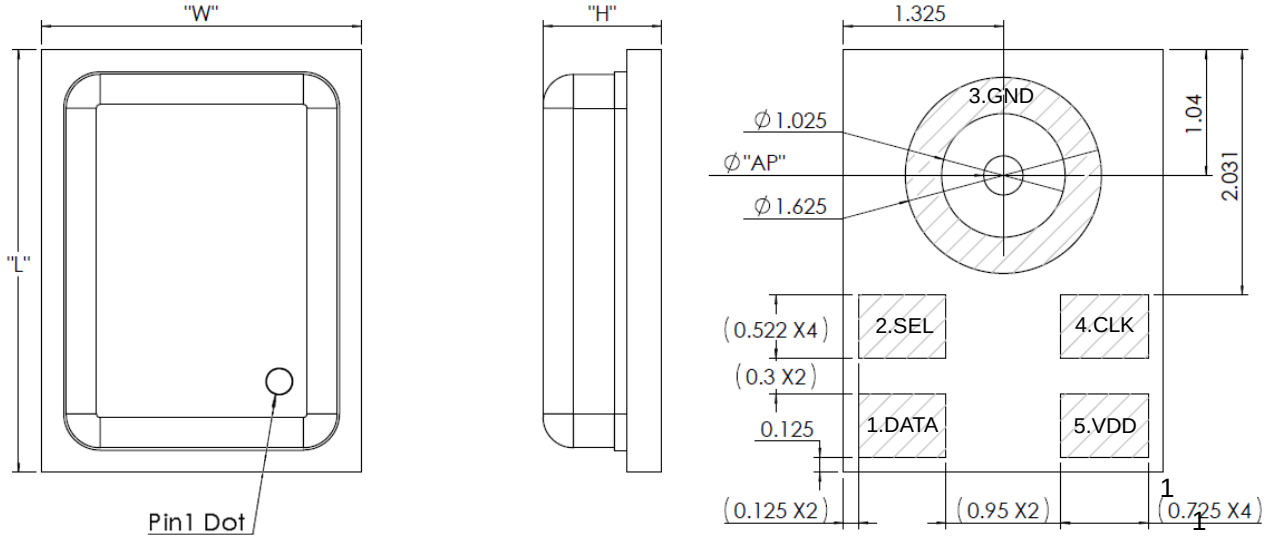
MECHANICAL SPECIFICATIOPNS



ITEM	DIMENSION	TOLERANCE	UNITS
Length (L)	3.50	±0.10	mm
Width (W)	2.65	±0.10	mm
Height (H)	0.98	±0.10	mm
Acoustic Port (AP)	Ø0.325	±0.05	mm

Pin	Symbol	Description
1	DATA	Output.
2	SELECT	Select.
3	GND	Ground
4	CLOCK	Clock.
5	VDD	Power Supply (V_{DD}).

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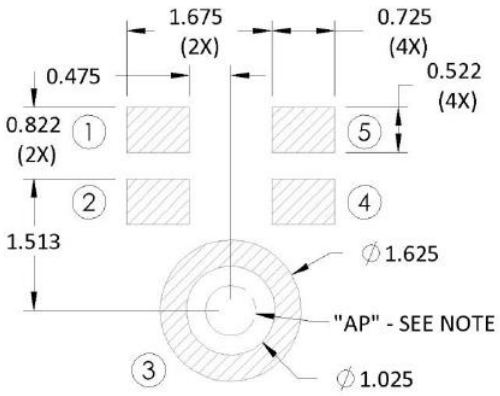
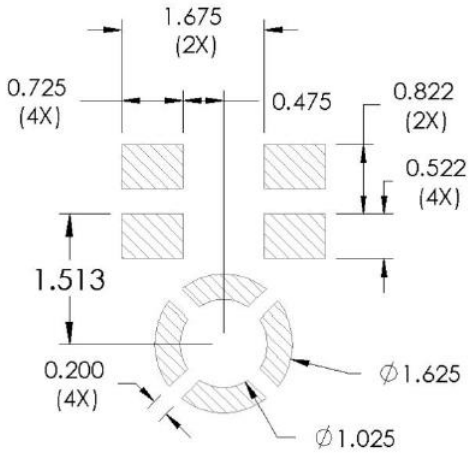
RECOMMENDED CUSTOMER LAND PATTERN

The recommended PCB land pattern for the ZTS6872SE should have a 1:1 ratio to the solder pads on the microphone package. Care should be taken to avoid applying solder paste to the sound hole in PCB. The dimensions of suggested solder paste pattern refer to the land pattern.



PCB Land Pattern Layout (Dimensions Shown in mm).



Suggested Solder Paste Stencil Pattern Layout.

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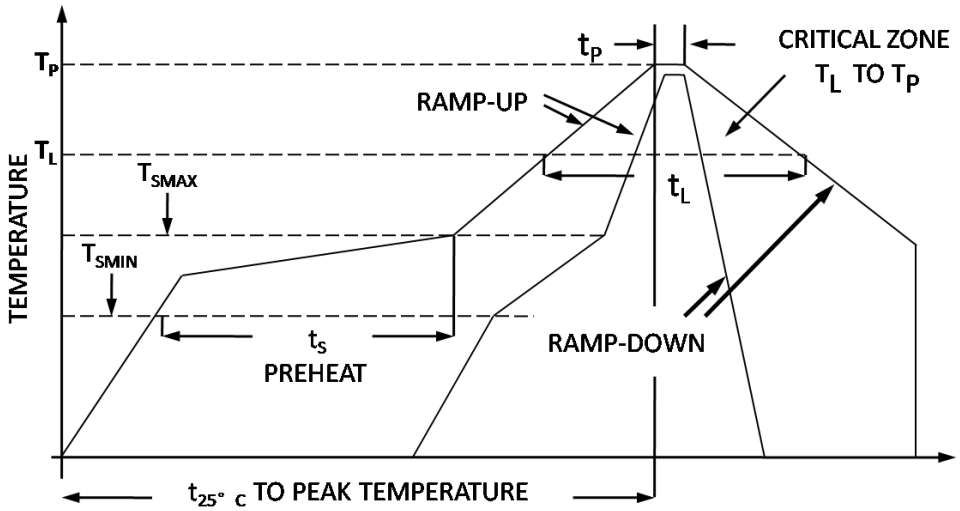
SOLDER FLOW PROFILE

The reflow profile specified in this section describes expected maximum heat exposure of components during the reflow process of NMP product PWBs. Temperature is measured on top of component. All components have to tolerate at least this profile five times (5x) without affecting electrical performance, mechanical performance or reliability.



Pb-free reflow profile requirements for soldering heat resistance:

Parameter		Reference	Pb-Free
Average Ramp Rate		T_L to T_P	3°C/sec max
Preheat	Minimum Temperature	T_{SMIN}	150°C
	Maximum Temperature	T_{SMAX}	200°C
	Time	T_{SMIN} to T_{SMAX}	60sec to 180sec
Time Maintained Above	Temperature	T_L	217°C
	Time	t_L	60sec to 150sec
Peak Temperature		T_P	260°C
Time Within +5°C of Actual Peak Temperature		t_P	20 sec to 40 sec
Ramp-Down Rate		T_{peak}	6°C/sec max
Time +25°C (t_{25OC}) to Peak Temperature			8 min max

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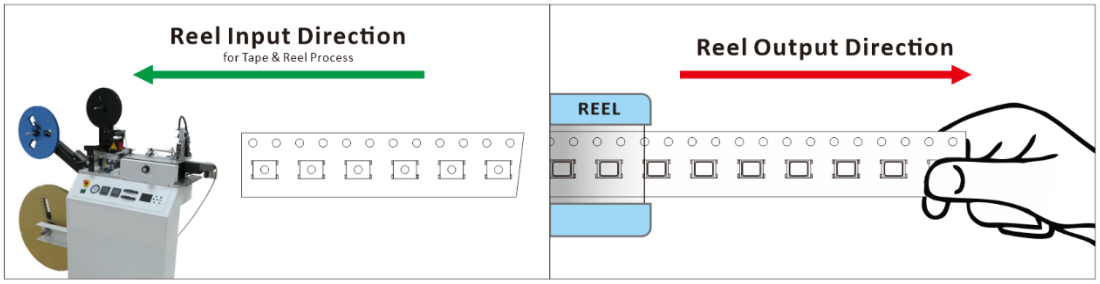
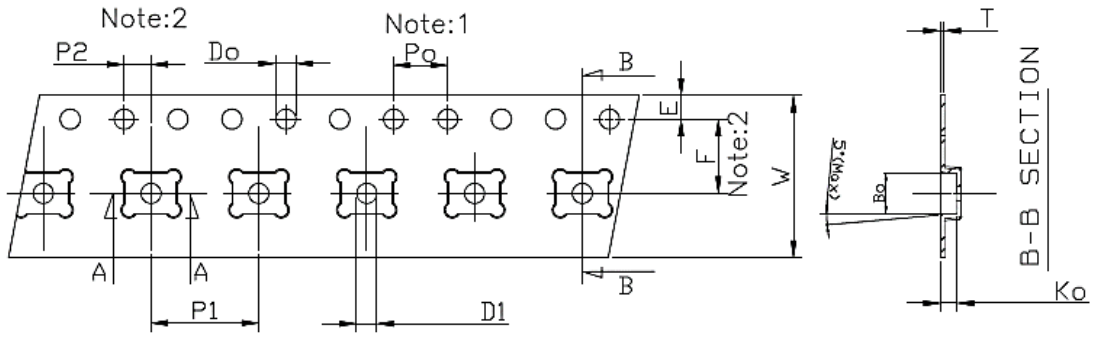
PACKAGING





Ao= 3.80±0.10 mm

Bo= 2.95±0.10 mm

Ko= 1.25±0.10 mm

Unit: mm

Symbol	Spec.
Po	4.0±0.10
P1	8.0±0.10
P2	2.0±0.05
Do	$1.50^{+0.10}_{-0.}$
D1	1.50(MIN)
E	1.75±0.10
F	5.50±0.05
10Po	40.0±0.10
W	$12.0^{+0.30}_{-0.10}$
T	0.30±0.05

Notice:

1. 10 Sprocket hole pitch cumulative tolerance is ±0.1mm
2. Pocket position relative to sprocket hole measured as true position of pocket not pocket hole.
3. Ao & Bo measured on a place 0.3mm above the bottom of the pocket to top surface of the carrier.
4. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
5. Carrier camber shall be not than 1mm per 100mm through a length of 250mm.

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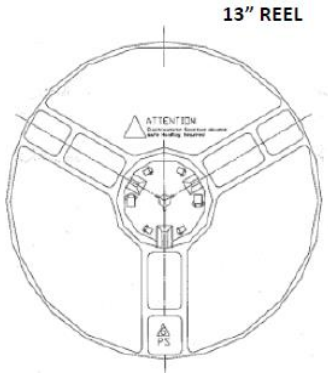
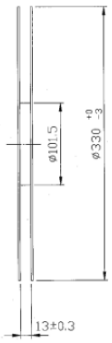
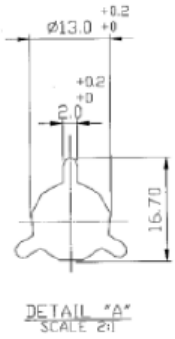
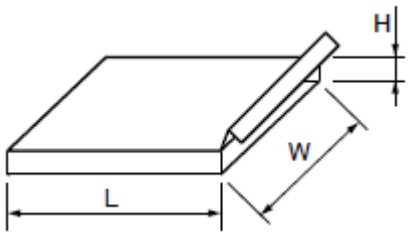






Part NO.	Reel Diameter	Quantity Per Reel	Quantity Per Inner Box	Quantity Per Outer Box
ZTS6872SE	13"	5200	5200	46800

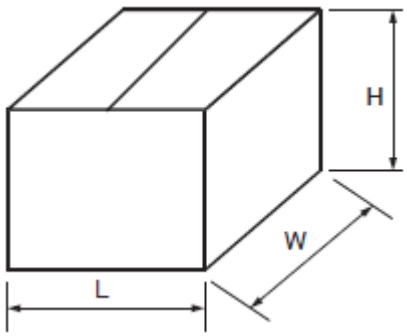
Dimensions for Inner Box



Unit：mm

L	W	H
335	339	45

Dimensions for Outer Box



Unit：mm

L	W	H
445	360	372

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