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Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

S98FL256S (×8)
S98FL512S (×8)
S98FL01GS (×8)

SUPPLEMENT

256 Mb (32 MB)/512 Mb (64 MB)/ 1 Gb (128 MB), 3.0 V, MirrorBit Flash

General Description

This supplementary document provides information on a device designed for limited distribution. It describes how the features, operation, and ordering options of this device have been enhanced or changed from the standard device on which it is based. The information contained in this document modifies any information on the same topics established by the datasheets listed in the Affected Documents/Related Documents and should be used in conjunction with those documents. This document may also contain information that was not previously covered by the S79FL256S/S79FL512S and S79FL01GS datasheets. It is intended for hardware system designers and software developers of applications, operating systems, or tools.

Affected Documents/Related Documents

Title	Publication Number
S79FL256S/S79FL512S Datasheet	002-00518
S79FL01GS Datasheet	002-00466

Timing Specifications

The specification parameters that changed from the standard S79FL256S/S79FL512S and S79FL01GS datasheets are listed in the following tables.

Table 1. AC and DC Characteristics Parameters Changed

Symbol	Parameter	Standard Spec	S98 Spec	Unit
t_V	Clock Low to Output Valid (maximum)	6.5	4.25	ns
t_{SU}	Data in Setup Time	1.5	1.4	ns
Fsck, R	SCK Clock Frequency for DDR Read instruction	80	87 (1)/60 (2)	MHz
Psck, R	SCK Clock Period for DDR Read Instruction (min)	12.5	11.5 (3)/16.7 (4)	ns
I_{CC1}	Active Power Supply Current (Read) Quad DDR at 80 MHz	180	76	mA
I_{CC2}	Active Power Supply Current (Page Program) CS# = V_{IO}	200	120	mA
I_{CC3}	Active Power Supply Current (WRR) CS# = V_{IO}	200	120	mA
I_{CC4}	Active Power Supply Current (SE) CS# = V_{IO}	200	120	mA
I_{CC5}	Active Power Supply Current (BE) CS# = V_{IO}	200	120	mA

Notes:

1. *V_{CC} range (2.9 V – 3.6 V) and CL = 10 pF. The max t_V time will apply for all DDR frequencies ≤ 87 MHz.*
2. *V_{CC} range (2.7 V – 3.6 V) and CL = 10 pF. The max t_V time will apply for all DDR frequencies ≤ 60 MHz.*
3. *Applies for a DDR frequency of 87 MHz.*
4. *Applies for a DDR frequency of 60 MHz.*

The latency table for 87 MHz is as follows.

Table 2. Latency table for 87 MHz

Frequency (MHz)	LC	DDR Quad I/O Read (EDh, EEh)	
		Mode	Dummy
80 MHz ≤ 90 MHz	01	1	7

Clock (SCK) Input Glitch Parametric

Figure 1. Clock (SCK) Input Glitch (1)(2)

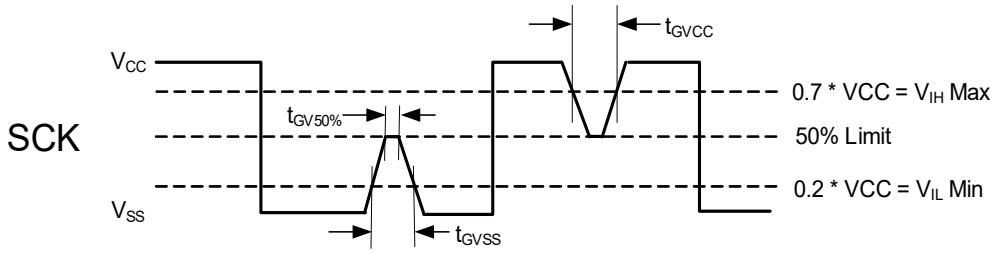


Table 3. Clock (SCK) Input Glitch

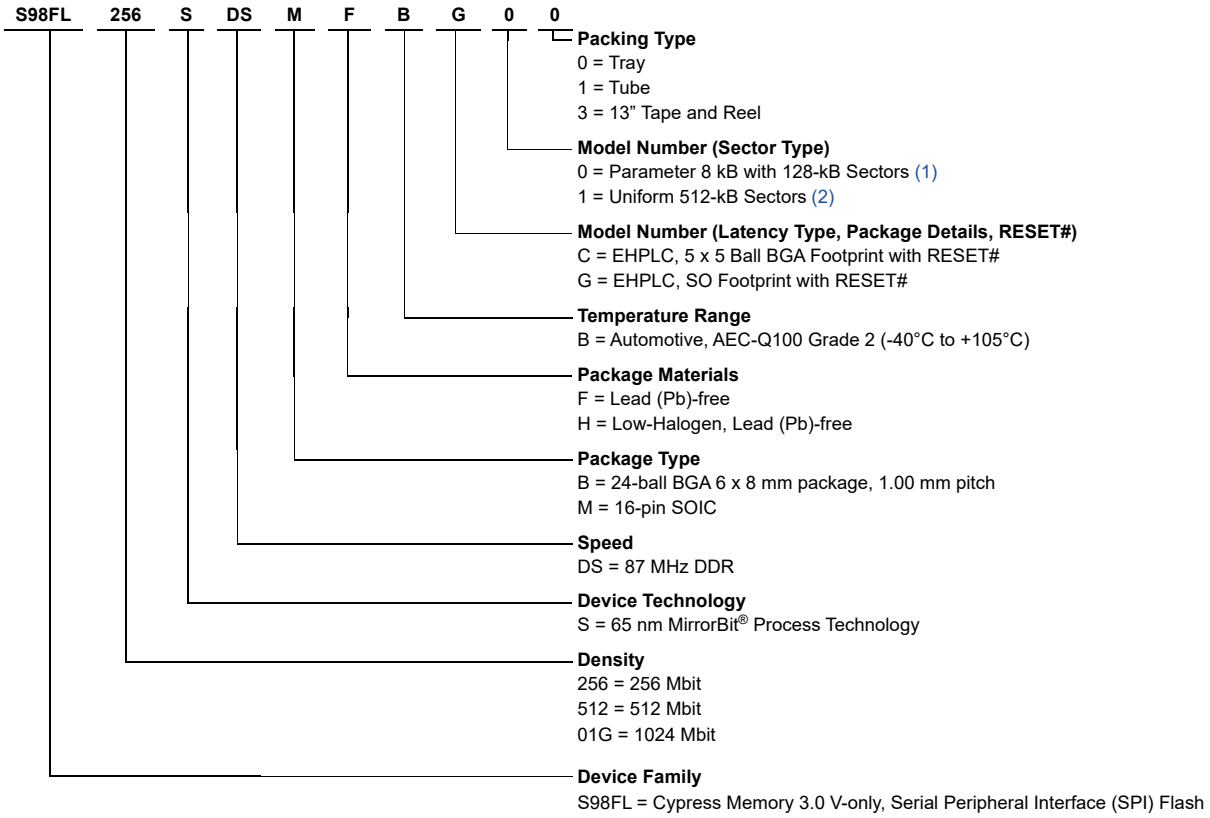
Symbol	Parameter	Spec		Unit
		Min	Max	
t_{GVSS}	Glitch from V_{SS} to 0.4 * V_{CC}	-	2.0	ns
t_{GVCC}	Glitch from V_{CC} to 0.6 * V_{CC}	-	2.0	
$t_{GV50\%}$	Glitch at 0.5 * V_{CC}	-	1.5	

Notes:

1. *SCK input signal glitch must not cross the 50% limit line (VCC/2) and shall remain within the timing boundary parameters as stated in Table 3.*
2. *A glitch shall not occur during the falling or rising edge of the SCK signal before the SCK signal reached VIL max. or VIH min. resp. SCK setup and hold time must not be violated.*

Ordering Part Numbers

The ordering part number is formed by a valid combination of the following:



Notes:

1. *Parameter with 128-kB sectors = A parameter of 32 × 8-kB sectors with all remaining sectors being 128 kB, with a 512B programming buffer.*
2. *Uniform 512-kB sectors = All sectors are uniform 512 kB with a 1024B programming buffer.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Contact the local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 4. Valid Combinations

Valid Combinations					
Base Ordering Part Number	**Speed Option**	**Package and Temperature**	**Model Number**	**Packing Type**	**Package Marking**
S98FL256S	DS	MFB	G0	0, 1, 3	98FL256SSBFG0
S98FL512S	DS	MFB	G0	0, 1, 3	98FL512SSBFG0
S98FL01GS	DS	BHB	C1	0, 1, 3	98FL01GSSBHC1

Document History Page

Document Title: S98FL256S (×8)/S98FL512S (×8)/S98FL01GS (×8), 256 Mb (32 MB)/512 Mb (64 MB)/1 Gb (128 MB), 3.0 V, MirrorBit Flash Document Number: 002-12608			
Rev.	**ECN**	**Submission Date**	**Description of Change**
**	5249635	04/29/2016	Initial release.
*A	5390725	08/04/2016	Updated Ordering Part Numbers: Updated details under “Model Number (Sector Type)” and “Temperature Range”.
*B	5584047	01/12/2017	Updated Ordering Part Numbers: Updated Valid Combinations: Updated Table 4: Updated details under “Package Marking” column. Updated to new template.
*C	5767436	06/08/2017	Updated Timing Specifications: Updated Table 1: Added t_{SU} parameter and its corresponding details. Updated to new template.
*D	6762483	12/27/2019	Added Electrical Specifications. Updated to new template.
*E	6796649	02/04/2020	Removed Electrical Specifications. Added Clock (SCK) Input Glitch Parametric. Updated to new template.

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