

Please note that Cypress is an Infineon Technologies Company.

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.



SUPPLEMENT

S98FL256S (×8)

S98FL512S (×8)

S98FL01GS (×8)

256 Mb (32 MB)/512 Mb (64 MB)/
1 Gb (128 MB), 3.0 V, MirrorBit Flash

General Description

This supplementary document provides information on a device designed for limited distribution. It describes how the features, operation, and ordering options of this device have been enhanced or changed from the standard device on which it is based. The information contained in this document modifies any information on the same topics established by the datasheets listed in the [Affected Documents/Related Documents](#) and should be used in conjunction with those documents. This document may also contain information that was not previously covered by the S79FL256S/S79FL512S and S79FL01GS datasheets. It is intended for hardware system designers and software developers of applications, operating systems, or tools.

Affected Documents/Related Documents

Title	Publication Number
S79FL256S/S79FL512S Datasheet	002-00518
S79FL01GS Datasheet	002-00466

Timing Specifications

The specification parameters that changed from the standard S79FL256S/S79FL512S and S79FL01GS datasheets are listed in the following tables.

Table 1. AC and DC Characteristics Parameters Changed

Symbol	Parameter	Standard Spec	S98 Spec	Unit
t_V	Clock Low to Output Valid (maximum)	6.5	4.25	ns
t_{SU}	Data in Setup Time	1.5	1.4	ns
Fsck, R	SCK Clock Frequency for DDR Read instruction	80	87 (1)/60 (2)	MHz
Psck, R	SCK Clock Period for DDR Read Instruction (min)	12.5	11.5 (3)/16.7 (4)	ns
I_{CC1}	Active Power Supply Current (Read) Quad DDR at 80 MHz	180	76	mA
I_{CC2}	Active Power Supply Current (Page Program) CS# = V_{IO}	200	120	mA
I_{CC3}	Active Power Supply Current (WRR) CS# = V_{IO}	200	120	mA
I_{CC4}	Active Power Supply Current (SE) CS# = V_{IO}	200	120	mA
I_{CC5}	Active Power Supply Current (BE) CS# = V_{IO}	200	120	mA

Notes:

1. V_{CC} range (2.9 V – 3.6 V) and $CL = 10$ pF. The max t_V time will apply for all DDR frequencies ≤ 87 MHz.
2. V_{CC} range (2.7 V – 3.6 V) and $CL = 10$ pF. The max t_V time will apply for all DDR frequencies ≤ 60 MHz.
3. Applies for a DDR frequency of 87 MHz.
4. Applies for a DDR frequency of 60 MHz.

The latency table for 87 MHz is as follows.

Table 2. Latency table for 87 MHz

Frequency (MHz)	LC	DDR Quad I/O Read	
		(EDh, EEh)	
		Mode	Dummy
80 MHz \leq 90 MHz	01	1	7

Clock (SCK) Input Glitch Parametric

Figure 1. Clock (SCK) Input Glitch (1)(2)

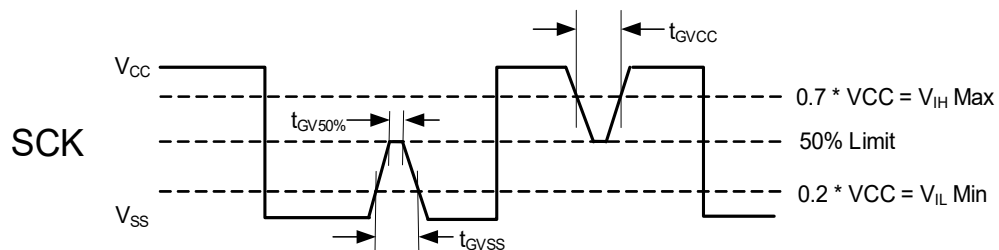


Table 3. Clock (SCK) Input Glitch

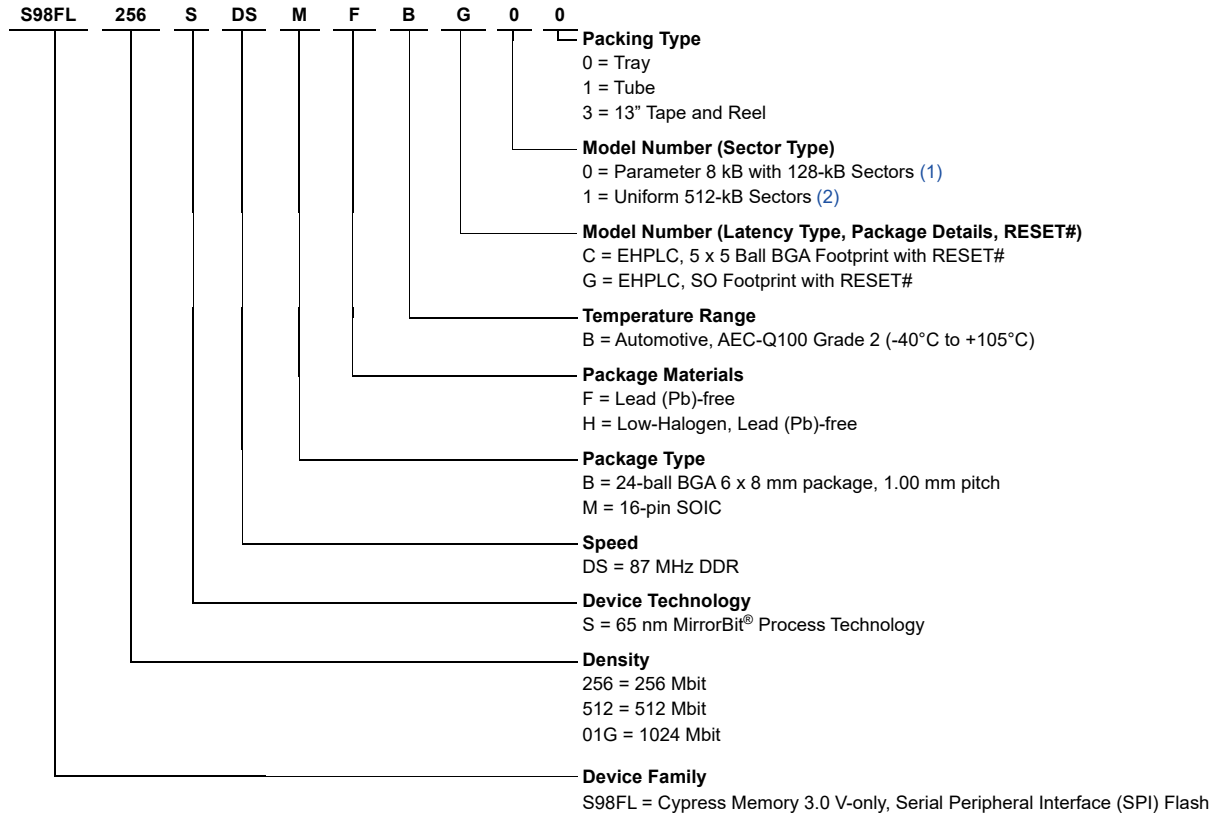
Symbol	Parameter	Spec		Unit
		Min	Max	
t_{GVSS}	Glitch from V_{SS} to $0.4 * V_{CC}$	-	2.0	ns
t_{GVCC}	Glitch from V_{CC} to $0.6 * V_{CC}$	-	2.0	
$t_{GV50\%}$	Glitch at $0.5 * V_{CC}$	-	1.5	

Notes:

1. SCK input signal glitch must not cross the 50% limit line ($V_{CC}/2$) and shall remain within the timing boundary parameters as stated in [Table 3](#).
2. A glitch shall not occur during the falling or rising edge of the SCK signal before the SCK signal reached $V_{IL} \text{ max.}$ or $V_{IH} \text{ min.}$ resp. SCK setup and hold time must not be violated.

Ordering Part Numbers

The ordering part number is formed by a valid combination of the following:



Notes:

- Parameter with 128-kB sectors = A parameter of 32 x 8-kB sectors with all remaining sectors being 128 kB, with a 512B programming buffer.
- Uniform 512-kB sectors = All sectors are uniform 512 kB with a 1024B programming buffer.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Contact the local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 4. Valid Combinations

Valid Combinations					
Base Ordering Part Number	Speed Option	Package and Temperature	Model Number	Packing Type	Package Marking
S98FL256S	DS	MFB	G0	0, 1, 3	98FL256SSBFG0
S98FL512S	DS	MFB	G0	0, 1, 3	98FL512SSBFG0
S98FL01GS	DS	BHB	C1	0, 1, 3	98FL01GSSBHC1

Document History Page

Document Title: S98FL256S (×8)/S98FL512S (×8)/S98FL01GS (×8), 256 Mb (32 MB)/512 Mb (64 MB)/1 Gb (128 MB), 3.0 V, MirrorBit Flash Document Number: 002-12608			
Rev.	ECN	Submission Date	Description of Change
**	5249635	04/29/2016	Initial release.
*A	5390725	08/04/2016	Updated Ordering Part Numbers : Updated details under “Model Number (Sector Type)” and “Temperature Range”.
*B	5584047	01/12/2017	Updated Ordering Part Numbers : Updated Valid Combinations : Updated Table 4 : Updated details under “Package Marking” column. Updated to new template.
*C	5767436	06/08/2017	Updated Timing Specifications : Updated Table 1 : Added t_{SU} parameter and its corresponding details. Updated to new template.
*D	6762483	12/27/2019	Added Electrical Specifications. Updated to new template.
*E	6796649	02/04/2020	Removed Electrical Specifications. Added Clock (SCK) Input Glitch Parametric . Updated to new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Code Examples](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2016–2020. This document is the property of Cypress Semiconductor Corporation and its subsidiaries ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress shall have no liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. CYPRESS DOES NOT REPRESENT, WARRANT, OR GUARANTEE THAT CYPRESS PRODUCTS, OR SYSTEMS CREATED USING CYPRESS PRODUCTS, WILL BE FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (collectively, "Security Breach"). Cypress disclaims any liability relating to any Security Breach, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any Security Breach. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. "High-Risk Device" means any device or system whose failure could cause personal injury, death, or property damage. Examples of High-Risk Devices are weapons, nuclear installations, surgical implants, and other medical devices. "Critical Component" means any component of a High-Risk Device whose failure to perform can be reasonably expected to cause, directly or indirectly, the failure of the High-Risk Device, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any use of a Cypress product as a Critical Component in a High-Risk Device. You shall indemnify and hold Cypress, its directors, officers, employees, agents, affiliates, distributors, and assigns harmless from and against all claims, costs, damages, and expenses, arising out of any claim, including claims for product liability, personal injury or death, or property damage arising from any use of a Cypress product as a Critical Component in a High-Risk Device. Cypress products are not intended or authorized for use as a Critical Component in any High-Risk Device except to the limited extent that (i) Cypress's published data sheet for the product explicitly states Cypress has qualified the product for use in a specific High-Risk Device, or (ii) Cypress has given you advance written authorization to use the product as a Critical Component in the specific High-Risk Device and you have signed a separate indemnification agreement.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.