Rochester Electronics

Datasheet

PART NUMBER

CD74HC4511EE4-ROC

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

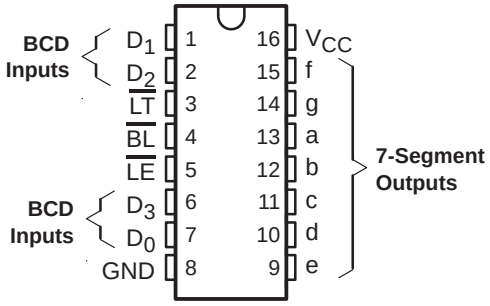
- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

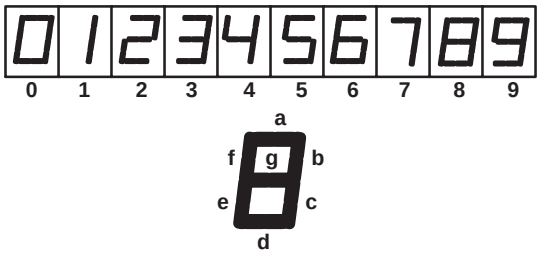
The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

- **2-V to 6-V V_{CC} Operation ('HC4511)**
- **4.5-V to 5.5-V V_{CC} Operation (CD74HCT4511)**
- **High-Output Sourcing Capability**
  - **7.5 mA at 4.5 V (CD74HCT4511)**
  - **10 mA at 6 V ('HC4511)**
- **Input Latches for BCD Code Storage**
- **Lamp Test and Blanking Capability**
- **Balanced Propagation Delays and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **'HC4511**
  - **High Noise Immunity, N_{IL} or N_{IH} = 30% of V_{CC} at V_{CC} = 5 V**
- **CD74HCT4511**
  - **Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8 V Maximum, V_{IH} = 2 V Minimum**
  - **CMOS Input Compatibility, $I_I \le 1\ \mu A$ at V_{OL}, V_{OH}**

CD54HC4511 . . . F PACKAGE
CD74HC4511 . . . E, M, OR PW PACKAGE
CD74HCT4511 . . . E PACKAGE
(TOP VIEW)



DISPLAY



description/ordering information

The CD54HC4511, CD74HC4511, and CD74HCT4511 are BCD-to-7 segment latch/decoder/drivers with four address inputs (D_0−D_3), an active-low blanking ($\overline{BL}$) input, lamp-test ($\overline{LT}$) input, and a latch-enable ($\overline{LE}$) input that, when high, enables the latches to store the BCD inputs. When $\overline{LE}$ is low, the latches are disabled, making the outputs transparent to the BCD inputs.

These devices have standard-size output transistors, but are capable of sourcing (at standard V_{OH} levels) up to 7.5 mA at 4.5 V. The HC types can supply up to 10 mA at 6 V.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−55°C to 125°C	PDIP − E	Tube of 25	CD74HC4511E	CD74HC4511E
			CD74HCT4511E	CD74HCT4511E
	SOIC − M	Tube of 40	CD74HC4511M	HC4511M
		Reel of 2500	CD74HC4511M96	
		Reel of 250	CD74HC4511MT	
	TSSOP − PW	Reel of 2000	CD74HC4511PWR	HJ4511
		Reel of 250	CD74HC4511PWT	
	CDIP − F	Tube of 25	CD54HC4511F3A	CD54HC4511F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTION TABLE

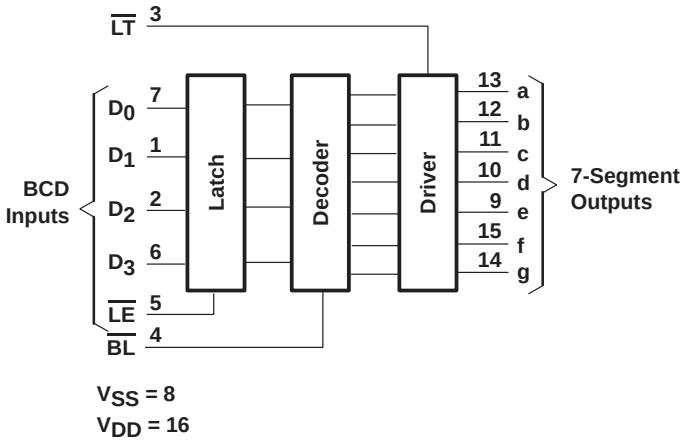
INPUTS							OUTPUTS							
$\overline{LE}$	$\overline{BL}$	$\overline{LT}$	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	DISPLAY
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	Blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	Blank
H	H	H	X	X	X	X	†	†	†	†	†	†	†	†

X = Don't care

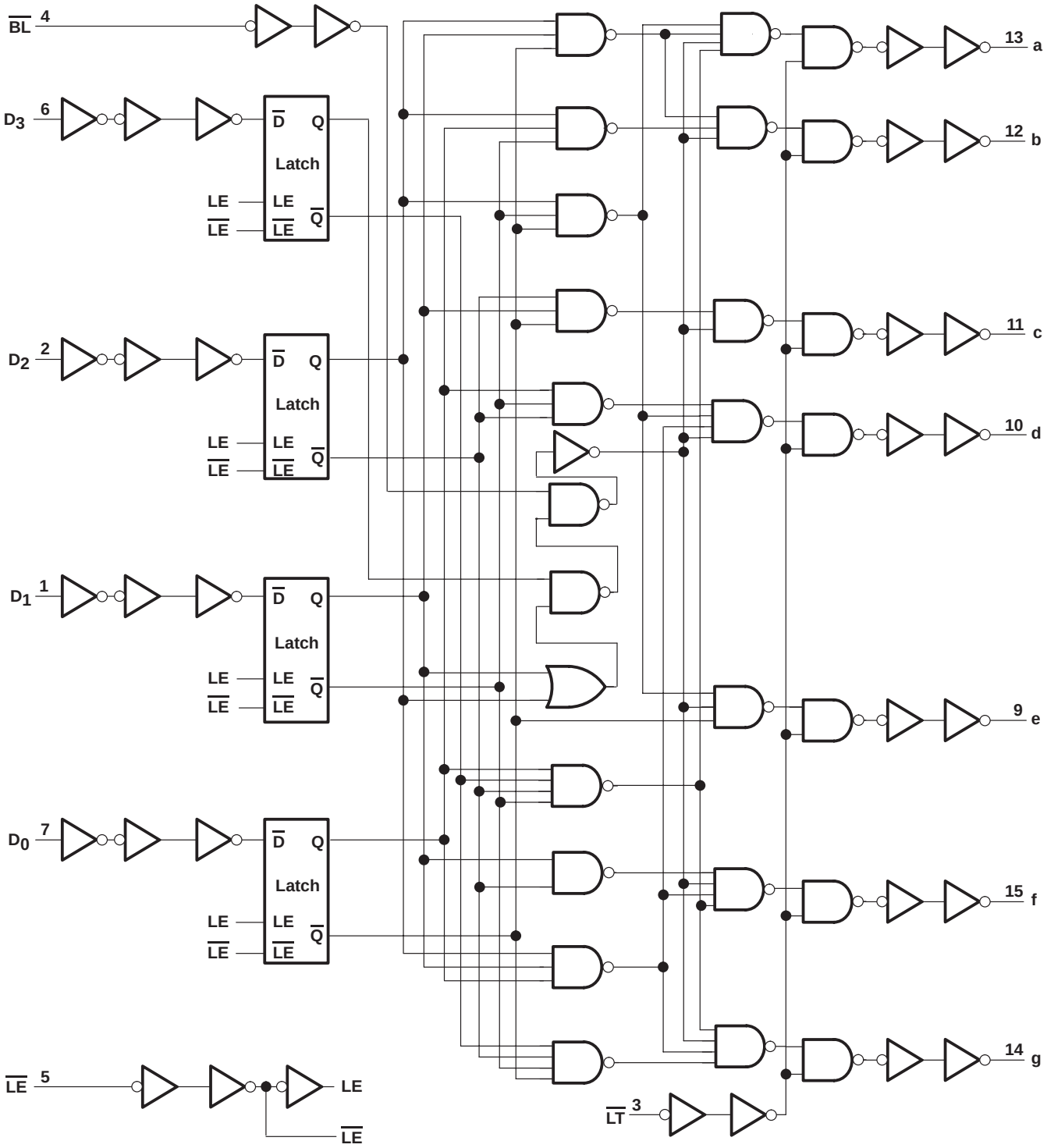
† Depends on BCD code previously applied when $\overline{LE}$ = L

NOTE: Display is blank for all illegal input codes (BCD > HLLH).

function diagram



logic diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input diode current, I_{IK} ($V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)) (see Note 1) . . . . . ±20 mA
Output diode current, I_{OK} ($V_O < -0.5$ V or $V_O > V_{CC} + 0.5$V) (see Note 1) . . . . . ±20 mA
Continuous output source or sink current per output, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): E package . . . . . 67°C/W
M package . . . . . 73°C/W
PW package . . . . . 108°C/W
Lead temperature (during soldering):
At distance 1/16 ± 1/32 in (1.59 ± 0.79 mm) from case for 10 s maximum . . . . . 265°C
Unit inserted into a PC board (minimum thickness 1/16 in, 1.59 mm),
with solder contacting lead tips only . . . . . 300°C
Storage temperature, T_{stg} . . . . . −65 to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions for ’HC4511 (see Note 3)

			T_A = 25°C		T_A = −55°C TO 125°C		T_A = −40°C TO 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	6	2	6	2	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		1.5		V
		V_{CC} = 4.5 V	3.15		3.15		3.15		
		V_{CC} = 6 V	4.2		4.2		4.2		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5		0.5	V
		V_{CC} = 4.5 V		1.35		1.35		1.35	
		V_{CC} = 6 V		1.8		1.8		1.8	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V		1000		1000		1000	ns
		V_{CC} = 4.5 V		500		500		500	
		V_{CC} = 6 V		400		400		400	

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions for CD74HCT4511 (see Note 4)

		T_A = 25°C		T_A = −55°C TO 125°C		T_A = −40°C TO 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		2		V
V_{IL}	Low-level input voltage		0.8		0.8		0.8	V
V_I	Input voltage		V_{CC}		V_{CC}		V_{CC}	V
V_O	Output voltage		V_{CC}		V_{CC}		V_{CC}	V
t_t	Input transition (rise and fall) time		500		500		500	ns

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

’HC4511

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C		T_A = −55°C TO 125°C		T_A = −40°C TO 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = −20 µA	2 V	1.9		1.9		1.9		V
			4.5 V	4.4		4.4		4.4		
			6 V	5.9		5.9		5.9		
		I_{OH} = −7.5 mA	4.5 V	3.98		3.7		3.84		
		I_{OH} = −10 mA	6 V	5.48		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V		0.1		0.1		0.1	V
			4.5 V		0.1		0.1		0.1	
			6 V		0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1		±1		±1	µA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V		8		160		80	µA
C_i					10		10		10	pF

CD74HCT4511

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			T_A = −55°C TO 125°C		T_A = −40°C TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = −20 μA	4.5 V	4.4			4.4		4.4		V
		I_{OH} = −4 mA		3.98			3.7		3.84		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5 V			0.1		0.1		0.1	V
		I_{OL} = 4 mA				0.26		0.4		0.33	
I_I	V_I = V_{CC} to GND		5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or 0, I_O = 0		5.5 V			8		160		80	μA
ΔI_{CC}†	One input at V_{CC} − 2.1 V, Other inputs at 0 or V_{CC}		4.5 V to 5.5 V		100	360		490		450	μA
C_i						10		10		10	pF

† Additional quiescent supply current per input pin, TTL inputs high, 1 unit load. For dual-supply systems, theoretical worst-case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS‡
$\overline{LT}$, $\overline{LE}$	1.5
$\overline{BL}$, Dn	0.3

‡ Unit load is ΔI_{CC} limit specified in electrical characteristics table, e.g., 360 μA maximum at 25°C.

'HC4511 timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V_{CC}	T_A = 25°C		T_A = −55°C TO 125°C		T_A = −40°C TO 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LE}$ low	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, BCD inputs before $\overline{LE}$↑	2 V	60		90		75		ns
		4.5 V	12		18		15		
		6 V	10		15		13		
t_h	Hold time, BCD inputs before $\overline{LE}$↑	2 V	3		3		3		ns
		4.5 V	3		3		3		
		6 V	3		3		3		

’HC4511

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			T_A = −55°C TO 125°C		T_A = −40°C TO 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D_n	Output	C_L = 50 pF	2 V			300		450		375	ns
				4.5 V			60		90		75	
				6 V			51		77		64	
			C_L = 15 pF	5 V		25						
	$\overline{LE}$	Output	C_L = 50 pF	2 V			270		405		340	
				4.5 V			54		81		68	
				6 V			46		69		58	
			C_L = 15 pF	5 V		23						
	$\overline{BL}$	Output	C_L = 50 pF	2 V			220		330		275	
				4.5 V			44		66		55	
				6 V			37		56		47	
			C_L = 15 pF	5 V		18						
	$\overline{LT}$	Output	C_L = 50 pF	2 V			160		240		200	
				4.5 V			32		48		40	
				6 V			27		41		34	
			C_L = 15 pF	5 V		13						
t_t		Any	C_L = 50 pF	2 V			75		110		95	ns
				4.5 V			15		22		19	
				6 V			13		19		16	

CD74HCT4511

timing requirements over recommended operating free-air temperature range V_{CC} = 4.5 V (unless otherwise noted) (see Figure 2)

		T_A = 25°C		T_A = −55°C TO 125°C		T_A = −40°C TO 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LE}$ low	16		24		20		ns
t_{su}	Setup time, BCD inputs before $\overline{LE}\uparrow$	16		24		20		ns
t_h	Hold time, BCD inputs before $\overline{LE}\uparrow$	5		5		5		ns

CD74HCT4511

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

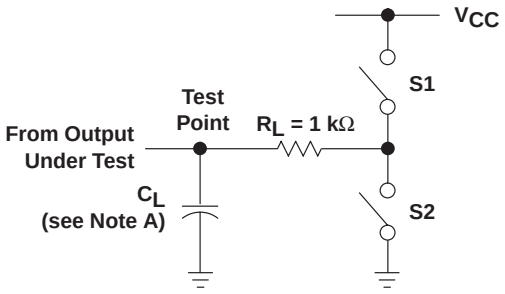
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			T_A = −55°C TO 125°C		T_A = −40°C TO 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D_n	Output	C_L = 50 pF	4.5 V			60		90		75	ns
			C_L = 15 pF	5 V		25						
	$\overline{LE}$	Output	C_L = 50 pF	4.5 V			54		81		68	
			C_L = 15 pF	5 V		23						
	$\overline{BL}$	Output	C_L = 50 pF	4.5 V			44		66		55	
			C_L = 15 pF	5 V		18						
	$\overline{LT}$	Output	C_L = 50 pF	4.5 V			33		50		41	
			C_L = 15 pF	5 V		13						
t_t		Any	C_L = 50 pF	4.5 V			15		22		19	ns

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TYP	UNIT
C_{pd}†	Power dissipation capacitance	'HC4511	114	pF
		CD74HCT4511	110	

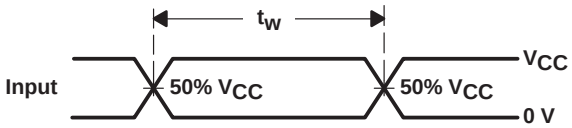
† C_{pd} is used to determine the dynamic power consumption, per package.
$P_D = C_{pd} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$
where: f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage

PARAMETER MEASUREMENT INFORMATION − ’HC4511

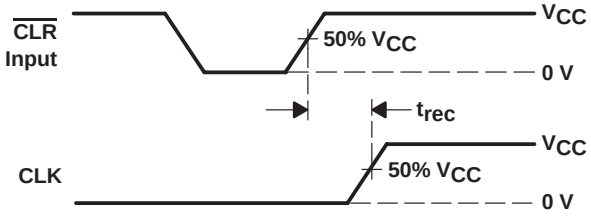


LOAD CIRCUIT

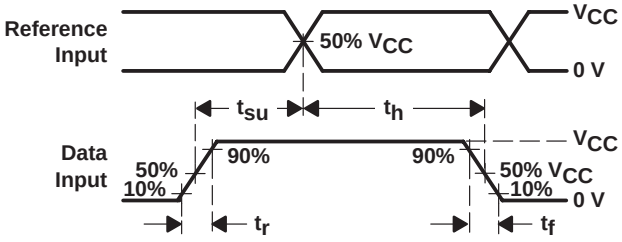
PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd} or t_t		Open	Open



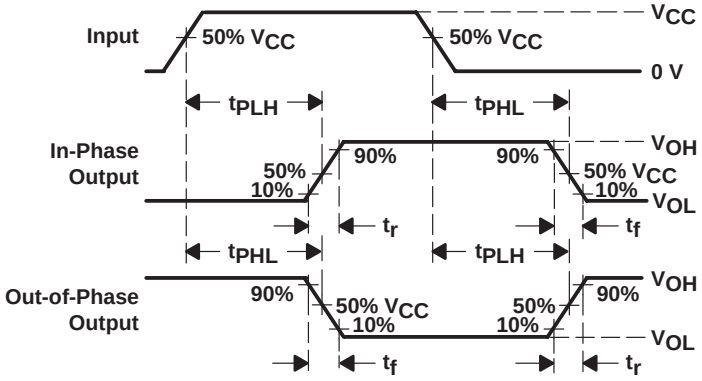
VOLTAGE WAVEFORMS
PULSE DURATION



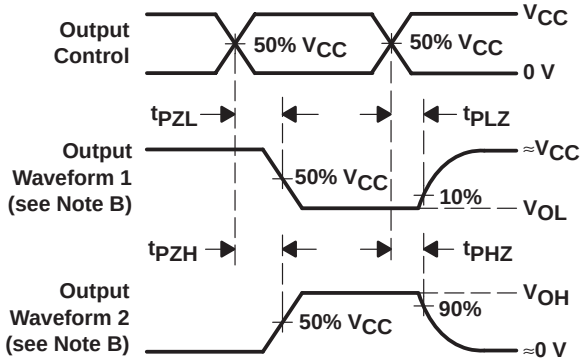
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

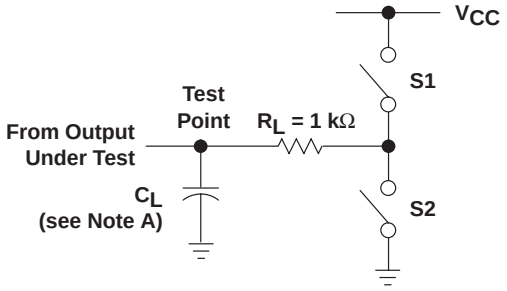


VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

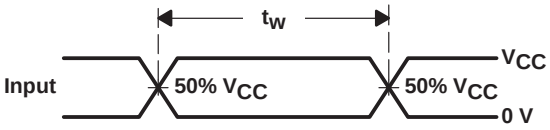
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION − CD74HCT4511

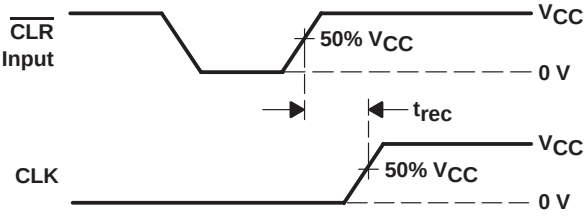


LOAD CIRCUIT

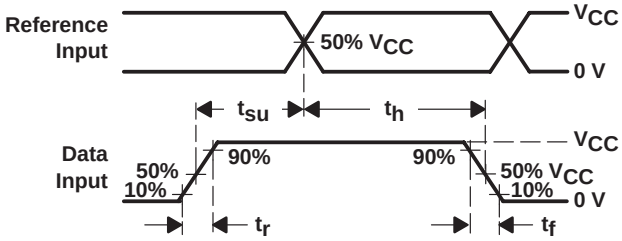
PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd} or t_t		Open	Open



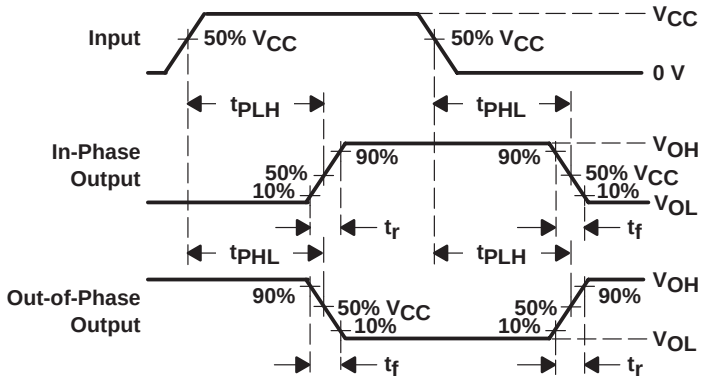
VOLTAGE WAVEFORMS
PULSE DURATION



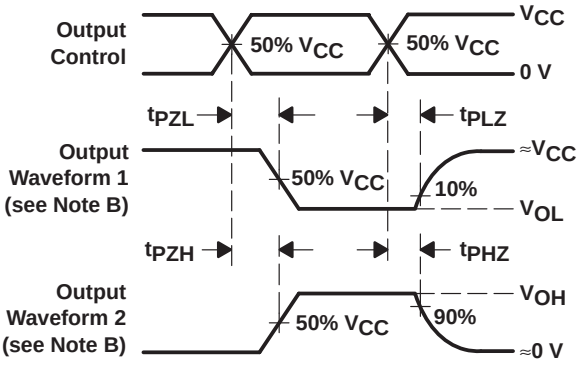
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-8773301EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD54HC4511F3A	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD74HC4511E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HC4511EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HC4511M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4511M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4511M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4511ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4511MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4511MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4511PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4511PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4511PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4511PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4511E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HCT4511EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

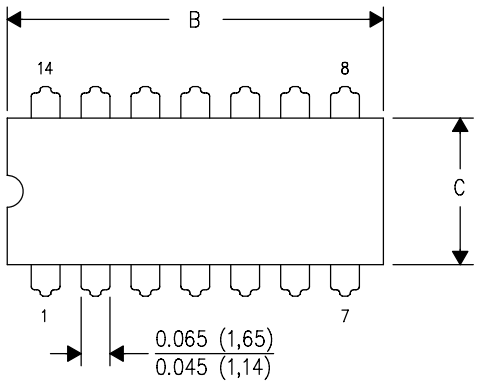
provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

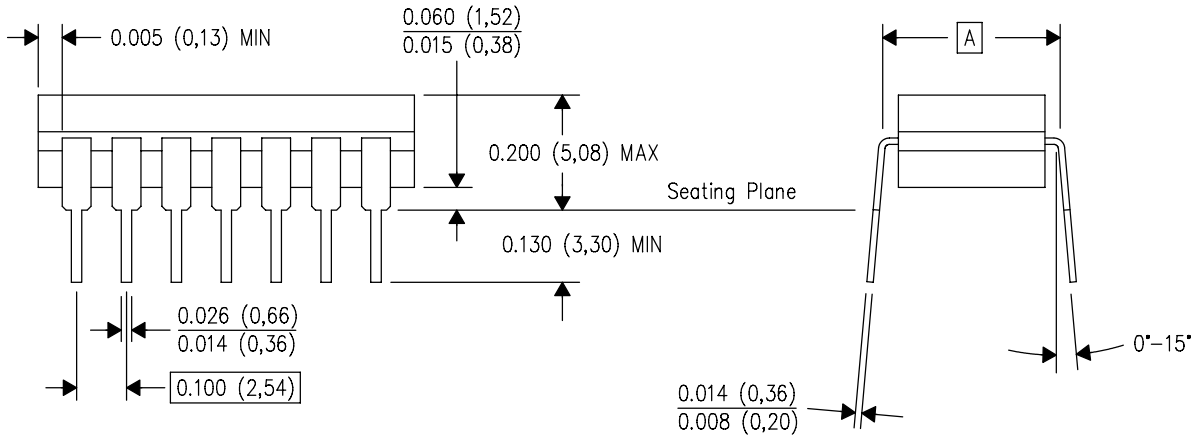
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



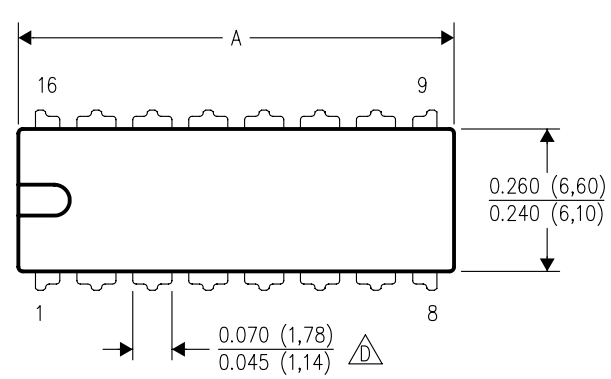
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

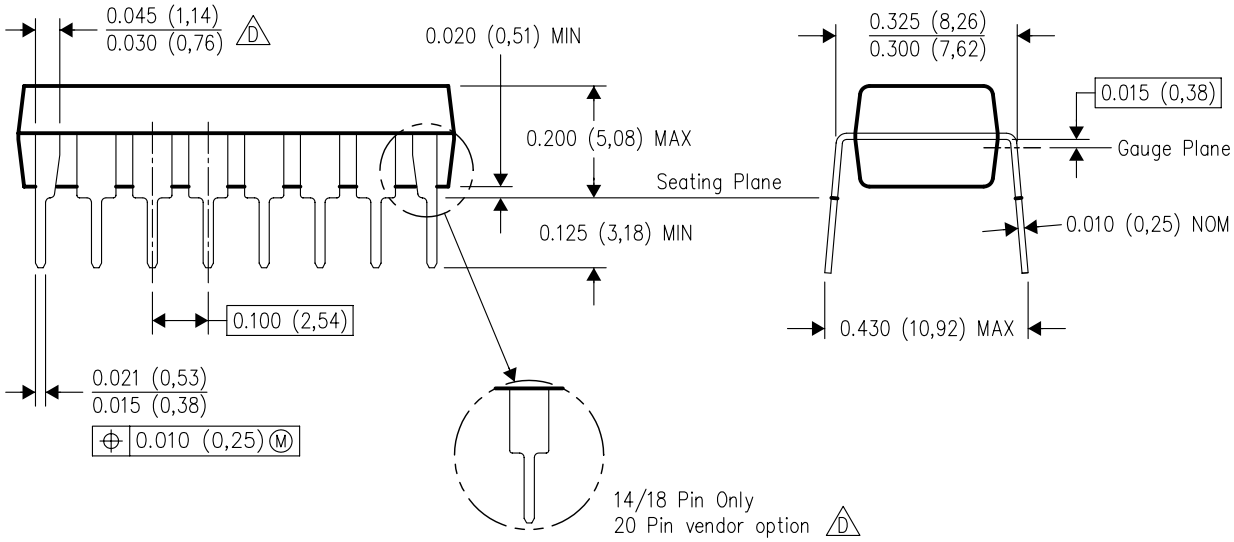
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



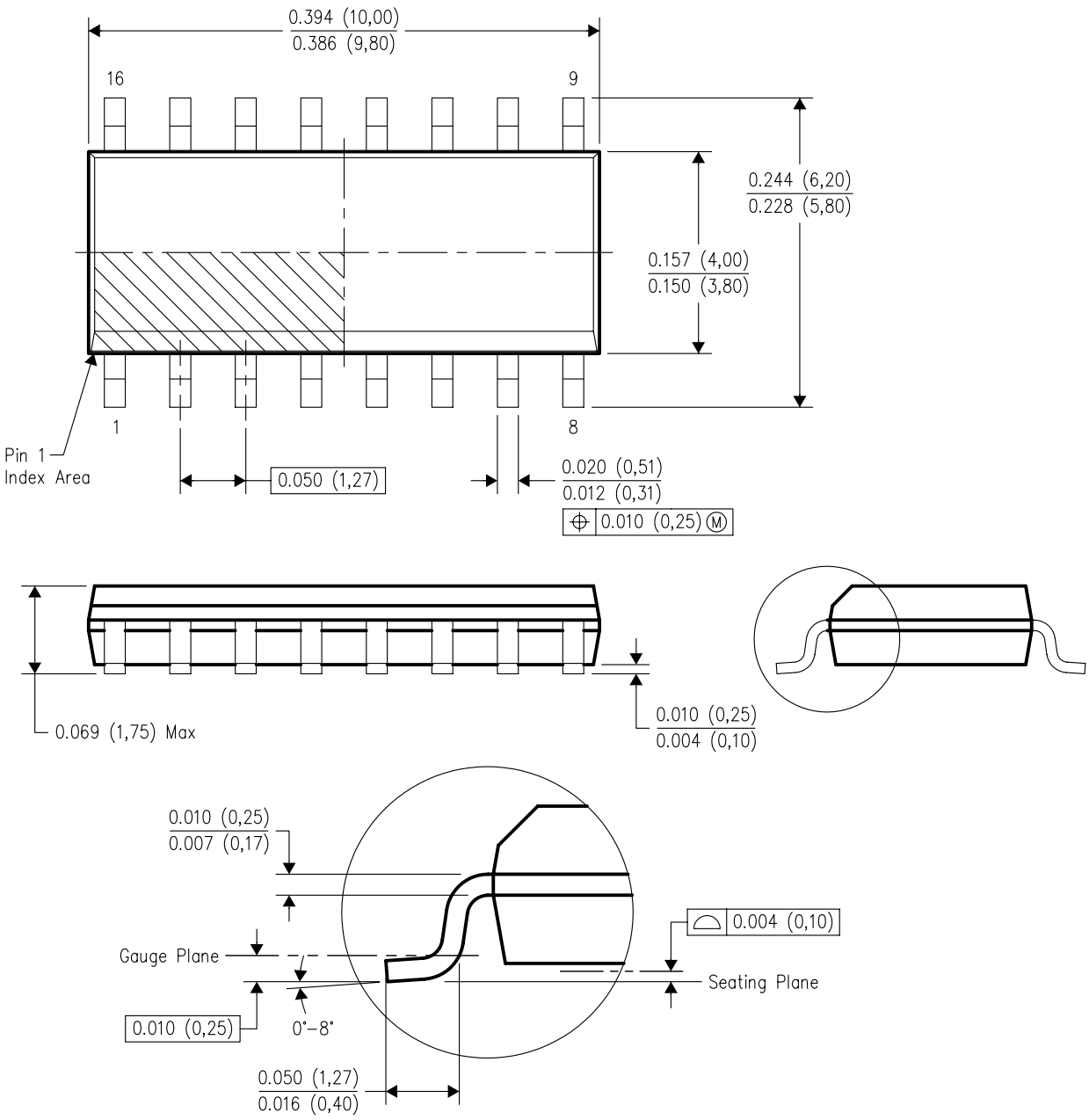
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

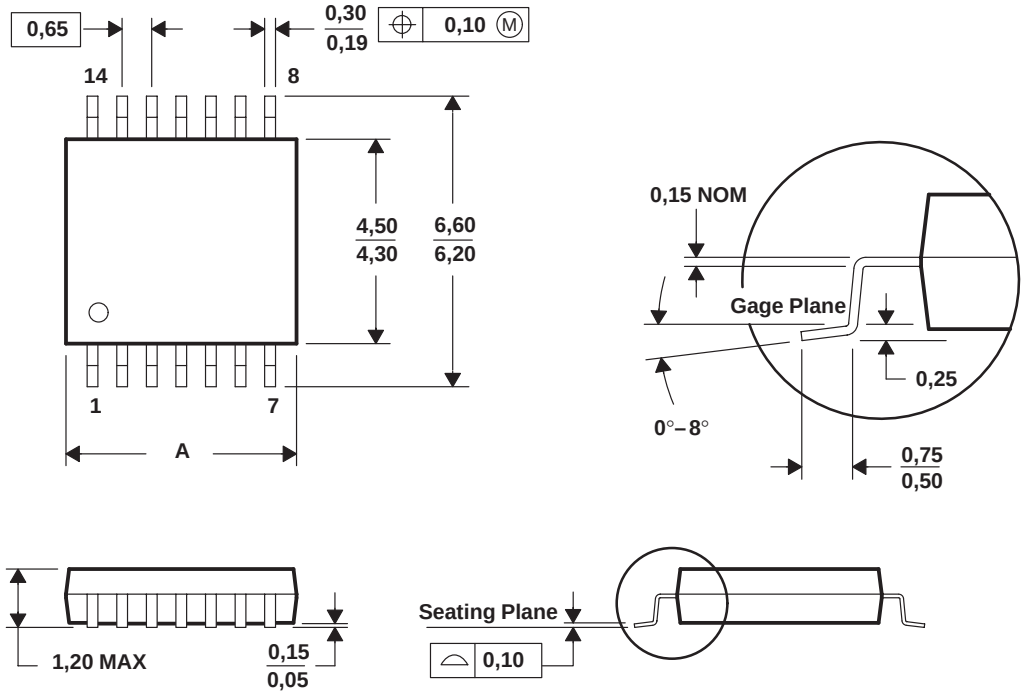
D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AC.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

View ROHS Compliant Devices
View RoHS Compliant Devices
clear gif

CD74HC4511, Status: ACTIVE

High Speed CMOS Logic BCD-to-7 Segment Latch/Decoder/Driver

clear gif

Features	Samples	Technical Documents
Quality & Pb-Free Data	Pricing/Packaging	Applications Notes
Related Products	Inventory	Simulation Models
Tools & Software	Symbols/Footprints	Reference Designs

Refine Your Selection
- Logic: Decoders/Demu

Support
- KnowledgeBase
- Contact Technical Supp
- TI Cross Reference
- Training
- Part Marking Lookup
- Part Number Nomencla

Datasheet

Download Datasheet

CD54HC4511, CD74HC4511, CD74HCT4511 (Rev. D) (cd74hc4511.pdf, 435 KB)
07 Oct 2003 Download

	CD54HC4511	CD74HC4511
Voltage Nodes(V)	6, 5, 2	
	Samples	Samples
	Inventory	Inventory

Product Information

Features

Save this to your personal library

2-V to 6-V V_{CC} Operation ('HC4511)
4.5-V to 5.5-V V_{CC} Operation (CD74HCT4511)
High-Output Sourcing Capability
- 7.5 mA at 4.5 V (CD74HCT4511)
- 10 mA at 6 V ('HC4511)

Input Latches for BCD Code Storage
Lamp Test and Blanking Capability
Balanced Propagation Delays and Transition Times
Significant Power Reduction Compared to LSTTL Logic ICs
'HC4511
- High Noise Immunity, N_{IL} or N_{IH} = 30% of V_{CC} at V_{CC} = 5 V

CD74HCT4511
Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8 V Maximum, V_{IH} = 2 V Minimum
- CMOS Input Compatibility, I_I 1 µA at V_{OL}, V_{OH}

Description

The CD54HC4511, CD74HC4511, and CD74HCT4511 are BCD-to-7 segment latch/decoder/drivers with four address inputs (D_0–D_3), an active-low blanking (BL)\ input, lamp-test (LT)\ input, and a latch-enable (LE)\ input that, when high, enables the latches to store the BCD inputs. When LE\ is low, the latches are disabled, making the outputs transparent to the BCD inputs.

These devices have standard-size output transistors, but are capable of sourcing (at standard V_{OH} levels) up to 7.5 mA at 4.5 V. The HC types can supply up to 10 mA at 6 V.

Pricing/Packaging/CAD Design Tools/Samples

			Price	Packaging			CAD Design Tools	Samples
Device	Status	Temp (°C)	Budget Price ($US) | QTY	Industry Standard (TI Pkg) | Pins	Top Side Marking	Standard Pack Quantity	Footprints	Samples
CD74HC4511E	ACTIVE	-55 to 125	0.44 | 1KU	PDIP (N) | 16	View	25	☐	Contact TI Distributor or Sales Office
CD74HC4511EE4	ACTIVE	-55 to 125	0.44 | 1KU	PDIP (N) | 16	View	25	☐	Request Free Samples
CD74HC4511M	ACTIVE	-55 to 125	0.44 | 1KU	SOIC (D) | 16	View	40	☐	Contact TI Distributor or Sales Office
CD74HC4511M96	ACTIVE	-55 to 125	0.44 | 1KU	SOIC (D) | 16	View	2500	☐	Purchase Samples
CD74HC4511M96E4	ACTIVE	-55 to 125	0.44 | 1KU	SOIC (D) | 16	View	2500	☐	Purchase Samples
CD74HC4511ME4	ACTIVE	-55 to 125	0.44 | 1KU	SOIC (D) | 16	View	40	☐	Request Free Samples
CD74HC4511MT	ACTIVE	-55 to 125	0.46 | 1KU	SOIC (D) | 16	View	250	☐	Purchase Samples
CD74HC4511MTE4	ACTIVE	-55 to 125	0.46 | 1KU	SOIC (D) | 16	View	250	☐	Purchase Samples
CD74HC4511PWR	ACTIVE	-55 to 125	0.44 | 1KU	TSSOP (PW) | 16	View	2000	☐	Purchase Samples
CD74HC4511PWRE4	ACTIVE	-55 to 125	0.44 | 1KU	TSSOP (PW) | 16	View	2000	☐	Purchase Samples
CD74HC4511PWT	ACTIVE	-55 to 125	0.46 | 1KU	TSSOP (PW) | 16	View	250	☐	Purchase Samples
CD74HC4511PWTE4	ACTIVE	-55 to 125	0.46 | 1KU	TSSOP (PW) | 16	View	250	☐	Purchase Samples

Inventory

View all Distributors

Choose a Region

CD74HC4511E	TI Inventory Status			Reported Distributor Inventory			
	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY | Date	Lead Time	Region	Company	In Stock	Purchase
	600*	1625 | 12 Dec	10 Weeks	Americas	Avnet	483	
		>10k | 16 Jan			DigiKey	969	
					Newark InOne	210	
				Europe	Abacus Polar	>1k	
					Arrow Northern Europe	350	
					Arrow Southern Europe	851	
					Avnet-SILICA	25	
					EBV Elektronik	>1k	

CD74HC4511EE4	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY | Date	Lead Time	Region	Company	In Stock	Purchase
	600*	1625 | 12 Dec	10 Weeks	None Reported View Distributors			
		>10k | 16 Jan					

CD74HC4511M	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY | Date	Lead Time	Region	Company	In Stock	Purchase

	0*	>10k | 24 Jan	10 Weeks	Americas	DigiKey	923	
				Europe	Arrow Southern Europe	263	
					Avnet-SILICA	400	
					Spoerle	>1k	
CD74HC4511M96	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	>10k | 23 Jan	10 Weeks	None Reported View Distributors			
CD74HC4511M96E4	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	>10k | 23 Jan	10 Weeks	None Reported View Distributors			
CD74HC4511ME4	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	>10k | 24 Jan	10 Weeks	None Reported View Distributors			
CD74HC4511MT	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	>10k | 24 Jan	10 Weeks	None Reported View Distributors			
CD74HC4511MTE4	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	>10k | 24 Jan	10 Weeks	None Reported View Distributors			
CD74HC4511PWR	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	2000*	1303 | 30 Nov	12 Weeks	None Reported View Distributors			
		>10k | 3 Apr					
CD74HC4511PWRE4	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	2000*	1303 | 30 Nov	12 Weeks	None Reported View Distributors			
		>10k | 3 Apr					
CD74HC4511PWT	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*		16 Weeks	None Reported View Distributors			
CD74HC4511PWTE4	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*		16 Weeks	None Reported View Distributors			

* Our information is updated daily, so please check back with us soon if this does not meet your needs. You may also contact your TI Authorized Distributor, including those listed above, for real time stock information.

** Lead time information is not available at this time. However, our information is updated daily so please check back with us soon. Please contact your preferred TI Authorized Distributor for additional information.

Quality & Lead (Pb)-Free Data

	Product Content				MTBF/FIT Rate
Device	**Eco Plan***	**Lead/Ball Finish**	**MSL Rating/Peak Reflow**	**Details**	**Details**
CD74HC4511E	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	View	View
CD74HC4511EE4	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	View	View
CD74HC4511M	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4511M96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4511M96E4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4511ME4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4511MT	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4511MTE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4511PWR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4511PWRE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4511PWT	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4511PWTE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View

* The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please click on the Product Content Details "View" link in the table above for the latest availability information and additional product content details.

If the information you are requesting is not available online at this time, contact one of our Product Information Centers regarding the availability of this information.

Technical Documents

Datasheets

Keep track of what's new

CD54HC4511, CD74HC4511, CD74HCT4511 (Rev. D) (cd74hc4511.pdf, 435 KB)
07 Oct 2003 Download

Application Notes

Semiconductor Packing Material Electrostatic Discharge (ESD) Protection (szza047.htm, 9 KB)
08 Jul 2004 Abstract

Shelf-Life Evaluation of Lead-Free Component Finishes (szza046.htm, 9 KB)
24 May 2004 Abstract

Understanding and Interpreting Standard-Logic Data Sheets (Rev. B) (szza036b.htm, 8 KB)
28 May 2003 Abstract

TI IBIS File Creation, Validation, and Distribution Processes (szza034.htm, 9 KB)
29 Aug 2002 Abstract

Selecting the Right Texas Instruments Signal Switch (szza030.htm, 9 KB)
07 Sep 2001 Abstract

Implications of Slow or Floating CMOS Inputs (Rev. C) (scba004c.htm, 9 KB)
01 Feb 1998 Abstract

CMOS Power Consumption and CPD Calculation (Rev. B) (scaa035b.htm, 9 KB)
01 Jun 1997 Abstract

Designing With Logic (Rev. C) (sdya009c.htm, 9 KB)
01 Jun 1997 Abstract

Live Insertion (sdya012.htm, 9 KB)
01 Oct 1996 Abstract

Input and Output Characteristics of Digital Integrated Circuits (sdya010.htm, 9 KB)
01 Oct 1996 Abstract

SN54/74HCT CMOS Logic Family Applications and Restrictions (scla011.htm, 9 KB)
01 May 1996 Abstract

Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc (scla008.htm, 9 KB)
01 Apr 1996 Abstract

View Application Notes for DECODERS/DEMULTIPLEXERS

User Guides

Signal Switch Data Book (Rev. A) (scdd003a.pdf, 19732 KB)
14 Nov 2003 Download

LOGIC Pocket Data Book (scyd013.pdf, 4835 KB)
05 Dec 2002 Download

More Literature

Logic Selection Guide 2005 (Rev. X) (sdyu001x.pdf, 6909 KB)
15 Mar 2005 Download

Military Semiconductors Selection Guide 2004-2005 (Rev. D) (sgyc003d.pdf, 964 KB)
10 Aug 2004 Download

SN74HC4851/HC4852 Product Clip (Rev. B) (scyb019b.pdf, 501 KB)
11 May 2004 Download

Logic Cross-Reference (Rev. A) (scyb017a.pdf, 2938 KB)
07 Oct 2003 Download

View More Literature for DECODERS/DEMULTIPLEXERS