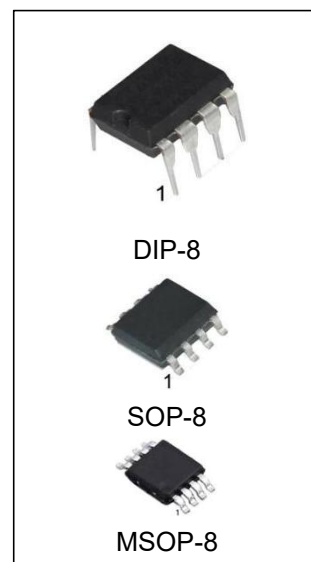


Low Power μ P Supervisor Circuits

Features

- 140 μ A maximum supply current
- Precision power supply monitor
 - 4.40V threshold (MAX706)
 - 3.08V threshold (MAX706T)
 - 2.93V threshold (MAX706S)
 - 2.63V threshold (MAX706R)
- Debounced manual reset input
- Voltage monitor
 - 1.25V threshold
 - Battery monitor/Auxiliary supply monitor
- Watchdog timer (MAX706/MAX706T/MAX706S/MAX706R)
- 300ms reset pulse width
- MicroSOP Package



Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
MAX706N	DIP-8	MAX706	TUBE	2000pcs/box
MAX706TN	DIP-8	MAX706T	TUBE	2000pcs/box
MAX706SN	DIP-8	MAX706S	TUBE	2000pcs/box
MAX706RN	DIP-8	MAX706R	TUBE	2000pcs/box
MAX706M/TR	SOP-8	X706	REEL	2500pcs/reel
MAX706TM/TR	SOP-8	X706T	REEL	2500pcs/reel
MAX706SM/TR	SOP-8	X706S	REEL	2500pcs/reel
MAX706RM/TR	SOP-8	X706R	REEL	2500pcs/reel
MAX706MM/TR	MSOP-8	X706	REEL	3000pcs/reel
MAX706TMM/TR	MSOP-8	X706T	REEL	3000pcs/reel
MAX706SMM/TR	MSOP-8	X706S	REEL	3000pcs/reel
MAX706RMM/TR	MSOP-8	X706R	REEL	3000pcs/reel

General Description

The MAX706/MAX706T/MAX706S/MAX706R CMOS supervisor circuits monitor powersupply and battery voltage level, and $\mu\text{P}/\mu\text{C}$ operation. Compared to pin-compatible devices offered by Maxim Integrated Products, these devices feature 60 percent lower maximum supply current.

The family offers several functional options. Each device generates a reset signal during power-up, power-down and during brownout conditions.

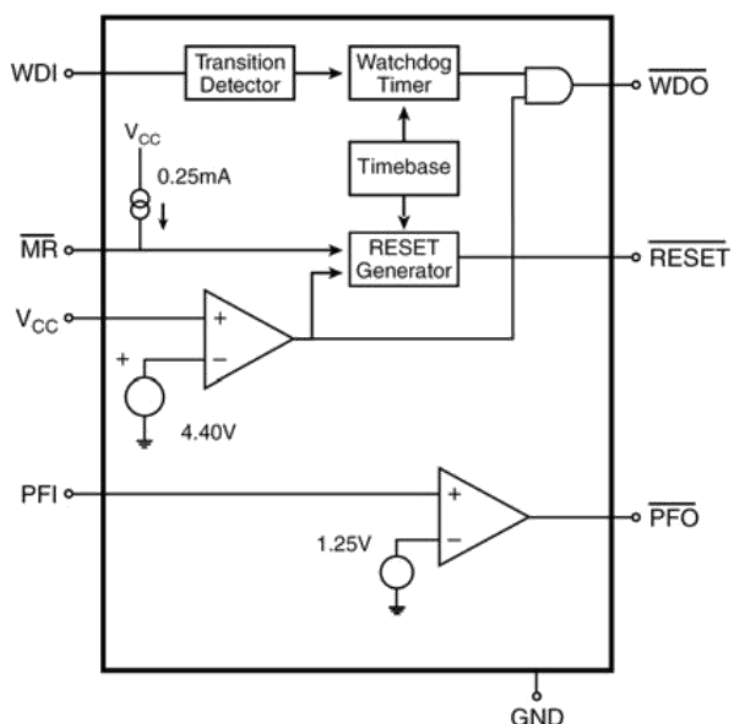
A reset is generated when the supply drops below 4.4V (MAX706), 3.08V(MAX706T), 2.93V(MAX706S), 2.63V(MAX706R).In addition,the MAX706/MAX706T/MAX706S/MAX706R feature a 1.6 second watchdog timer. A versatile power-fail circuit has a1.25V threshold, useful in checking battery levels and non-5V supplies. All devices have a manual reset ($\overline{\text{MR}}$) input. The watchdog timer output will trigger a reset if connected to $\overline{\text{MR}}$.

All devices are available in DIP-8, SOP-8 and MSOP-8 packages

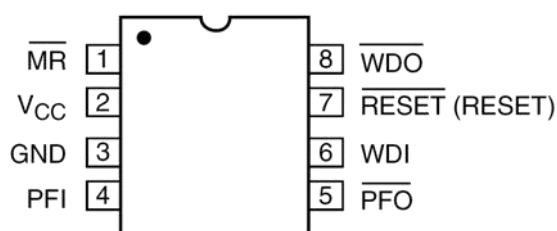
Application

- Computers and embedded controllers
- Battery-operated systems
- Intelligent instruments
- Wireless communication systems
- PDAs and handheld equipment

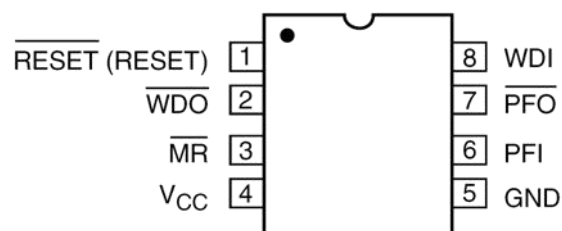
Block Diagram



Pin Configuration



DIP-8/SOP-8



MSOP-8

Pin Description

Pin No.		Name	Pin Function
MAX706/MAX706T/MAX706S/MAX706R			
DIP-8/SOP-8	MSOP-8		
1	3	$\overline{\text{MR}}$	Manual RESET input. The active LOW input triggers a reset pulse. A 250 μA pull-up current allows the pin to be driven by TTL / CMOS logic or shorted to ground with a switch.
2	4	Vcc	+5V power supply input.
3	5	GND	Ground reference for all signals.
4	6	PFI	Power-fail voltage monitor input. With PFI less than 1.25V, $\overline{\text{PFO}}$ goes low. Connect PFI to ground or Vcc when not used.
5	7	$\overline{\text{PFO}}$	Power-fail output. The output is active LOW and sinks current when PFI is less than 1.25V.
6	8	WDI	Watchdog input. WDI controls the internal watchdog timer. A HIGH or LOW signal for 2.4sec at WDI allows the internal timer to run-out, setting $\overline{\text{WDO}}$ LOW. The watchdog function is disabled by floating WDI or by connecting WDI to a high-impedance Three-state buffer. The internal watchdog timer clears when: $\overline{\text{RESET}}$ is asserted; WDI is three- stated; or WDI sees a rising or falling edge.
7	1	$\overline{\text{RESET}}$	Active-LOW reset output. Pulses LOW for 300ms when triggered, and stays low whenever Vcc is below the reset threshold (MAX706: 4.4V, MAX706T: 3.08V, MAX706S: 2.93 V). $\overline{\text{RESET}}$ remains LOW for 300ms after Vcc rises above the $\overline{\text{RESET}}$ threshold or MR goes from LOW to HIGH. A watchdog timeout will not trigger $\overline{\text{RESET}}$ unless $\overline{\text{WDO}}$ is connected to MR .
8	2	$\overline{\text{WDO}}$	Watchdog output. $\overline{\text{WDO}}$ pulls LOW when the 1.6 sec internal watchdog timer times-out and does not go HIGH until the watchdog is cleared. In addition, when Vcc is below the reset threshold, $\overline{\text{WDO}}$ remains low. Unlike $\overline{\text{RESET}}$, $\overline{\text{WDO}}$ does not have a minimum pulse width and as soon as Vcc exceeds the reset threshold, $\overline{\text{WDO}}$ goes HIGH with no delay.

Absolute Maximum Ratings (Ta=25 °C)^{*1}

Characteristics	Value	Unit
Supply voltage	-0.3 ~ +6.0	V
All other inputs ^{*2}	-0.3 ~ Vcc+0.3	V
Input current at Vcc and GND	20	mA
Output current :All outputs	20	mA
Rate of Rise at Vcc	100	V/μs
Plastic DIP-8 power dissipation (Derate 9mW/ °C above 70 °C)	700	mW
SOP-8 power dissipation (Derate 5.9mW/ °C above 70 °C)	470	mW
MSOP-8 power dissipation (Derate 4.1mW/ °C above 70 °C)	330	mW
Operating temperature range	-40 ~ +125	°C
Storage temperature range	-55 ~ +150	°C
Lead temperature (soldering, 10 sec.)	260	°C

Note: *1、 Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured.

*2. The input voltage limits on PFI and \overline{MR} can be exceeded if the input current is less than 10mA

Electrical Characteristics

(Unless otherwise noted, $V_{CC} = 4.5V$ to $5.5V$ for the MAX706/MAX706T/MAX706S/MAX706R)

Characteristics	Symbol	Conditions	Min.	Typ.	Max	Unit
Operating voltage range	V_{CC}	MAX706/T/S/R	1.2		5.5	V
Supply current	I_{CC}	MAX706/T/S/R		75	140	μA
\overline{RESET} threshold	V_{RT}	MAX706	4.25	4.4	4.5	V
		MAX706T	3.00	3.08	3.15	
		MAX706S	2.85	2.93	3.00	
		MAX706R	2.55	2.63	2.70	
\overline{RESET} threshold hysteresis				40		mV
\overline{RESET} pulse width	t_{RS}		140	200	280	ms
\overline{MR} pulse width	t_{MR}		0.15			μs
\overline{MR} to \overline{RESET} out delay	t_{MD}				0.25	μs
\overline{MR} input threshold	V_{IH}		2.0			V
	V_{IL}				0.8	
\overline{MR} pull-up current		$MR = 0V$	100	250	600	μA
\overline{RESET} output voltage		$I_{SOURCE} = 800\mu A$	$V_{CC}-1.5$			V
		$I_{SINK} = 3.2mA$			0.4	
		MAX706/T/S/R, $V_{CC}=1.2V$, $I_{SINK} = 100\mu A$			0.3	
Watchdog timeout period	t_{WD}	MAX706 / T/ S	1.00	1.60	2.25	s
WDI pulse width	t_{WP}	$V_{IL} = 0.4V, V_{IH} = 0.8V_{CC}$	50			ns
WDI input threshold	V_{IH}	MAX706/ T/S/R , $V_{CC}=5V$	3.5			V
	V_{IL}				0.8	
WDI input current		MAX706 / T/ S/R, $WDI=V_{CC}$		50	150	μA
		MAX706 / T/ S/R, $WDI=0V$	- 150	- 50		
\overline{WDO} output voltage		MAX706/T/S/R, $I_{SOURCE} = 800\mu A$	$V_{CC}-1.5$			V
		MAX706/ T/ S/R, $I_{SINK} = 1.2mA$			0.4	
PFI input threshold		$V_{CC}=5V$	1.20	1.25	1.30	V
PFI input current			-25	0.01	25	nA
\overline{PFO} output voltage		$I_{SOURCE} = 800\mu A$	$V_{CC}-1.5$			V
		$I_{SINK} = 3.2mA$			0.4	

Features Summary

Characteristics	MAX706	MAX706T	MAX706S	MAX706R
Power-fail detector	•	•	•	•
Brownout detection	•	•	•	•
Manual RESET input	•	•	•	•
Power- up/down RESET	•	•	•	•
Watchdog timer	•	•	•	•
Active-HIGH RESET output				
Active-LOW RESET output	•	•	•	•
RESET threshold	4.4V	3.08V	2.93V	2.63V

Detail Descriptions

RESET Operation

The RESET signals are designed to start a $\mu\text{P}/\mu\text{C}$ in a known state or return the system to a known state.

RESET is guaranteed to be LOW with V_{CC} above 1.2V. During a power-up sequence,

RESET remains low until the supply rises above the threshold level, either 4.4V, 3.08V, 2.93V. RESET goes high approximately 200ms after crossing the threshold.

During power-down, RESET goes LOW as V_{CC} falls below the threshold level and is guaranteed to be under 0.4V with V_{CC} above 1.2V.

In a brownout situation where V_{CC} falls below the threshold level, RESET pulses low. If a brownout occurs during an already initiated reset, the pulse will continue for a minimum of 140ms

Auxiliary Comparator

All devices have an auxiliary comparator with 1.25V trip point and uncommitted output ($\overline{\text{PFO}}$) and noninverting input (PFI). This comparator can be used as a supply voltage monitor with an external resistor voltage divider. The attenuated voltage at PFI should be set just below the 1.25 threshold. As the supply level falls, PFI is reduced causing the $\overline{\text{PFO}}$ output to transit LOW. Normally $\overline{\text{PFO}}$ interrupts the processor so the system can be shut down in a controlled manner.

Manual Reset ($\overline{\text{MR}}$)

The active-LOW manual reset input is pulled high by a 250 μA pull-up current and can be driven low by CMOS/TTL logic or a mechanical switch to ground. An external debounce circuit is unnecessary since the 140ms minimum reset time will debounce mechanical pushbutton switches.

By connecting the watchdog output ($\overline{\text{WDO}}$) and $\overline{\text{MR}}$, a watchdog timeout forces RESET to be generated.

Watchdog Timer

The watchdog timer available on the MAX706/MAX706T/MAX706S/MAX706R monitors $\mu\text{P}/\mu\text{C}$ activity. If activity is not detected within 1.6 seconds, the internal timer puts the watchdog output, $\overline{\text{WDO}}$, into a LOW state. $\overline{\text{WDO}}$ will remain LOW until activity is detected at WDI.

The watchdog function is disabled, meaning it is cleared and not counting, if WDI is floated or connected to a three-stated circuit. The watchdog timer is also disabled if $\overline{\text{RESET}}$ is asserted. When $\overline{\text{RESET}}$ becomes inactive and the WDI input sees a high or low transition as short as 50ns, the watchdog timer will begin a 1.6 second countdown.

Additional transitions at WDI will reset the watchdog timer and initiate a new countdown sequence.

$\overline{\text{WDO}}$ will also become $\overline{\text{LOW}}$ and remain so, whenever the supply voltage, V_{CC} , falls below the device threshold level. $\overline{\text{WDO}}$ goes HIGH as soon as V_{CC} transitions above the threshold. There is no minimum pulse width for WDO as there is for the $\overline{\text{RESET}}$ outputs. If WDI is floated, WDO essentially acts as a low-power output indicator.

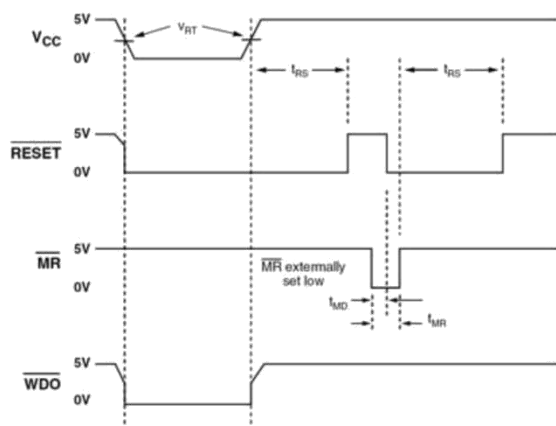


Figure 1. WDI Three-state operation

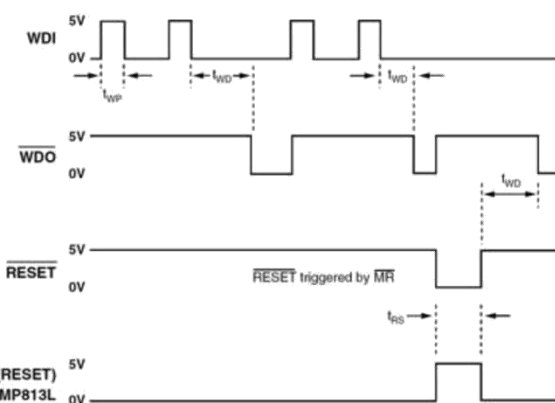


Figure 2. Watchdog Timing

Application Information

Ensuring That $\overline{\text{RESET}}$ is Valid Down to $V_{CC} = 0V$

When V_{CC} falls below 1.1V, the MAX706/MAX706T/MAX706S/MAX706R $\overline{\text{RESET}}$ output no longer pulls down; it becomes indeterminate. To avoid the possibility that stray charges build up and force $\overline{\text{RESET}}$ to the wrong state, a pull-down resistor should be connected to the $\overline{\text{RESET}}$ pin, thus draining such charges to ground and holding RESET low. The resistor value is not critical. A 100k Ω resistor will pull $\overline{\text{RESET}}$ to ground without loading it.

Bi-directional Reset Pin Interfacing

The MAX706/MAX706T/MAX706S/MAX706R can interface with $\mu P/\mu C$ bi-directional reset pins by connecting a 4.7k Ω resistor in series with the $\overline{\text{RESET}}$ output $\mu P/\mu C$ bi-directional $\overline{\text{RESET}}$ pin.

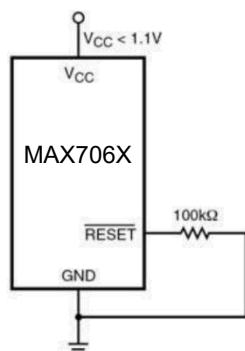


Figure 3. Ensuring That $\overline{\text{RESET}}$ is Valid Down to $V_{CC} = 0V$

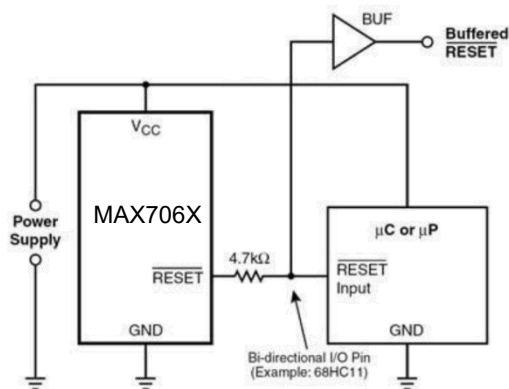


Figure 3. Bi-directional Reset Pin Interfacing

Monitoring Voltages Other Than Vcc

The MAX706/MAX706T/MAX706S/MAX706R can monitor voltages other than V_{CC} using the Power Fail circuitry. If a resistive divider is connected from the voltage to be monitored to the power Fail input, PFI, the $\overline{\text{PFO}}$ (output) will go LOW if the divider voltage goes below its 1.25V reference. Should hysteresis be desired, connect a resistor (equal to approximately 10 times the sum of the two resistors in the divider) between the PFI and $\overline{\text{PFO}}$ pins. A capacitor between PFI and GND will reduce circuit sensitivity to input high-frequency noise. If it is desired to assert a RESET in addition to the $\overline{\text{PFO}}$ flag, this may be achieved by connecting the $\overline{\text{PFO}}$ output to MR.

Monitoring a Negative Voltage

The Power-Fail circuitry can also monitor a negative supply rail. When the negative rail is OK, $\overline{\text{PFO}}$ will be LOW, and when the negative rail is failing (not negative enough), $\overline{\text{PFO}}$ goes HIGH (the opposite of when positive voltages are monitored). To trigger a reset, these outputs need to be inverted: adding the resistors and transistor as shown achieves this. The $\overline{\text{RESET}}$ output will then have the same sense as for positive voltages: good = HIGH, bad = LOW. It should be noted that this circuit's accuracy depends on the V_{CC} line, the PFI threshold tolerance, and the resistors.

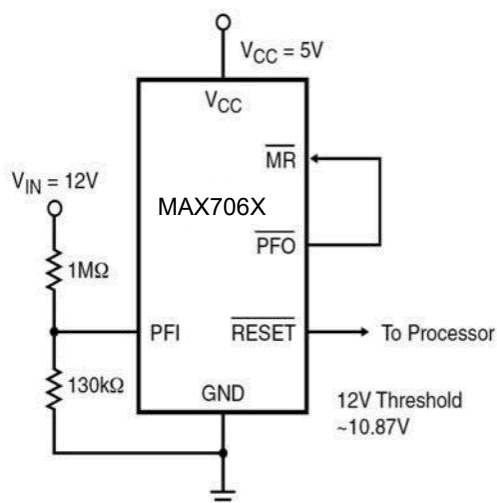


Figure 4. Monitoring Voltages Other Than V_{CC}

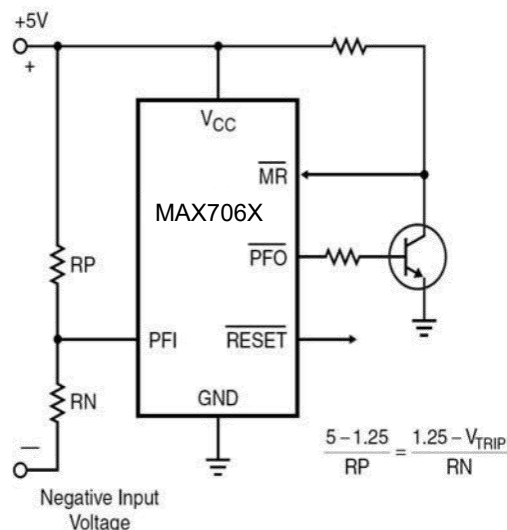
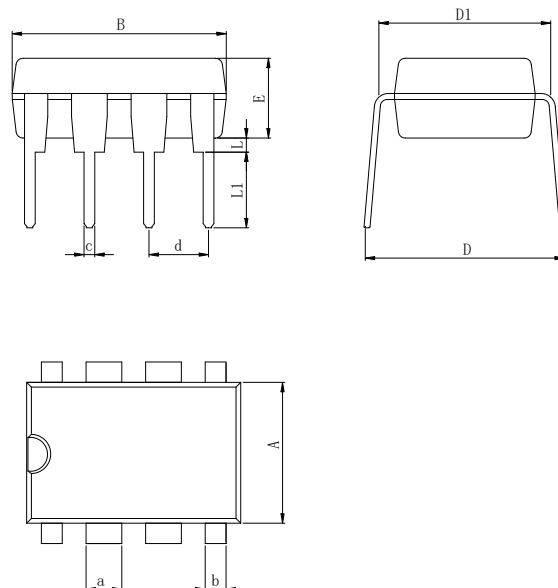


Figure 5. Monitoring a Negative Voltage

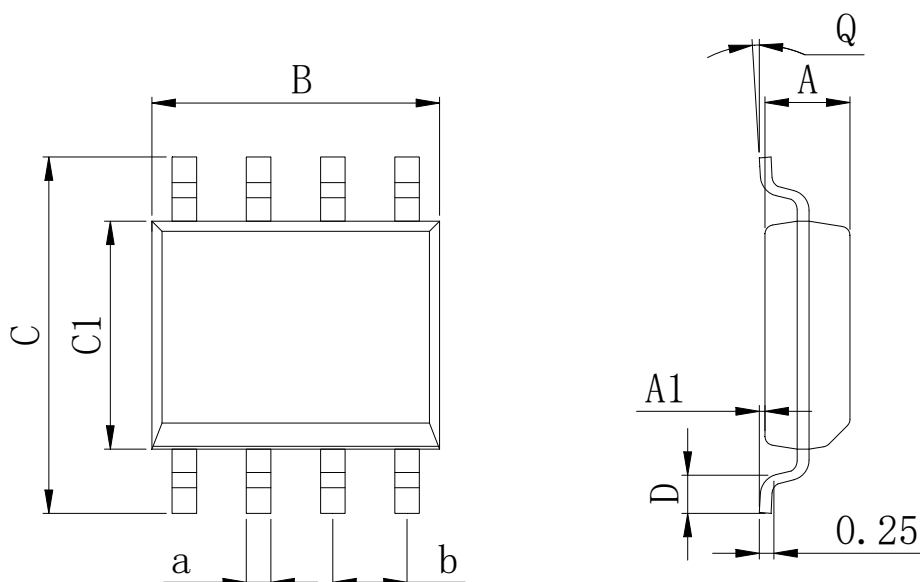
Physical Dimensions

DIP-8



Dimensions In Millimeters(DIP-8)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	9.00	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	9.50	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

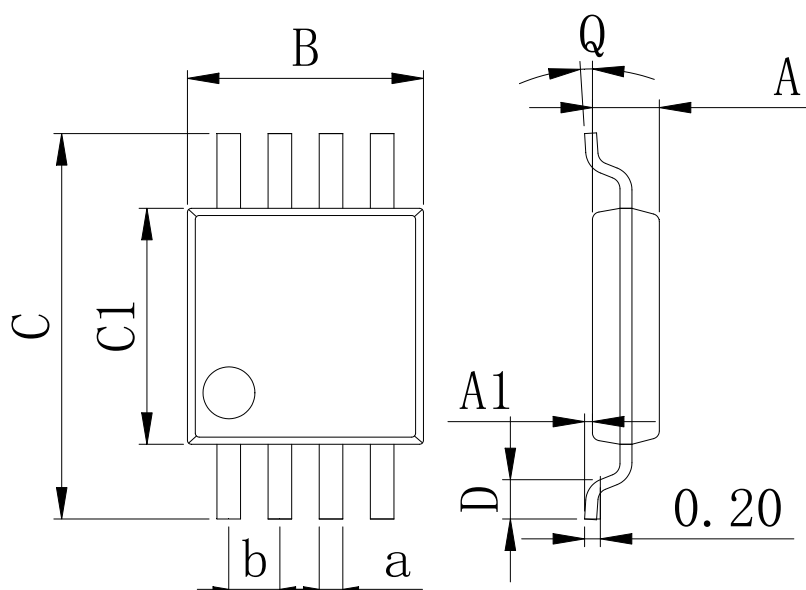
SOP-8 (150mil)



Dimensions In Millimeters(SOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

Physical Dimensions

MSOP-8



Dimensions In Millimeters(MSOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.80	0.05	2.90	4.75	2.90	0.35	0°	0.25	0.65 BSC
Max:	0.90	0.20	3.10	5.05	3.10	0.75	8°	0.35	

Revision History

DATE	REVISION	PAGE
2015-6-6	New	1-12

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