Rochester Electronics

Datasheet

PART NUMBER

95016DCB-ROCV

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
  - Class Q Military
  - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

F95010 • F95016

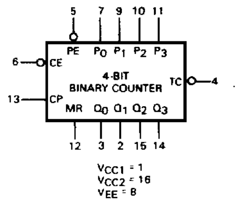
BCD DECADE COUNTER/4-BIT BINARY COUNTER

GENERAL DESCRIPTION — The F95010 is a high speed synchronous, presettable, cascadable BCD Decade Counter and the F95016 is a high speed synchronous, presettable, cascadable 4-Bit Binary Counter. They are multifunction MSI building blocks useful for a large number of counting, digital integration, and conversion applications. Up to nine devices can be cascaded with no speed degradation using standard 95K gates. A multidecade synchronous counter up to 150 MHz can be built. Typical count frequency is 200 MHz.

Features include assertion inputs and outputs on each of the four master/slave counting flip-flops. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter.

- HIGH SPEED COUNT . . . 200 MHz TYPICAL COUNT FREQUENCY
- INTERNAL COUNT ENABLE — FOR HIGHEST SPEED EXPANSION
- ASYNCHRONOUS MASTER RESET
- 50Ω DRIVE CAPABILITY
- WIRED-OR CAPABILITY
- SEPARATE V_{CC} PINS — ELIMINATE NOISE COUPLING
- INTERNAL 50 kΩ INPUT PULL DOWNS
- SINGLE -5.2 V POWER SUPPLY

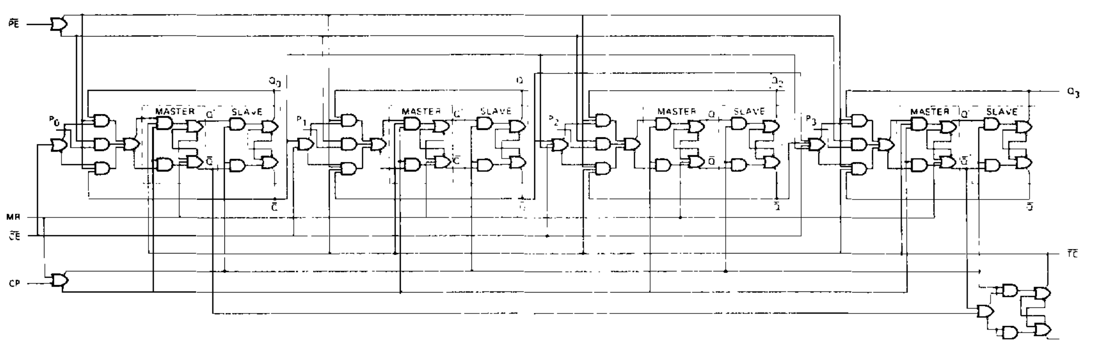
LOGIC SYMBOL



PIN NAMES

$\overline{PE}$	Parallel Load Enable (Active LOW)
P_n	Parallel Inputs
CP	Clock Input (Clocks on Positive Transition)
$\overline{CE}$	Count Enable (LOW to Count)
MR	Master Reset (HIGH Forces all Q Outputs LOW)
$\overline{TC}$	Terminal Count (95010, LOW at HLLH; 95016 LOW at HHHH)
Q_n	Counter Outputs

LOGIC DIAGRAM F95010



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

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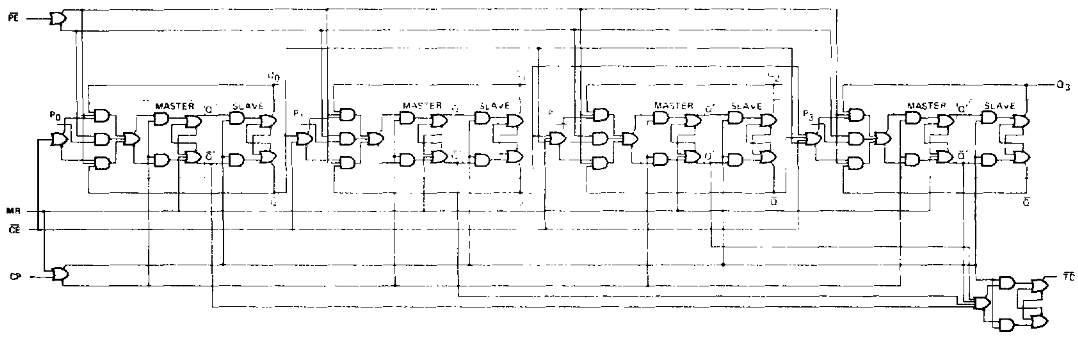
LOGIC DIAGRAM F95016



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

FUNCTIONAL DESCRIPTION — The F95010 is a high speed BCD Decade Counter and the F95016 is a high speed Binary Counter. The four master/slave flip-flops are fully synchronous and are driven in parallel through a clock driver. The masters are loaded during the LOW period of the clock pulse. During the LOW to HIGH transition of the clock, the master is disabled from the input and data is transferred to the slaves and then to the outputs. When the clock is HIGH, the masters are inhibited from changing and the master/slave data path remains open. During the HIGH to LOW transition of the clock, the master/slave data path is inhibited, followed by the enabling of the masters for the acceptance of inputs from the counting logic, parallel entry, or count hold logic.

The Terminal Count ($\overline{TC}$) is generated at count 9 (HLLH) on the 95010 and at count 15 (HHHH) on the 95016.

The $\overline{TC}$ output is available simultaneously with the Q outputs through the use of unique lookahead logic and a fifth slave which is loaded during the LOW portion of the clock cycle. This feature, in conjunction with the triggered Count Enable ($\overline{CE}$) and the Parallel Enable ($\overline{PE}$) select the mode of operation as shown in the table below. The status of these control lines is sampled only during the LOW to HIGH transition of the clock.

The Master Reset (MR) function is asynchronous. When HIGH, it overrides all other commands and forces all Q outputs LOW and the $\overline{TC}$ HIGH.

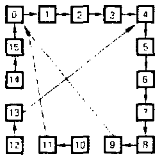
TRUTH TABLE

$\overline{CE}$	$\overline{PE}$	MR	CP	Function
L	L	L	↑	Load Parallel (P_n to Q_n)
H	L	L	↑	Load Parallel (P_n to Q_n)
L	H	L	↑	Count
H	H	L	↑	Hold
X	X	L	↓	Masters Respond, Slaves Hold
X	X	H	X	Reset (Q_n = LOW, $\overline{TC}$ = HIGH)

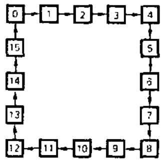
L = LOW
H = HIGH Voltage Level
X = Don't Care
↑ = Clock Pulse (LOW to HIGH)
↓ = Clock Pulse (HIGH to LOW)

STATE DIAGRAMS

F95010



F95016



NOTE: The 95010 can be preset to any state, but will not count beyond 9 (HLLH). If preset to state 10, 11, 12, 13, 14 or 15, it will return to its normal sequence within two clock pulses.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE: V_{EE} = -5.2 V, T_A = 0°C to 75°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OH}	Output Voltage HIGH	-1025	-965	880	mV	50 Ω to -2.0 V	V_{IN} = V_{IHA} or V_{ILB} per Truth Table
V_{OL}	Output Voltage LOW	-1810	-1705	-1620	mV	50 Ω to -2.0 V	
V_{OHC}	Output Voltage HIGH	-1035			mV	50 Ω to -2.0 V	V_{IN} = V_{IHB} or V_{ILA} per Truth Table
V_{OLC}	Output Voltage LOW			-1610	mV	50 Ω to -2.0 V	
V_{IH}	Input Voltage HIGH	-1165		-880	mV	Guaranteed Input HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1810		-1475	mV	Guaranteed Input LOW for All Inputs	
I_{IH}	Input Current HIGH, MR (Pin 12)			265 700	μA μA	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW	0.5			μA	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current	-115	-80		mA	MR to V_{IH}, Other Inputs and Outputs Open	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 25°C, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
f_{count}	Count Frequency	140	200		MHz	See Figure 1
t_{PLH}	Propagation Delay Clock to Output (Q_n or $\overline{TC}$)	2.0	3.6	5.0	ns	See Figure 2
t_{PHL}	Propagation Delay Clock to Output (Q_n or $\overline{TC}$)	2.0	3.6	5.0	ns	
t_{PHL}	Propagation Delay Master Reset to Output		4.0		ns	See Figure 3
T_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.3	2.5	3.3	ns	See Figure 2
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.3	2.5	3.3	ns	
t_w	Clock Pulse Width		2.3		ns	See Figure 2
t_w	MR Pulse Width		2.8		ns	See Figure 3
t_s	Set-Up Time Prior to Clock P_n to CP	2.0			ns	
t_s	Set-Up Time Prior to Clock $\overline{PE}$ or $\overline{CE}$ to CP	2.5			ns	
t_h	Hold Time After Clock $\overline{PE}$ or $\overline{CE}$ to CP	0.5			ns	

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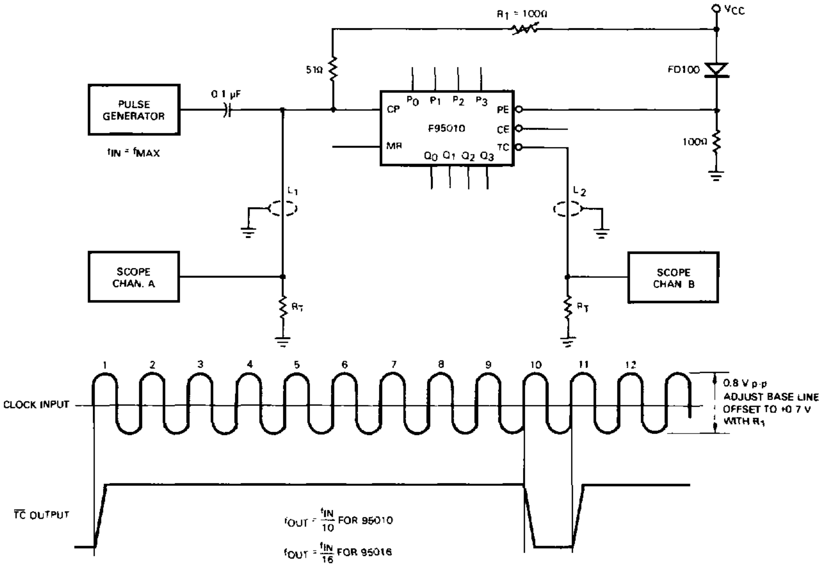
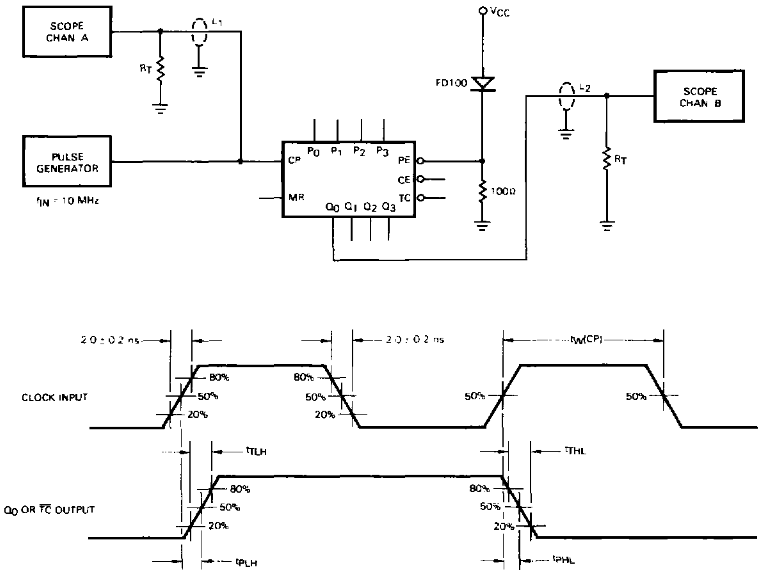
SWITCHING CIRCUITS AND WAVEFORMS



L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF

Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 1. Maximum Count Frequency

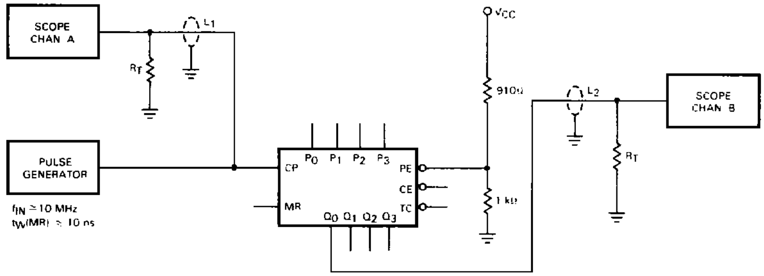


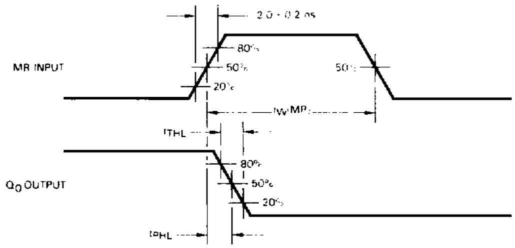
L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance <5.0 pF

Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 2. Clock to Output

SWITCHING CIRCUITS AND WAVEFORMS (Cont'd.)



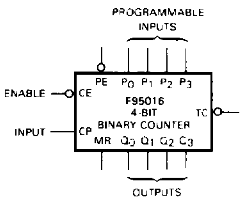


L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF

Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

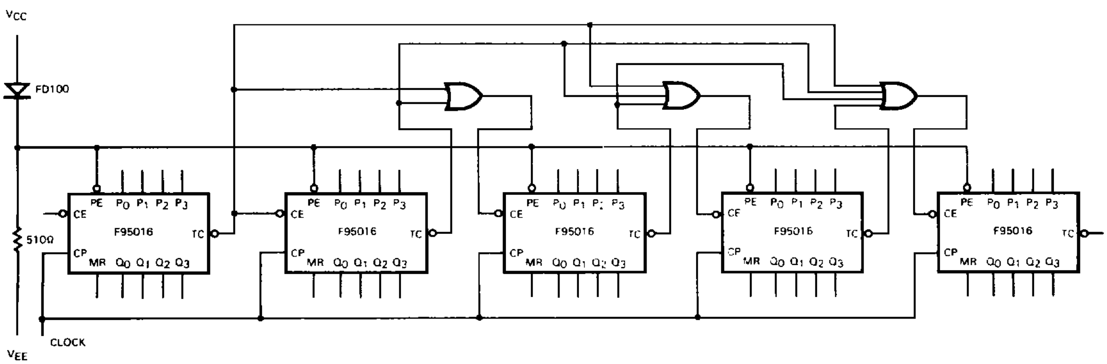
Fig. 3. **Master Reset to Output**

APPLICATION INFORMATION



DIVIDE RATIO	INPUT REQUIRED P_0	P_1	P_2	P_3
2	L	H	H	H
3	H	L	H	H
4	L	L	H	H
5	H	H	L	H
6	L	H	L	H
7	H	L	L	H
8	L	L	L	H
9	H	H	H	L
10	L	H	H	L
11	H	L	H	L
12	L	L	H	L
13	H	H	L	L
14	L	H	L	L
15	H	L	L	L
16	L	L	L	L

The F95016 may be connected to divide by any modulo from 2 to 16. The table illustrates the inputs required for each modulo. The terminal count output is utilized to load the parallel data, this in turn determines the number of clock pulses which will occur before $\overline{TC}$ goes LOW again.



CASCADE COUNTERS USING OR GATES FOR CARRY PROPAGATION