RELIABILITY REPORT

FOR

MAX2507ELM

PLASTIC ENCAPSULATED DEVICES

March 28, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Quality Assurance
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Conclusion

The MAX2507 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX250_ series of complete transmitters are designed for low-cost cellular applications. The minia-ture 7mm x 7mm transmitter includes a quadraturemodulator, upconverters, drivers, power amplifiers(PAs), a peak detector, a monolithic voltage-controlledoscillator (VCO), and a PLL. Each transmitter is tailoredfor specific frequency bands according to the SelectorGuide. The MAX2500/MAX2502/MAX2503/MAX2504/MAX2504A/MAX2506/MAX2507 are compatible withvoltage-mode baseband interfaces.

The devices are based on quasi-direct I/Q modulation.The devices accept differential I/Q baseband inputs,which are upconverted to IF. The IF signal is thenupconverted to the RF frequency. Each signal is thenfed into separate on-chip PAs through external RF fil-ters. PA matching is integrated onto the chip to furtherreduce external component count. These chips featurean on-chip VCO and synthesizer to generate LO signalsfor both the IF and RF sections.

The MAX250_ devices are programmed with anSPI/MICROWIRE-compatible 3-wire serial bus. Thesedevices feature multiple modes of operation, includingshutdown, idle, high power, and low power, for flexiblepower management. To further reduce the current con-sumption, the PA supply voltage can be reduced to aslow as 0.5V at lower output powers. The devices operatefrom single 2.7V to 3.3V regulated supplies and are pack-aged in a small 7mm x 7mm, 48-lead LGA package.

B. Absolute Maximum Ratings

Item	Rating
VCCTXBIAS, VCCVCO, VCCCP, VCCPLL to GND	-0.3V to +3.6V
VCCDRV_, VCCPAB, VCC1_, VCCPA, VCCMOD, VCCAUX to GND	-0.3V to +4.5V
DET_OUT, PA_OUT, OUT_, PA_INL, Q_, I_ to GND	-0.3V to (VBATT + 0.3V)
All Other Pins to GND	-0.3V to (VREG_ + 0.3V)
PA_INH, NOISE_FILT, OUT_DRV_ Input Current	±10mA
Digital Input Current	±10mA
Maximum VSWR without Damage (Note 1)	4:1
Maximum VSWR without Oscillation (Notes 1)	4:1
Continuous Power Dissipation (TA = +70°C)	
48-Lead LGA (derate 28.5mW/°C above +70°C)	2.3W
Theta JC	16°C/W
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+240°C

Note 1: VGC ≤ level to provide 28dBm (PCS) or 28dBm (cellular) into 50Ω load. VBATT = 3.45V (PCS), VBATT = 3.35V (cell).
Note 2: VGC ≤ level to provide 28dBm (TDSCDMA). VBATT = 4.2V.

II. Manufacturing Information

A. Description/Function:	Complete Cellular Baseband-to-RF Transmitters with PA
B. Process:	GST4
C. Number of Device Transistors:	18,805
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia
F. Date of Initial Production:	October, 2005

III. Packaging Information

A. Package Type:	**48-Pin LGA**
B. Lead Frame:	N/A
C. Lead Finish:	Gold
D. Die Attach:	N/A
E. Bondwire:	N/A
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-9000-1323
H. Flammability Rating:	Class: UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 3

IV. Die Information

A. Dimensions:	116 x 136 mils
B. Passivation:	Si_3N_4 (Silicon nitride)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1: 1.2; Metal2: 1.2; Metal3: 1.2; Metal4: 5.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1: 1.6; Metal2: 1.6; Metal3: 1.6; Metal4: 4.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9706 \times 120 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 4.10 \times 10^{-8}$ λ = 4.10 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-7110) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Reports (**RR-1M** & **RR-B3A**). Current monitor data for the GST4 Process results in a FIT Rate of 0.10 @ 25C and 1.70 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The WC32 die type has been found to have all pins able to withstand a transient pulse of <+/-500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX2507ELM

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	120	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic process/package data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

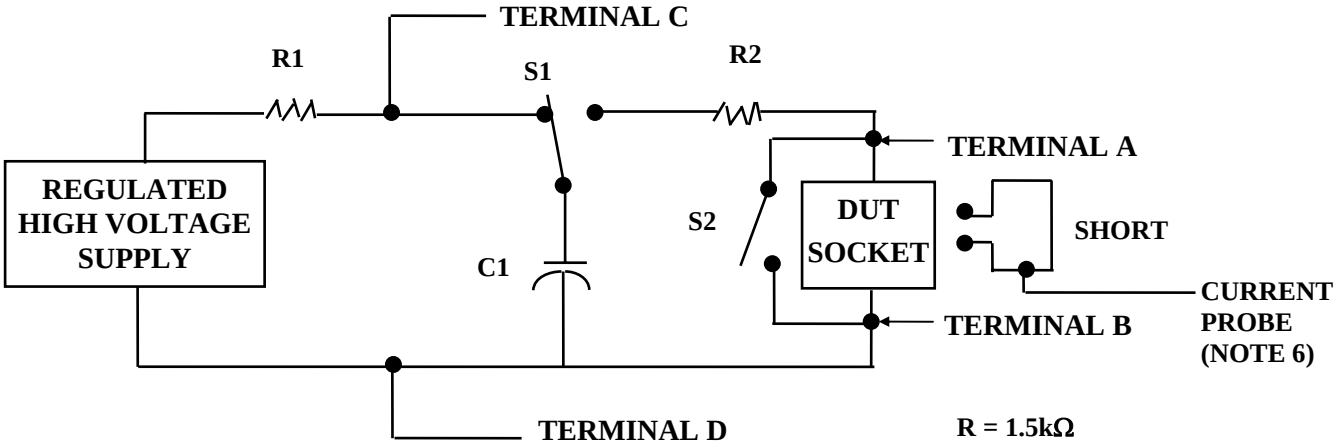
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

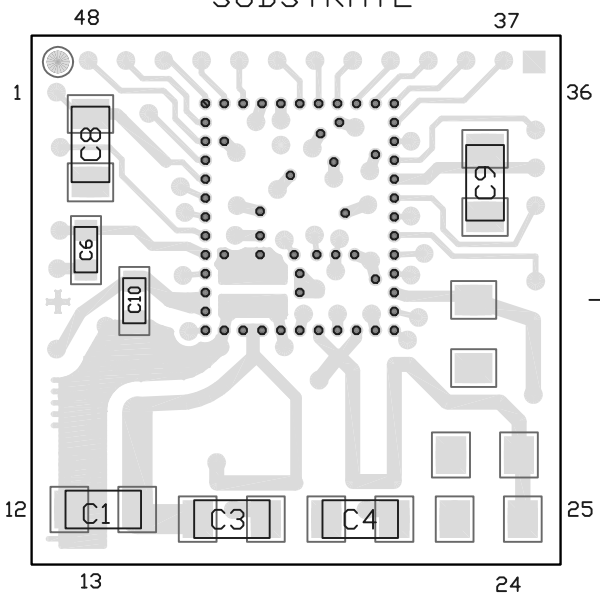


Mil Std 883D
Method 3015.7
Notice 8

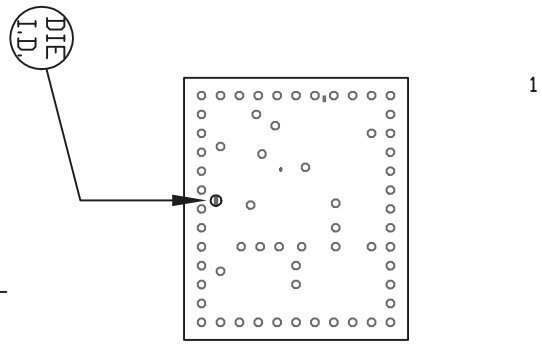
7x7x1.4 MM LGA, FLIP CHIP SIP PKG. SCALE: 10x

FLIP LINE

SUBSTRATE

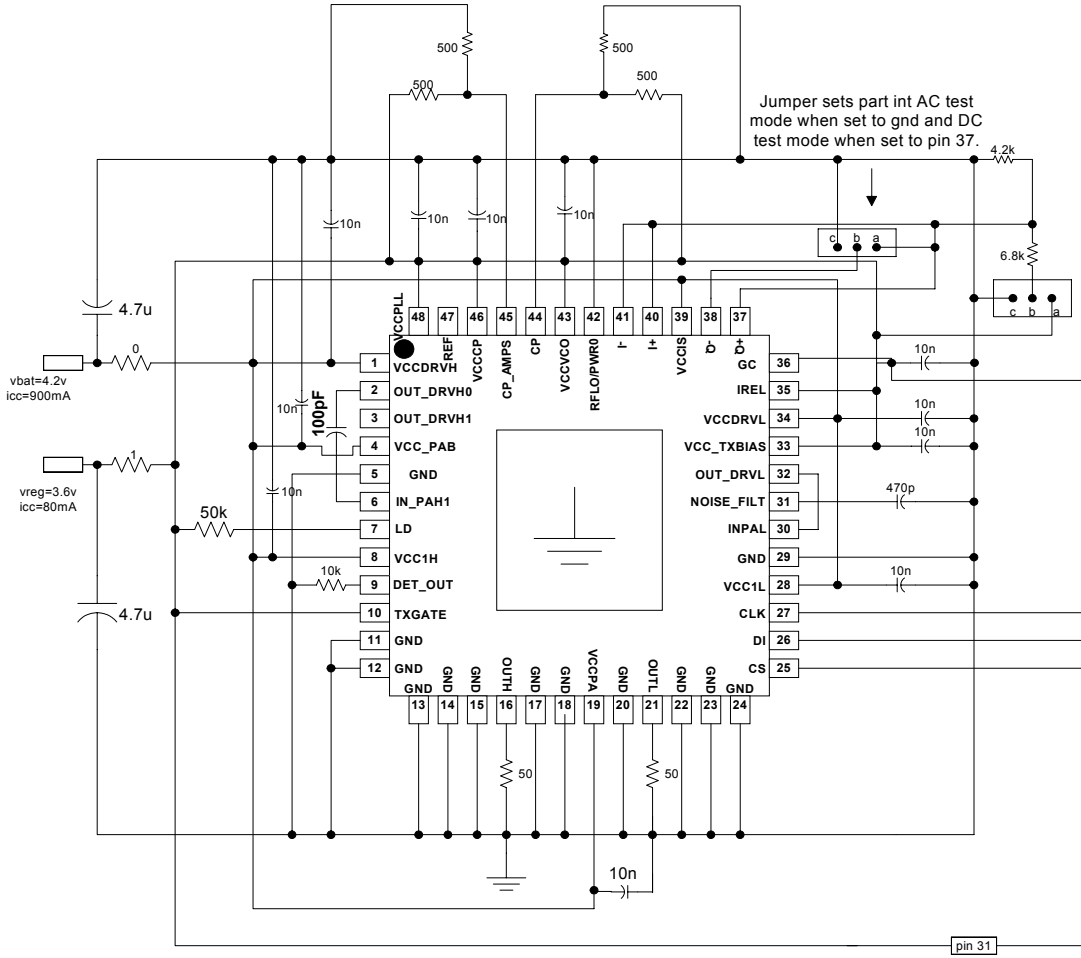


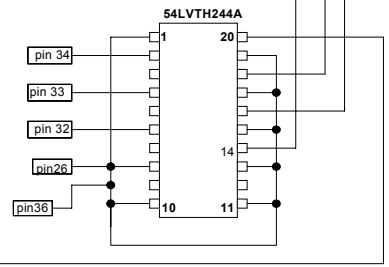
DIE



PKG. CODE: L4877A-3		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: --	PKG.			BOND DIAGRAM #: 05-9000-1323	REV: F
	DESIGN				

ONCE PER SOCKET





ONCE PER BOARD

Jumper settings

mode	jumper to pin 38, jumper to 6.8k resistor		finger 18 on bib
max2500/04/07/09			
dc mode	A-->B	A-->B	float
max2501/14/19			
dc mode	A-->B	C-->B	float
max2500/04/07/09			servo to adjust
ac mode	B-->C	A-->B	Icc
max2501/14/19			servo to adjust
ac mode	B-->C	C-->B	Icc

DEVICES: MAX 2500
PACKAGE: 48-LGA 7X7
MAX. EXPECTED CURRENT = 800mA