



CYPRESS

PRELIMINARY

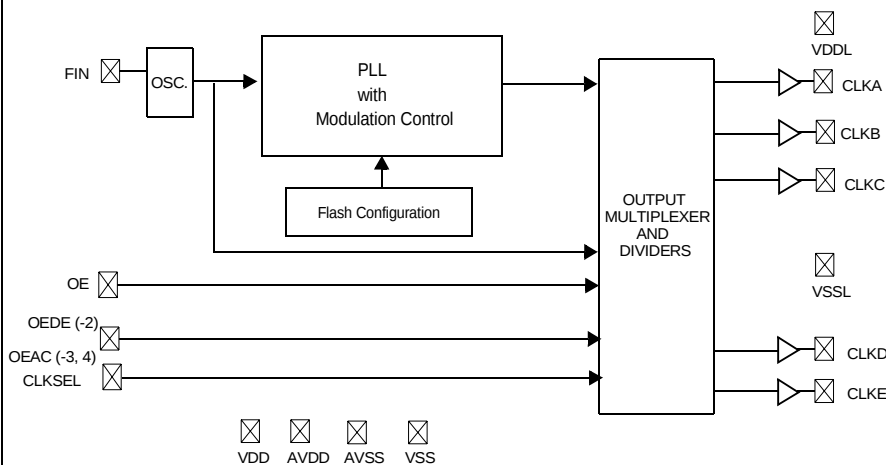
CY28507

PowerPC® Spread Spectrum Clock Generator

Features

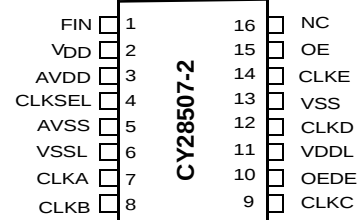
- Integrated phase-locked loop (PLL)
- Low jitter, high-accuracy outputs
- 3.3V operation
- 100-MHz input frequency
- 100-MHz or 66-MHz output frequency
- 1% Downspread Spread Spectrum on -2 and -3 with 30-kHz nominal modulation frequency
- Global output enable
- Separate enable for two clocks
- Meets critical timing requirements in complex system design

Block Diagram

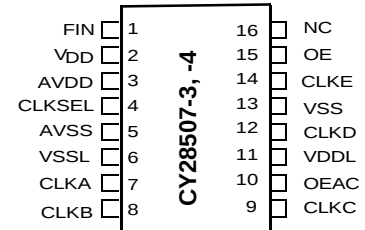


Pin Configuration

CY28507 16-pin TSSOP



CY28507 16-pin TSSOP



Frequency Table for CLKA-E

CLKSEL	CLKA-E
0	66.6 MHz
1	100.0 MHz

Pin Description

Pin Number	Pin Name	I/O	Pin Description
1	FIN		Reference input
2	VDD		3.3V voltage supply
3	AVDD		3.3V analog voltage
4	CLKSEL		1 = 100 MHz out, 0 = 66.6 MHz out. Weak pull-up.
5	AVSS		Analog ground
6	VSSL		CLK ground
7,8,9,12	CLK(A:D)		Clock outputs at VDDL level
14	CLKE		Clock output at VDD level
15	OE		Output enable for all clocks. Weak pull-up. 0 = High-Z, 1 = Active
10	OEDE (-2)		Output enable for CLKD and CLKE. Weak pull-up. 0 = outputs driven high, 1 = Active
10	OEAC (-3,-4)		Output enable for CLKA and CLKC. Weak pull-up. 0 = outputs driven high, 1 = Active
11	VDDL		3.3V clock voltage supply
13	VSS		Ground
16	NC		No connect

Absolute Maximum Rating

Supply Voltage (VDD, AVDD, VDDL).....-0.5 to +7.0V
 DC Input Voltage.....-0.5V to V_{DD}+0.5
 Storage Temperature (Non-condensing).....-55°C to +125°C
 Junction Temperature -40°C to +125°C

Data Retention @ T_j = 125°C.....> 10 years
 Package Power Dissipation..... 350 mW
 Static Discharge Voltage..... ≥ 2000V
 (per MIL-STD-883, Method 3015)
 (Above which the useful life may be impaired. For user guide-
 lines, not tested.)

Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V _{DD} , AVDD, VDDL	Supply Voltage	3.135	3.30	3.465	V
T _A	Ambient Temperature	0		70	° C
C _{LOAD}	Max. Load Capacitance			15	pF
F _{ref}	Reference Frequency	100		100	MHz

DC Electrical Characteristics

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
I _{OH}	Output High Current	V _{OH} = V _{DD} - 0.5, V _{DD} /V _{DDL} =3.3V	12	24		mA
I _{OL}	Output Low Current	V _{OL} = 0.5, V _{DD} /V _{DDL} = 3.3V	12	24		mA
V _{IH}	Input High Voltage	CMOS levels, 70% of V _{DD}	0.7V _{DD}			V
V _{IL}	Input Low Voltage	CMOS levels, 30% of V _{DD}			0.3V _{DD}	V
C _{IN} ^[1]	Input Capacitance	Input pins excluding XIN			7	pF
R _{UP} ^[1]	Pull-up resistor on input pins	V _{DD} = 3.14 to 3.47V, measured at V _{IN} = 0V		100	150	kΩ
I _{VDD}	Supply Current	AV _{DD} /V _{DD} Current. CLKE = 100 MHz		25	35	mA
I _{VDDL}	Supply Current	V _{DDL} Current, Frequency of CLK(A-D) = 100 MHz		30	40	mA

AC Electrical Characteristics^[1]

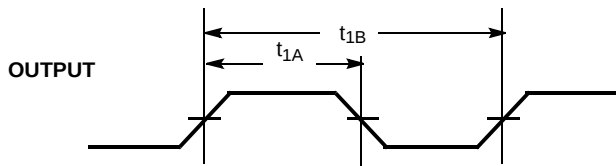
Parameter	Description	Condition	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Measured at V _{DD} /2, t _{1A} /t _{1B}	45	50	55	%
t _r	Rising Edge Slew Rate	20% – 80% of V _{DD} /V _{DDL}	0.8	1.4		V/ns
t _f	Falling Edge Slew Rate	80% – 20% of V _{DD} /V _{DDL}	0.8	1.4		V/ns
t _j	RMS Clock Cycle-to-Cycle Jitter	RMS cycle-to-cycle jitter with Spread on. Measured at VDD/2.		15	40	ps

Note:

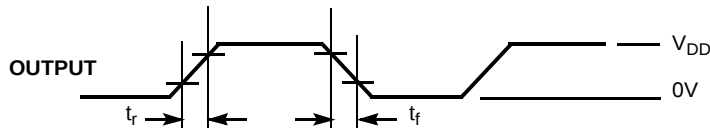
1. Guaranteed by Characterization, not 100% tested.

Switching Waveforms

Duty Cycle Timing ($DC = t_{1A}/t_{1B}$)



Output Rise/Fall Time

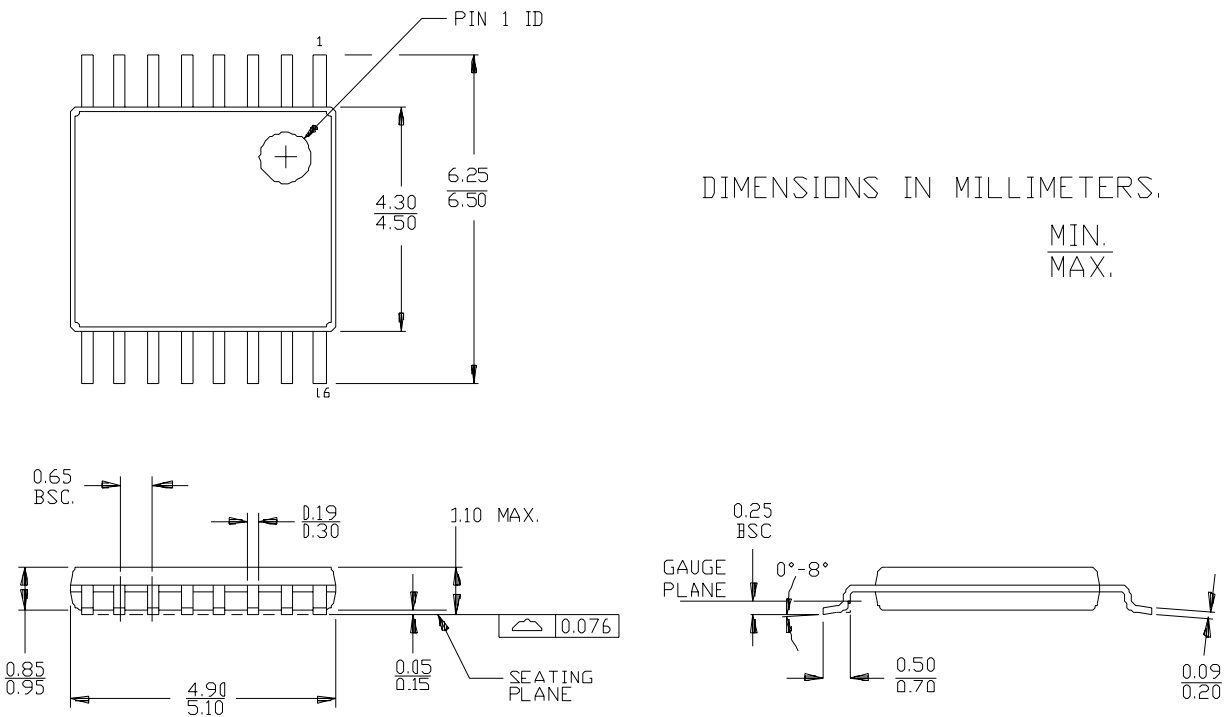


Ordering Information

Ordering Code	Package Type	Operating Range	Spread Profile
CY28507ZC-2	16-pin TSSOP	Commercial, 0°C to 70°C	1% downspread
CY28507ZC-2T	16-pin TSSOP – Tape and Reel	Commercial, 0°C to 70°C	1% downspread
CY28507ZC-3	16-pin TSSOP	Commercial, 0°C to 70°C	1% downspread
CY28507ZC-3T	16-pin TSSOP – Tape and Reel	Commercial, 0°C to 70°C	1% downspread
CY28507ZC-4	16-pin TSSOP	Commercial, 0°C to 70°C	no spread
CY28507ZC-4T	16-pin TSSOP – Tape and Reel	Commercial, 0°C to 70°C	no spread

Package Drawing and Dimensions

16-pin Thin Shrunk Small Outline Package (4.40 MM Body) Z16



51-85091-.**

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**	114667	08/30/02	CKN	New Data Sheet