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# HN27C4096AHG/AHCC Series

262,144-word × 16-bit CMOS UV Erasable and Programmable  
ROM

# HITACHI

ADE-203-247A(Z)

Rev. 1.0

Apr. 4, 1997

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## Description

HN27C4096AHG/AHCC is a 4-Mbit ultraviolet erasable and electrically programmable ROM, featuring high speed access time and programming. Fabricated on advanced fine process and high speed circuitry technique, the HN27C4096AHG/AHCC makes high speed access time possible. Therefore, it is suitable for 16-bit microcomputer systems using high speed microcomputer such as the 80286/68020. The HN27C4096AHG/AHCC offers high speed programming using page programming mode. This device has the package variation of cerdip 40-pin and JLCC 44-pin.

## Features

- High speed
  - Access time: 85 ns (max)
- Low power dissipation
  - Active mode: 35 mW/MHz (typ)
- Fast high reliability page programming and fast high-reliability programming
  - Programming voltage: +12.5 V D.C.
  - Programming time: 3.5 sec. (min) (Theoretical in page programming)
- Inputs and outputs TTL compatible during both read and program modes.
- Pin arrangement: 40-pin JEDEC standard, 44-pin JLCC JEDEC standard
- Device identifier mode: Manufacturer code and device code
- Fully compatible with the HN27C4096HG/HCC Series.

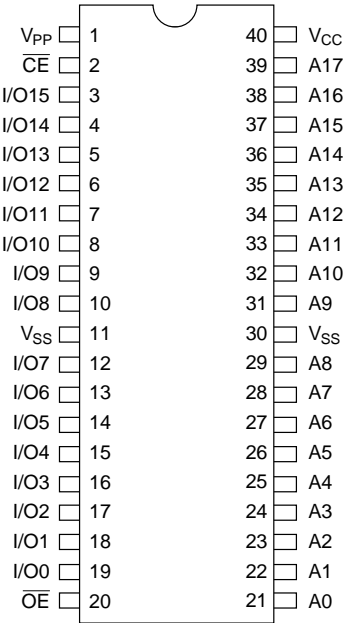
## Ordering Information

Type No.	Access time	Package
HN27C4096AHG-85	85 ns	600-mil 40-pin Cerdip (DG-40A)
HN27C4906AHCC-85	85 ns	44-pin J-bend leaded chip carrier (CC-44)

# HN27C4096AHG/AHCC Series

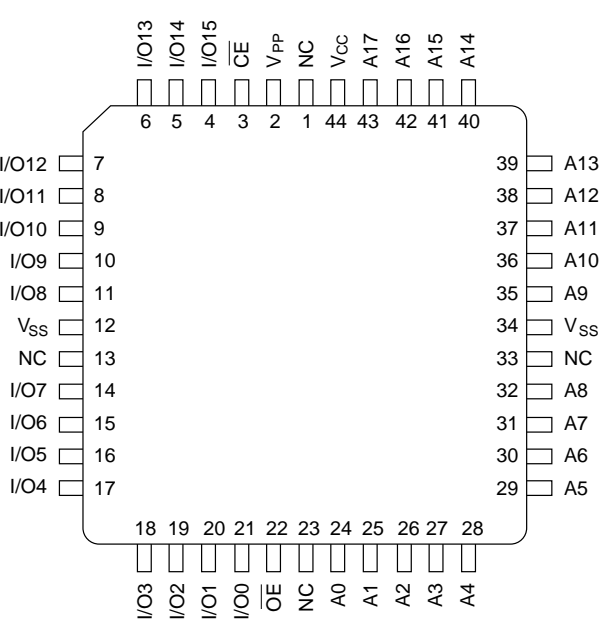
## Pin Arrangement

HN27C4096AHG Series



(Top View)

HN27C4096AHCC Series

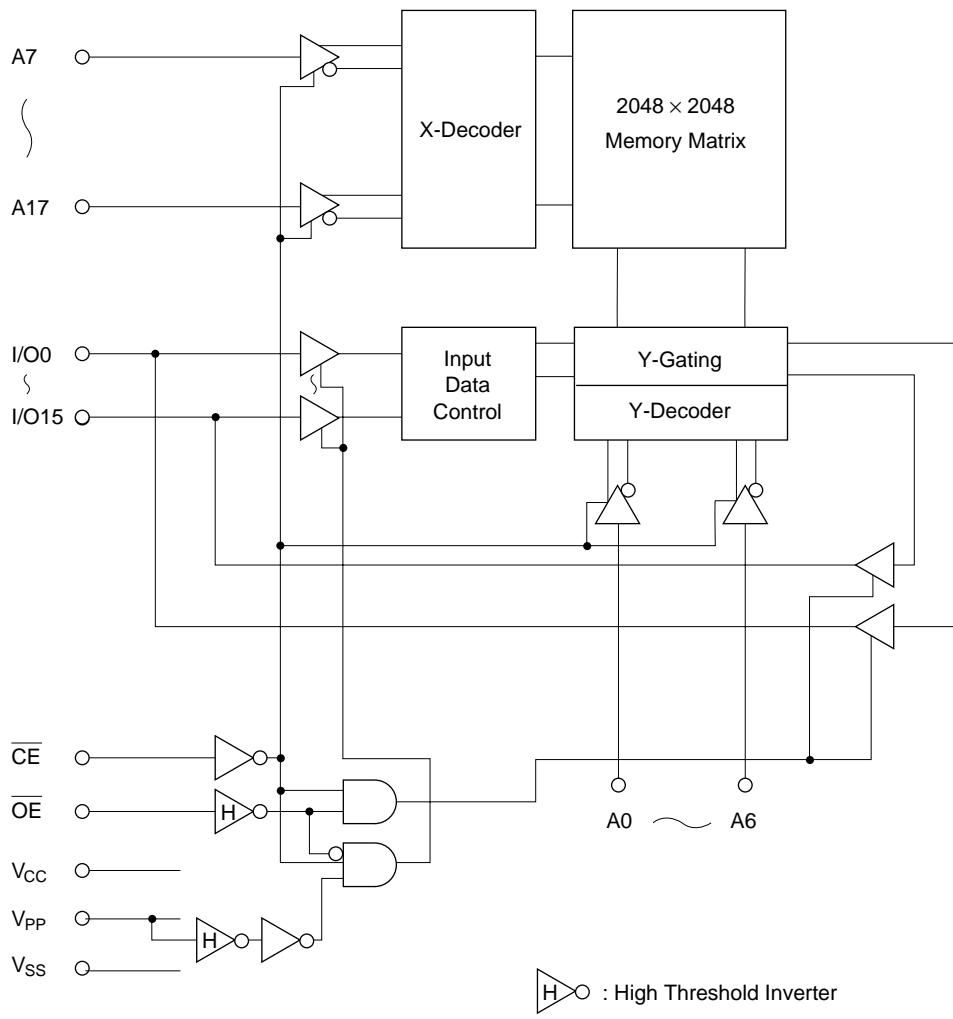


(Top View)

## Pin Description

Pin name	Function
A0 – A17	Address
I/O0 – I/O15	Input/output
CE	Chip enable
OE	Output enable
V <sub>CC</sub>	Power supply
V <sub>PP</sub>	Programming power supply
V <sub>SS</sub>	Ground
NC	No connection

Block Diagram



Mode Selection

		Pin	$\overline{CE}$	$\overline{OE}$	A9	$V_{PP}$	$V_{CC}$	I/O
		CC-44	(3)	(22)	(35)	(2)	(44)	(4 – 11, 14 – 21)
Mode		DG-40A	(2)	(20)	(31)	(1)	(40)	(3 – 10, 12 – 19)
Read			$V_{IL}$	$V_{IL}$	×	$V_{SS} - V_{CC}$	$V_{CC}$	Dout
Output disable			$V_{IL}$	$V_{IH}$	×	$V_{SS} - V_{CC}$	$V_{CC}$	High-Z
Standby			$V_{IH}$	X	×	$V_{SS} - V_{CC}$	$V_{CC}$	High-Z
Page prog.	Page program set		$V_{IH}$	$V_H^{*2}$	×	$V_{PP}$	$V_{CC}$	High-Z
	Page data latch		$V_{IL}$	$V_H^{*2}$	×	$V_{PP}$	$V_{CC}$	Din
	Page program		$V_{IL}$	$V_{IH}$	×	$V_{PP}$	$V_{CC}$	High-Z
	Page program verify		$V_{IH}$	$V_{IL}$	×	$V_{PP}$	$V_{CC}$	Dout
	Page program reset		$V_{IH}$	$V_{IH}$	×	$V_{CC}$	$V_{CC}$	High-Z
Word prog.	Program		$V_{IL}$	$V_{IH}$	×	$V_{PP}$	$V_{CC}$	Din
	Program verify		$V_{IH}$	$V_{IL}$	×	$V_{PP}$	$V_{CC}$	Dout
	Optional verify		$V_{IL}$	$V_{IL}$	×	$V_{PP}$	$V_{CC}$	Dout
	Program inhibit		$V_{IH}$	$V_{IH}$	×	$V_{PP}$	$V_{CC}$	High-Z
Identifier			$V_{IL}$	$V_{IL}$	$V_H^{*2}$	$V_{SS} - V_{CC}$	$V_{CC}$	Code

Notes: 1. ×: Don't care.  
2.  $V_H$ : 12.0 V ± 0.5 V

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
All input and output voltages <sup>*1</sup>	$V_{in}, V_{out}$	−0.6 <sup>*2</sup> to +7.0	V
Voltage on pin A9 and $\overline{OE}$	$V_{ID}$	−0.6 <sup>*2</sup> to +13.0	V
$V_{PP}$ voltage <sup>*1</sup>	$V_{PP}$	−0.6 to +13.5	V
$V_{CC}$ voltage <sup>*1</sup>	$V_{CC}$	−0.6 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range <sup>*3</sup>	Tstg	−65 to +125	°C
Storage temperature under bias	Tbias	−20 to +80	°C

Notes: 1. Relative to  $V_{SS}$ .  
2.  $V_{in}, V_{out}, V_{ID}$  min = −2.0 V for pulse width ≤ 20 ns  
3. Storage temperature range of device before programming.

**Capacitance** ( $T_a = 25^{\circ}\text{C}$ ,  $f = 1\text{ MHz}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	12	pF	Vin = 0 V
Output capacitance	Cout	—	—	20	pF	Vout = 0 V

**Read Operation****DC Characteristics** ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{PP} = V_{SS}$  to  $V_{CC}$ ,  $T_a = 0$  to  $+70^{\circ}\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I <sub>LI</sub>	—	—	2	μA	Vin = 5.5 V
Output leakage current	I <sub>LO</sub>	—	—	2	μA	Vout = 5.5 V/0.45 V
V <sub>PP</sub> current	I <sub>PP1</sub>	—	1	20	μA	V <sub>PP</sub> = 5.5 V
Standby V <sub>CC</sub> current	I <sub>SB</sub>	—	—	30	mA	$\overline{CE} = V_{IH}$
Operating V <sub>CC</sub> current	I <sub>CC1</sub>	—	—	30	mA	Iout = 0 mA, f = 1 MHz
	I <sub>CC2</sub>	—	—	140	mA	Iout = 0 mA, f = 11.8 MHz
Input voltage	V <sub>IL</sub>	-0.3 <sup>*1</sup>	—	0.8	V	
	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> + 1 <sup>*2</sup>	V	
Output voltage	V <sub>OL</sub>	—	—	0.45	V	I <sub>OL</sub> = 2.1 mA
	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> = -400 μA

Notes: 1. V<sub>IL</sub> min = -1.0 V for pulse width ≤ 50 ns  
V<sub>IL</sub> min = -2.0 V for pulse width ≤ 20 ns  
2. V<sub>IH</sub> max = V<sub>CC</sub> + 1.5 V for pulse width ≤ 20 ns  
If V<sub>IH</sub> is over the specified maximum value, read operation cannot be guaranteed.

AC Characteristics ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{PP} = V_{SS}$  to  $V_{CC}$ ,  $T_a = 0$  to  $+70^{\circ}\text{C}$ )

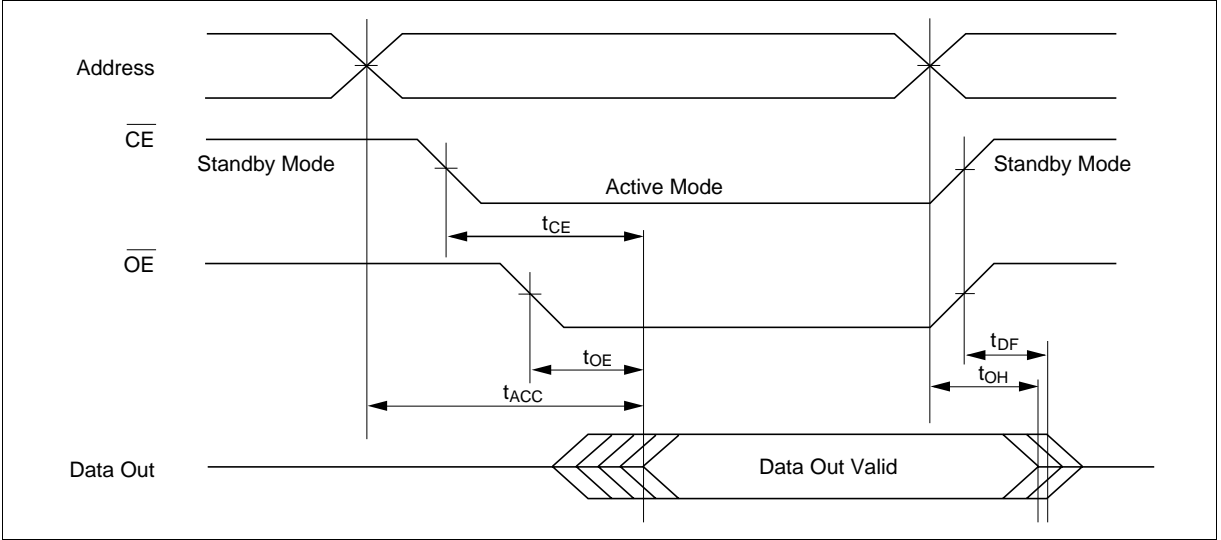
Test Conditions

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall time:  $\leq 10\text{ ns}$
- Output load: 1 TTL gate +100 pF
- Reference levels for measuring timing: 1.5 V

Parameter	Symbol	HN27C4096AHG/AHCC-85		Unit	Test conditions
		Min	Max		
Address to output delay	$t_{ACC}$	—	85	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	$t_{CE}$	—	85	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to output delay	$t_{OE}$	—	45	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ high to output float <sup>*1</sup>	$t_{DF}$	0	30	ns	$\overline{CE} = V_{IL}$
Address to output hold	$t_{OH}$	5	—	ns	$\overline{CE} = \overline{OE} = V_{IL}$

Note: 1.  $t_{DF}$  is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Read Timing Waveform



## **Fast High-Reliability Page Programming**

This device can be applied the high performance page programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.

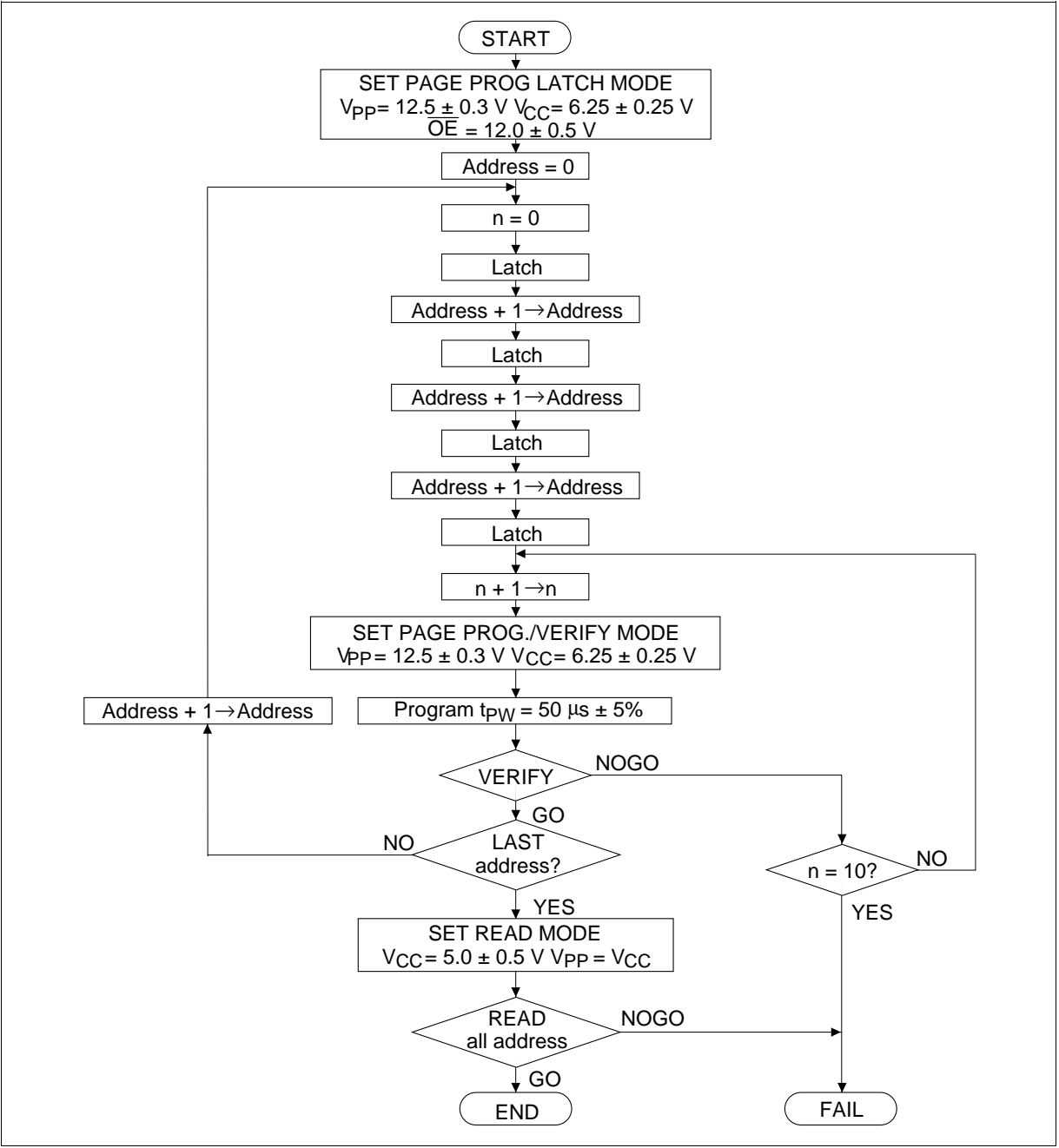
### **Page Program Set**

Apply 12 V to  $\overline{\text{OE}}$  pin after applying 12.5 V to  $V_{\text{PP}}$  to set a page program mode.

The device operates in a page program mode until reset.

### **Page Program Reset**

Set  $V_{\text{PP}}$  to  $V_{\text{CC}}$  level or less to reset a page program mode.





DC Characteristics ( $V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$ ,  $T_a = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	$I_{LI}$	—	—	2	$\mu\text{A}$	$V_{in} = 6.5\text{ V}/0.45\text{ V}$
Output voltage during verify	$V_{OL}$	—	—	0.45	V	$I_{OL} = 2.1\text{ mA}$
	$V_{OH}$	2.4	—	—	V	$I_{OH} = -400\text{ }\mu\text{A}$
Operating $V_{CC}$ current	$I_{CC}$	—	—	50	mA	
Input voltage	$V_{IL}$	$-0.1^{*5}$	—	0.8	V	
	$V_{IH}$	2.2	—	$V_{CC} + 0.5^{*6}$	V	
	$V_H$	11.5	12.0	12.5	V	
$V_{PP}$ supply current	$I_{PP}$	—	—	70	mA	$\overline{CE} = V_{IL}$

- Notes:
- 1.  $V_{CC}$  must be applied before  $V_{PP}$  and removed after  $V_{PP}$ .
  - 2.  $V_{PP}$  must not exceed 13.5 V including overshoot.
  - 3. An influence may be had upon device reliability if the device is installed or removed while  $V_{PP} = 12.5\text{ V}$ .
  - 4. Do not alter  $V_{PP}$  either  $V_{IL}$  to 12.5 V or 12.5 V to  $V_{IL}$  when  $\overline{CE} = \text{low}$ .
  - 5.  $V_{IL}\text{ min} = -0.6\text{ V}$  for pulse width  $\leq 20\text{ ns}$ .
  - 6. If  $V_{IH}$  is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics ( $V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$ ,  $T_a = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ )

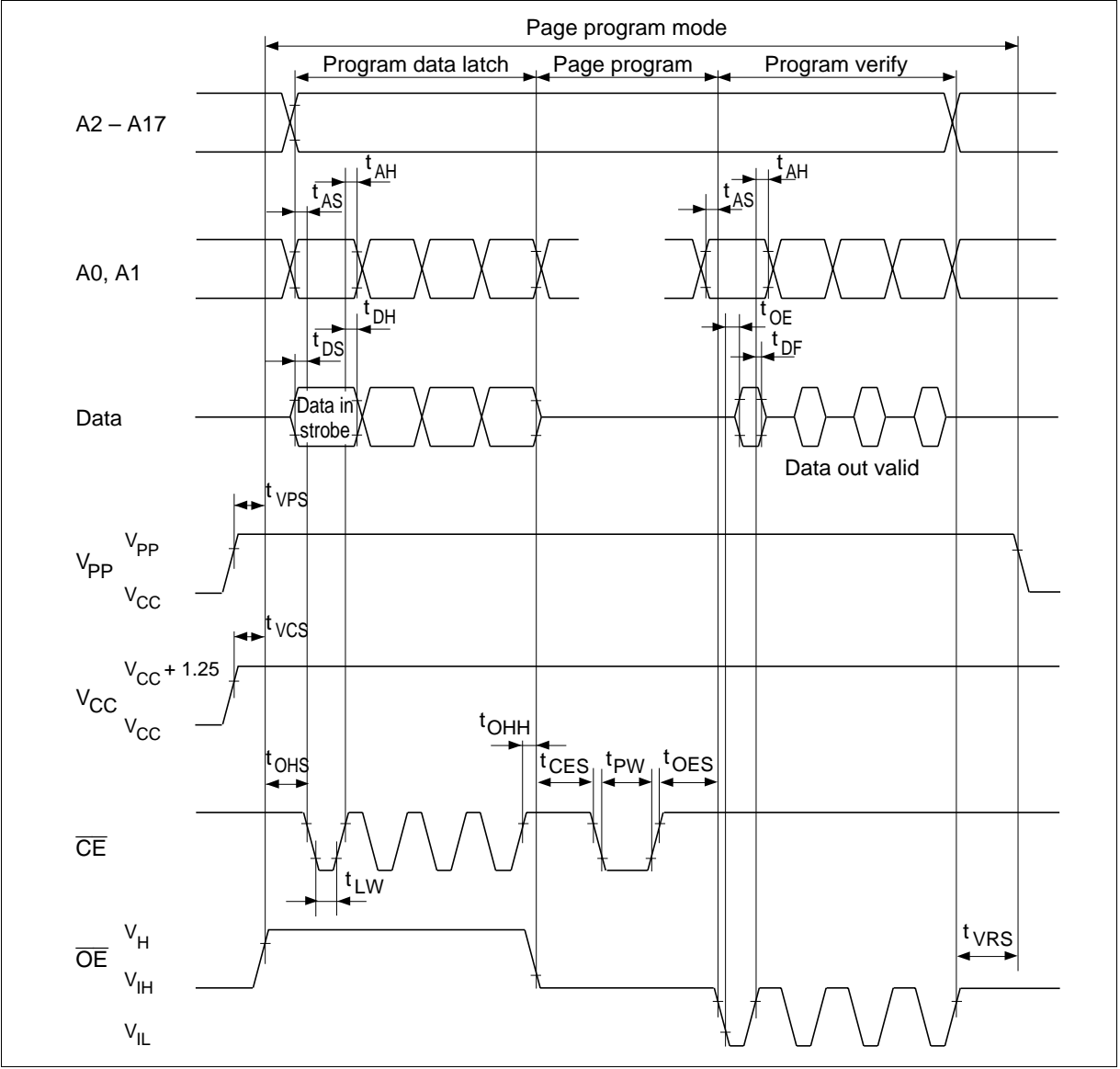
Test Conditions

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall time:  $\leq 20\text{ ns}$
- Reference levels for measuring timings: Inputs; 0.8 V, 2.0 V  
Outputs; 0.8 V, 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	$t_{AS}$	2	—	—	$\mu\text{s}$	
$\overline{OE}$ setup time	$t_{OES}$	2	—	—	$\mu\text{s}$	
Data setup time	$t_{DS}$	2	—	—	$\mu\text{s}$	
Address hold time	$t_{AH}$	0	—	—	$\mu\text{s}$	
Data hold time	$t_{DH}$	2	—	—	$\mu\text{s}$	
$\overline{OE}$ high to output float delay	$t_{DF}^{*1}$	0	—	130	ns	
$V_{PP}$ setup time	$t_{VPS}$	2	—	—	$\mu\text{s}$	
$V_{CC}$ setup time	$t_{VCS}$	2	—	—	$\mu\text{s}$	
$\overline{CE}$ programming pulse width	$t_{PW}$	47.5	50.0	52.5	$\mu\text{s}$	
$\overline{CE}$ setup time	$t_{CES}$	2	—	—	$\mu\text{s}$	
Data valid from $\overline{OE}$	$t_{OE}$	0	—	150	ns	
$\overline{CE}$ pulse width during data latch	$t_{LW}$	1	—	—	$\mu\text{s}$	
$\overline{OE}=V_H$ setup time	$t_{OHS}$	2	—	—	$\mu\text{s}$	
$\overline{OE}=V_H$ hold time	$t_{OHH}$	2	—	—	$\mu\text{s}$	
$V_{PP}$ hold time <sup>*2</sup>	$t_{VRS}$	1	—	—	$\mu\text{s}$	

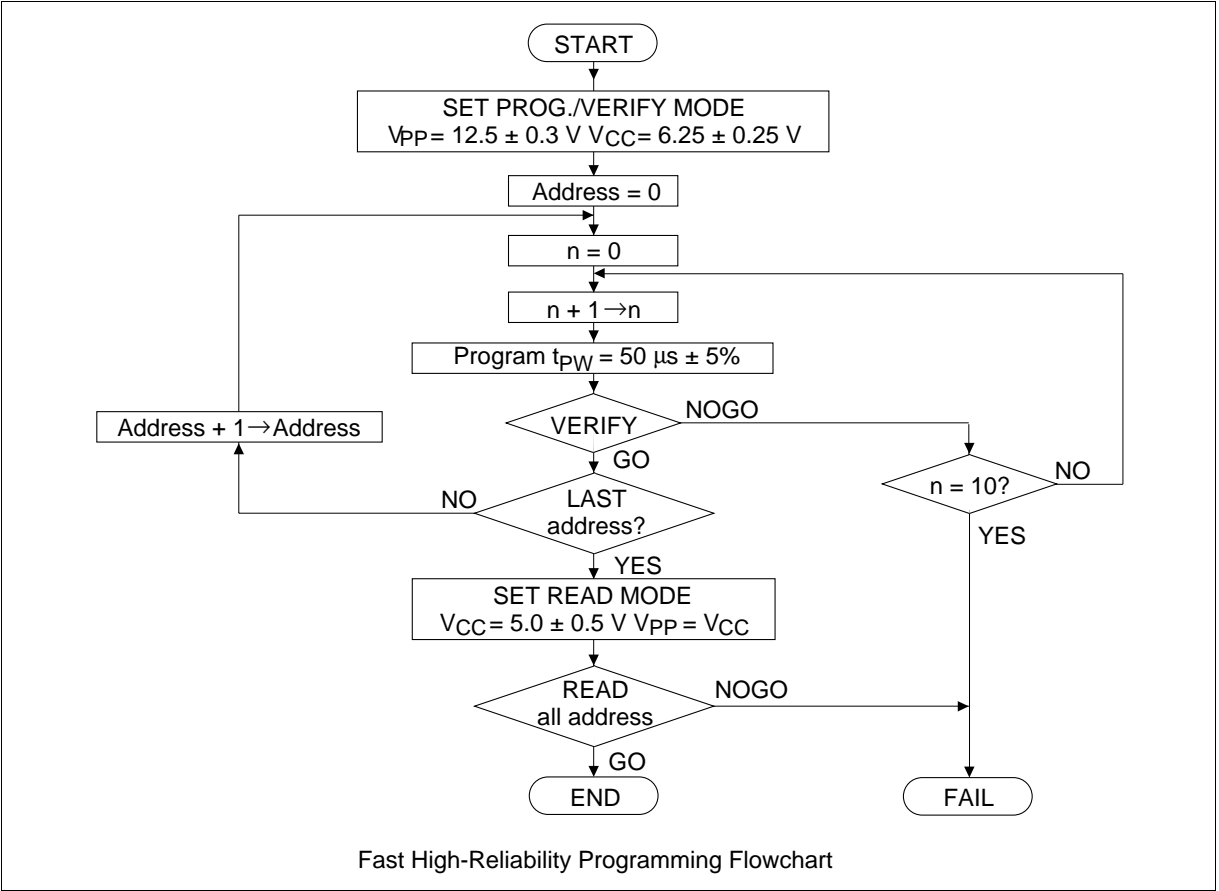
Notes: 1.  $t_{DF}$  is defined as the time at which the output achieves the open circuit condition and data is no longer driven.  
2. Page program mode will be reset when  $V_{PP}$  is set to  $V_{CC}$  or less.

Fast High-Reliability Page Programming Timing Waveform



Fast High-Reliability Programming

This device can be applied the fast high-reliability programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



DC Characteristics ( $V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$ ,  $T_a = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	$I_{LI}$	—	—	2	$\mu\text{A}$	$V_{in} = 6.5\text{ V}/0.45\text{ V}$
$V_{PP}$ supply current	$I_{PP}$	—	—	40	$\text{mA}$	$\overline{CE} = V_{IL}$
Operating $V_{CC}$ current	$I_{CC}$	—	—	50	$\text{mA}$	
Input voltage	$V_{IL}$	$-0.1^{*5}$	—	0.8	$\text{V}$	
	$V_{IH}$	2.2	—	$V_{CC} + 0.5^{*6}$	$\text{V}$	
Output voltage	$V_{OL}$	—	—	0.45	$\text{V}$	$I_{OL} = 2.1\text{ mA}$
	$V_{OH}$	2.4	—	—	$\text{V}$	$I_{OH} = -400\text{ }\mu\text{A}$

- Notes:
- 1.  $V_{CC}$  must be applied before  $V_{PP}$  and removed after  $V_{PP}$ .
  - 2.  $V_{PP}$  must not exceed 13.5 V including overshoot.
  - 3. An influence may be had upon device reliability if the device is installed or removed while  $V_{PP} = 12.5\text{ V}$ .
  - 4. Do not alter  $V_{PP}$  either  $V_{IL}$  to 12.5 V or 12.5 V to  $V_{IL}$  when  $\overline{CE} = \text{low}$ .
  - 5.  $V_{IL}\text{ min} = -0.6\text{ V}$  for pulse width  $\leq 20\text{ ns}$ .
  - 6. If  $V_{IH}$  is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics ( $V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$ ,  $T_a = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ )

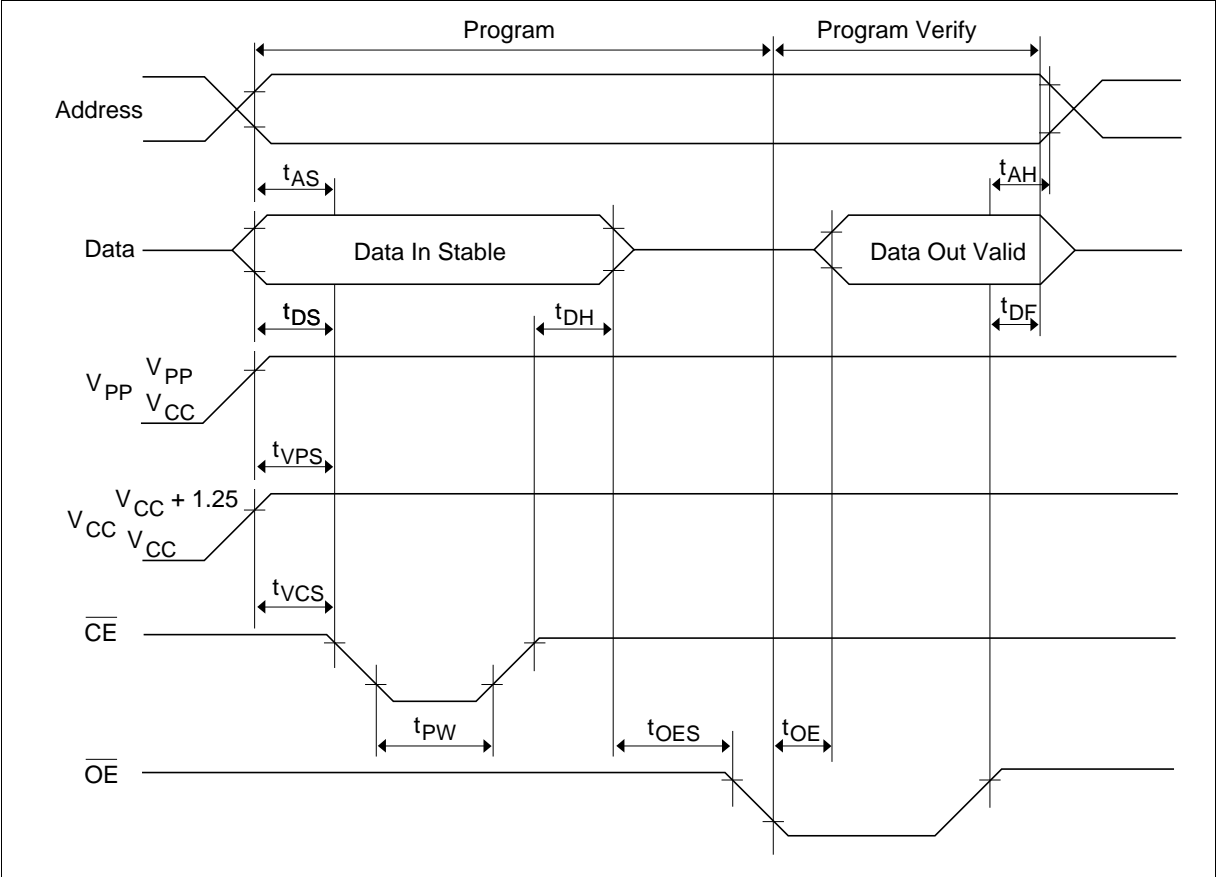
Test Conditions

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall time:  $\leq 20\text{ ns}$
- Reference levels for measuring timings: Inputs: 0.8 V, 2.0 V  
Outputs: 0.8 V, 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	$t_{AS}$	2	—	—	$\mu\text{s}$	
$\overline{OE}$ setup time	$t_{OES}$	2	—	—	$\mu\text{s}$	
Data setup time	$t_{DS}$	2	—	—	$\mu\text{s}$	
Address hold time	$t_{AH}$	0	—	—	$\mu\text{s}$	
Data hold time	$t_{DH}$	2	—	—	$\mu\text{s}$	
$\overline{OE}$ to output float delay	$t_{DF}^{*1}$	0	—	130	ns	
$V_{PP}$ setup time	$t_{VPS}$	2	—	—	$\mu\text{s}$	
$V_{CC}$ setup time	$t_{VCS}$	2	—	—	$\mu\text{s}$	
$\overline{CE}$ programming pulse width	$t_{PW}$	47.5	50.0	52.5	$\mu\text{s}$	
Data valid from $\overline{OE}$	$t_{OE}$	0	—	150	ns	

Note: 1.  $t_{DF}$  is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

# Fast High-Reliability Programming Timing Waveform

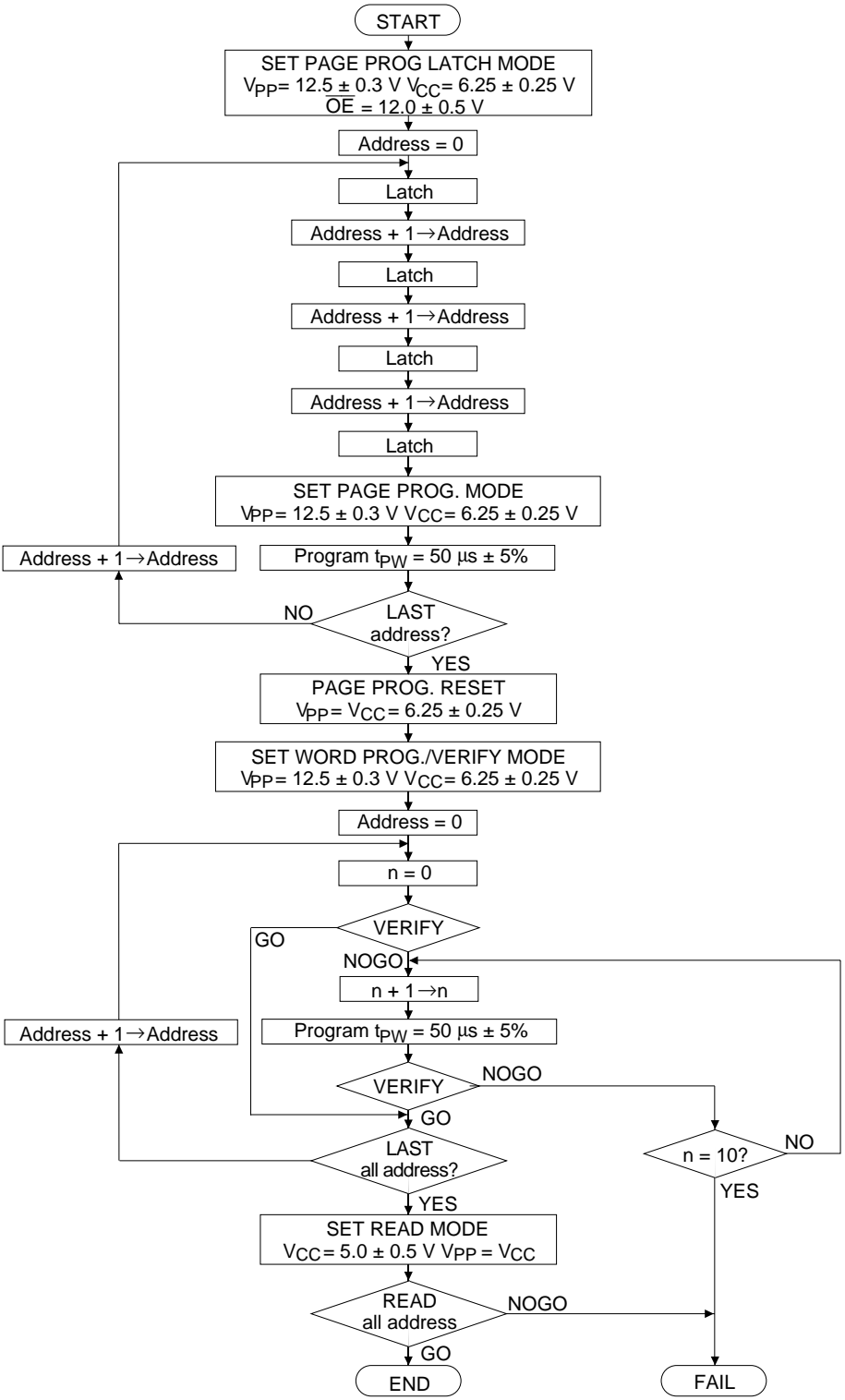


## Optional Page Programming

This device can be applied the optional page programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.

This programming algorithm is the combination of page programming and word verify. It can avoid the increase of programming verify time when a programmer with slow machine cycle is used, and shorten the total programming time.

Regarding the timing specifications for page programming and word verify, please refer to the specifications for fast high-reliability page programming and fast high-reliability programming.



Optional Page Programming Flowchart



**DC Characteristics** ( $V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$ ,  $T_a = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	$I_{LI}$	—	—	2	$\mu\text{A}$	$V_{in} = 6.5\text{ V}/0.45\text{ V}$
Output voltage during verify	$V_{OL}$	—	—	0.45	V	$I_{OL} = 2.1\text{ mA}$
	$V_{OH}$	2.4	—	—	V	$I_{OH} = -400\text{ }\mu\text{A}$
Operating $V_{CC}$ current	$I_{CC}$	—	—	50	mA	
Input voltage	$V_{IL}$	$-0.1^{*5}$	—	0.8	V	
	$V_{IH}$	2.2	—	$V_{CC} + 0.5^{*6}$	V	
	$V_H$	11.5	12.0	12.5	V	
$V_{PP}$ supply current	$I_{PP}$	—	—	70	mA	$\overline{CE} = V_{IL}$

- Notes:
- $V_{CC}$  must be applied before  $V_{PP}$  and removed after  $V_{PP}$ .
  - $V_{PP}$  must not exceed 13.5 V including overshoot.
  - An influence may be had upon device reliability if the device is installed or removed while  $V_{PP} = 12.5\text{ V}$ .
  - Do not alter  $V_{PP}$  either  $V_{IL}$  to 12.5 V or 12.5 V to  $V_{IL}$  when  $\overline{CE} = \text{low}$ .
  - $V_{IL}$  min =  $-0.6\text{ V}$  for pulse width  $\leq 20\text{ ns}$ .
  - If  $V_{IH}$  is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics ( $V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$ ,  $T_a = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ )

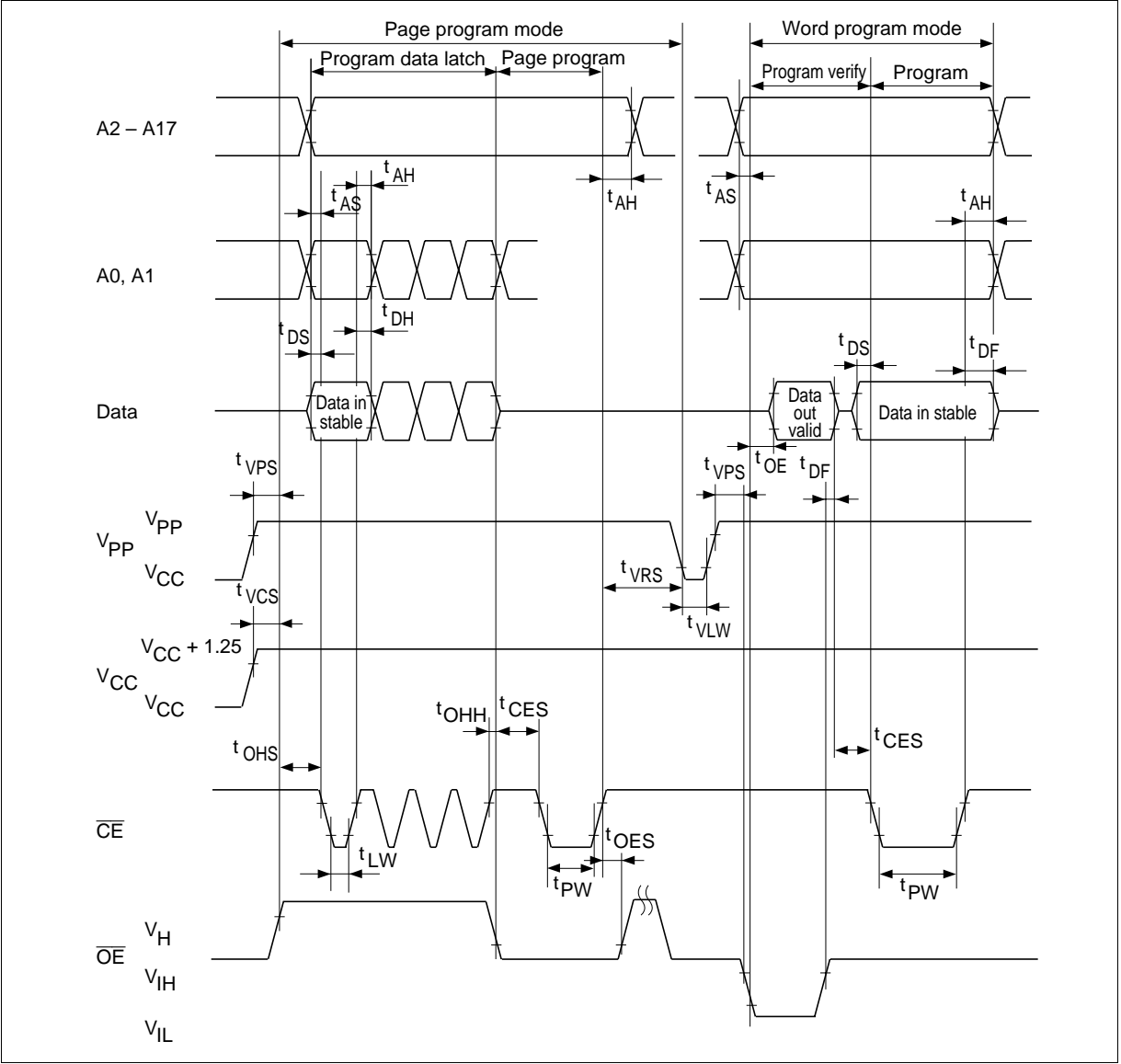
Test Conditions

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall time:  $\leq 20\text{ ns}$
- Reference levels for measuring timing: Inputs: 0.8 V, 2.0 V,  
Outputs: 0.8 V, 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	$t_{AS}$	2	—	—	$\mu\text{s}$	
$\overline{OE}$ setup time	$t_{OES}$	2	—	—	$\mu\text{s}$	
Data setup time	$t_{DS}$	2	—	—	$\mu\text{s}$	
Address hold time	$t_{AH}$	0	—	—	$\mu\text{s}$	
Data hold time	$t_{DH}$	2	—	—	$\mu\text{s}$	
$\overline{OE}$ high to output float delay	$t_{DF}^{*1}$	0	—	130	ns	
$V_{PP}$ setup time	$t_{VPS}$	2	—	—	$\mu\text{s}$	
$V_{CC}$ setup time	$t_{VCS}$	2	—	—	$\mu\text{s}$	
$\overline{CE}$ initial programming pulse width	$t_{PW}$	47.5	50.0	52.5	$\mu\text{s}$	
$\overline{CE}$ setup time	$t_{CES}$	2	—	—	$\mu\text{s}$	
Data valid from $\overline{OE}$	$t_{OE}$	0	—	150	ns	
$\overline{CE}$ pulse width during data latch	$t_{LW}$	1	—	—	$\mu\text{s}$	
$\overline{OE} = V_H$ setup time	$t_{OHS}$	2	—	—	$\mu\text{s}$	
$\overline{OE} = V_H$ hold time	$t_{OHH}$	2	—	—	$\mu\text{s}$	
Page programming reset time <sup>*2</sup>	$t_{VLW}$	1	—	—	$\mu\text{s}$	
$V_{PP}$ hold time <sup>*2</sup>	$t_{VRS}$	1	—	—	$\mu\text{s}$	

Notes: 1.  $t_{DF}$  is defined as the time at which the output achieves the open circuit condition and data is no longer driven.  
2. Page program mode will be reset when  $V_{PP}$  is set to  $V_{CC}$  or less.

Option Page Programming Timing Waveform



Erase

Erasure of HN27C4096AHG/AHCC is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to “1” after this erasure procedure. The minimum integrated dose (i.e. UV intensity × exposure time) for erasure is 15 W · sec/cm<sup>2</sup>.

Mode Description

Device Identifier Mode

The device identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

HN27C4096AH Identifier Code

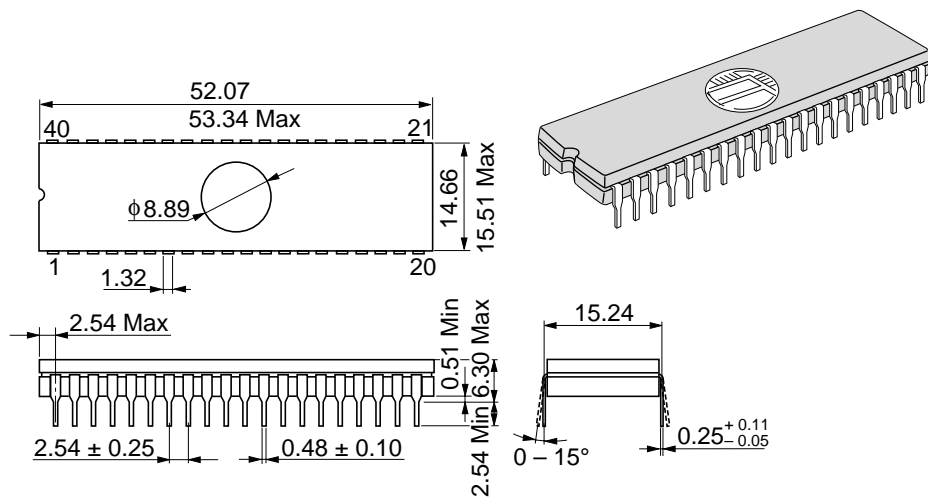
Identifier												Hex data
	A0	I/O8 – I/O15		I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	
	CC-44	(24)	(11) – (4)	(14)	(15)	(16)	(17)	(18)	(19)	(20)	(21)	
	DG-40A	(21)	(10) – (3)	(12)	(13)	(14)	(15)	(16)	(17)	(18)	(19)	
Manufacturer code	$V_{IL}$	×		0	0	0	0	0	1	1	1	07
Device code	$V_{IH}$	×		1	0	1	0	0	0	1	0	A2

- Notes: 1.  $V_{CC} = 5.0\text{ V} \pm 10\%$   
2.  $A9 = 12.0\text{ V} \pm 0.5\text{ V}$   
3.  $A1 - A8, A10 - A17, \overline{CE}, \overline{OE} = V_{IL}$   
4. ×: Don't care.

Package Dimensions

HN27C4096AHG Series (DG-40A)

Unit: mm



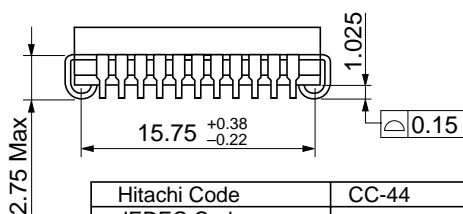
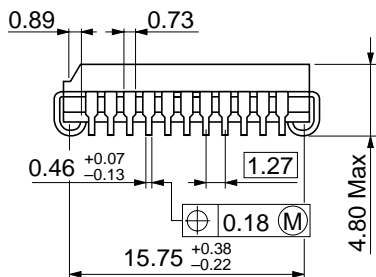
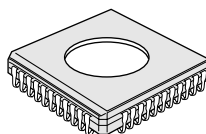
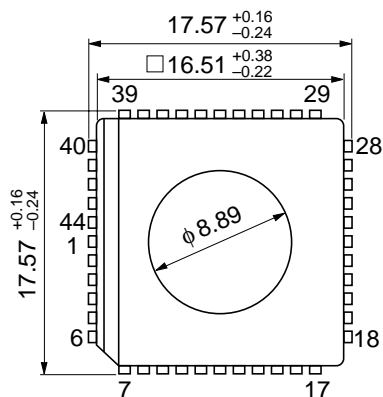
Hitachi Code	DG-40A
JEDEC Code	—
EIAJ Code	SC-615 Mod.
Weight	12.57 g

## HN27C4096AHG/AHCC Series

## Package Dimensions(cont)

## HN27C4096AHCC Series (CC-44)

Unit: mm



Hitachi Code	CC-44
JEDEC Code	—
EIAJ Code	—
Weight	2.62 g

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# HITACHI

## **Hitachi, Ltd.**

Semiconductor & IC Div.  
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan  
Tel: Tokyo (03) 3270-2111  
Fax: (03) 3270-5109

### **For further information write to:**

Hitachi America, Ltd.  
Semiconductor & IC Div.  
2000 Sierra Point Parkway  
Brisbane, CA. 94005-1835  
U S A  
Tel: 415-589-8300  
Fax: 415-583-4207

Hitachi Europe GmbH  
Electronic Components Group  
Continental Europe  
Domacher Straße 3  
D-85622 Feldkirchen  
München  
Tel: 089-9 91 80-0  
Fax: 089-9 29 30 00

Hitachi Europe Ltd.  
Electronic Components Div.  
Northern Europe Headquarters  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA  
United Kingdom  
Tel: 0628-585000  
Fax: 0628-778322

Hitachi Asia Pte. Ltd.  
16 Collyer Quay #20-00  
Hitachi Tower  
Singapore 0104  
Tel: 535-2100  
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.  
Unit 706, North Tower,  
World Finance Centre,  
Harbour City, Canton Road  
Tsim Sha Tsui, Kowloon  
Hong Kong  
Tel: 27359218  
Fax: 27306071

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	May. 6, 1994	Initial issue	A. Nara	T. Muto
1.0	Apr. 4, 1997	Change of format DC Characteristics ( $V_{CC} = 5\text{ V} \pm 10\%$ , $V_{PP} = V_{SS}$ to $V_{CC}$ , $T_a = 0$ to $+70^{\circ}\text{C}$ ) $I_{CC1}$ max 35 mA to 30 mA AC Characteristics Deletion of $t_{BAC}$ Change of Read timing waveform Deletion of Read timing waveform (Burst access mode) DC Characteristics ( $V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$ , $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$ , $T_a = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ ) Change of note2		