

SANYO**LC79430D****Dot Matrix LCD Driver**

Overview

The LC79430D is a large-scale dot matrix LCD common driver LSI. The LC79430D contains an 80-bit bidirectional shift register and is equipped with a 4-level LCD driver. The input/output pins for cascade connection can be used to further increase the IC number of bits. The LC79430D can be used in conjunction with segment driver LC79400D, LC79401D (QFP100D) to drive a wide-screen LCD panel.

Functions and Features

On-chip LCD drive circuit (80 bits)

Display duty selection ranging from 1/64 to 1/256

On-chip input/output pins support further increases in bit number

Supports externally supplied bias voltage

On-chip 80-bit bidirectional shift register (supports 40-bit \times 2 division)

Supports single mode (80-bit shift register) and dual mode (40-bit \times 2 shift register) applications

(1) O1 \rightarrow O80 } Single mode
(2) O80 \rightarrow O1 }

(3) O1 \rightarrow O40 and O41 \rightarrow O80 } Single mode
(4) O80 \rightarrow O41 and O40 \rightarrow O1 }

All four of the shift direction selection listed above all supported.

Operating power supply voltage/operating temperature include

V_{DD} (logic section) : 5 V -10% / 20 to +75 °C

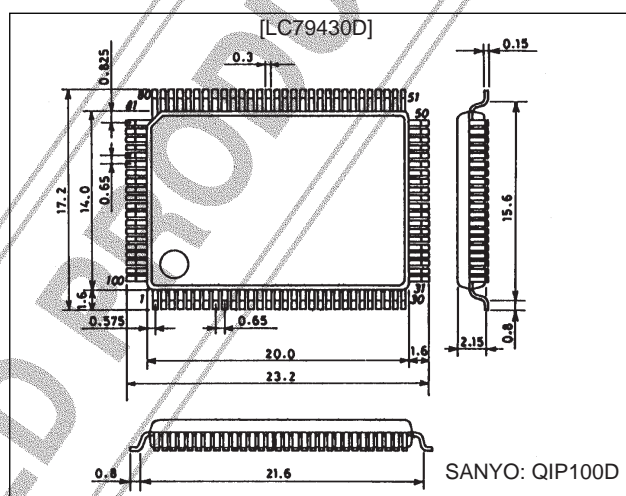
V_{DD} V_{EE} (LCD section) : 12 V to 32 V / 20 to +75 °C

CMOS process

Package Dimensions

unit: mm

3180-QFP100D



Specifications

Absolute Maximum Ratings at $T_a = 25\text{ °C}$ to -2 °C , $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage (LOGIC)	V_{DD} max		-0.3 to +7.0	V
Maximum supply voltage (LCD)	$V_{DD}-V_{EE}$ max *1		0 to 35	V
Maximum input voltage	V_{IN} max		-0.3 to $V_{DD}+0.3$	V
Storage temperature range	T_{stg}		-40 to +125	°C

Note : *1 The following relations between elements should be maintained: $V_{DD} \geq V_1 > V_2 > V_5 > V_{EE}$, $V_{DD} - V_2 \leq 7\text{ V}$, $V_5 - V_{EE} \leq 7\text{ V}$.

SANYO Electric Co.,Ltd. Semiconductor Business Headquarters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

D309THA (OT) /21593JN A8-9626 No. 4348-1/6

LC79430D

Allowable Operating Ranges at $T_a = 20$ to $+75$ °C, $V_{SS} = 0$ V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage (LOGIC)	V_{DD}		4.5		5.5	V
Supply voltage (LCD)	$V_{DD}-V_{EE}$	*2, *3	12		32	V
Input high level voltage	V_{IH}	DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, DISP OFF	$0.8 V_{DD}$			V
Input low level voltage	V_{IL}	DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, DISP OFF			$0.2 V_{DD}$	V
CP (Shift clock)	f_{CP}	CP			1	MHz
CP (Pulse width)	t_{WC}	CP	63			ns
Setup time	t_{SETUP}	DIO1 → CP, DIO80 → CP, DMIN → CP	100			ns
Hold time	t_{HOLD}	DIO1 → CP, DIO80 → CP, DMIN → CP	100			ns
CP rise fall time	t_R	CP			50	ns
	t_F	CP			50	ns

Note: *2 The following relations between elements should be maintained: $V_{DD} \geq V_1 > V_2 > V_5 > V_{EE}$. $V_{DD} - V_2 \leq 7$ V, $V_5 - V_{EE} \leq 7$ V.

*3 When the power supply is turned on, power to the LCD drive is turned on after or simultaneously with the turning on of the logic section's power supply. When the power supply is turned off, the logic power supply is turned off after or at the same time the LCD driver power supply is turned off.

Electrical Characteristics at $T_a = 25-2$ °C, $V_{SS} = 0$ V, $V_{DD} = 5$ V -10%

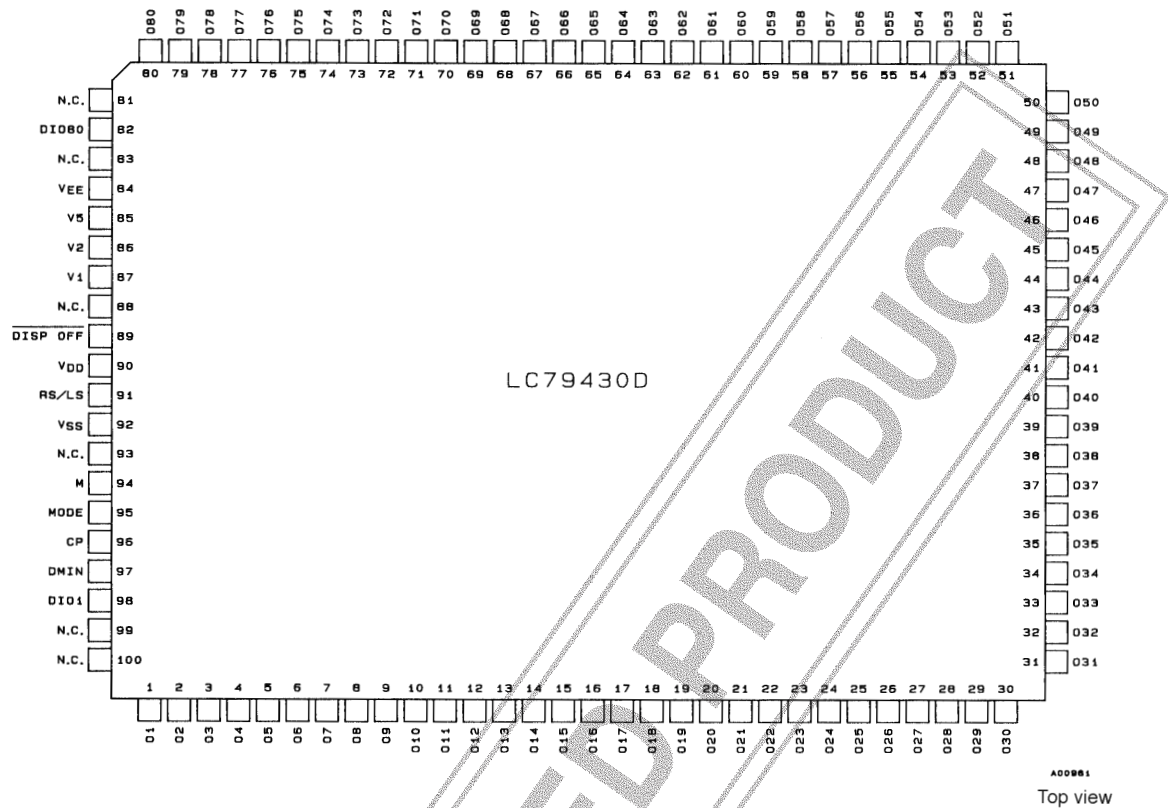
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high level current	I_{IH}	$V_{IN} = V_{DD}$, $V_{DD} = 5.5$ V; DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, DISP OFF			1	μ A
Input low level current	I_{IL}	$V_{IN} = V_{SS}$, $V_{DD} = 5.5$ V; DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, DISP OFF	-1			μ A
Output high level voltage	V_{OH}	$I_{OH} = -0.4$ mA, $V_{DD} = 4.5$ V; DIO1, DIO80	$V_{DD}-0.4$			V
Output low level voltage	V_{OL}	$I_{OL} = 0.4$ mA, $V_{DD} = 4.5$ V; DIO1, DIO80			0.4	V
Driver on register	$R_{ON(1)}$	$V_{DD}-V_{EE} = 30$ V, $ V_{DE} - V_O = 0.5$ V, $V_{DD} = 4.5$ V *4; O1 TO O80			1.0	K Ω
	$R_{ON(2)}$	$V_{DD}-V_{EE} = 20$ V, $ V_{DE} - V_O = 0.5$ V, $V_{DD} = 4.5$ V *4; O1 TO O80			1.0	K Ω
Consumable current (1)	I_{SS}	$V_{DD}-V_{EE} = 30$ V, CP = 14 kHz, no-load, $V_{DD} = 5.5$ V; V_{SS}			100	μ A
Consumable current (2)	I_{EE}	$V_{DD}-V_{EE} = 30$ V, CP = 14 kHz, no-load, $V_{DD} = 5.5$ V; V_{EE}			100	μ A
Input capacity	C_{IN}	$f = 1$ MHz; CP		5		pF

Note: *4 $V_{DE} = V_1$ or V_2 or V_5 or V_{EE} , $V_1 = V_{DD}$, $V_2 = 16/17 (V_{DD}-V_{EE})$, $V_5 = 1/17 (V_{DD}-V_{EE})$

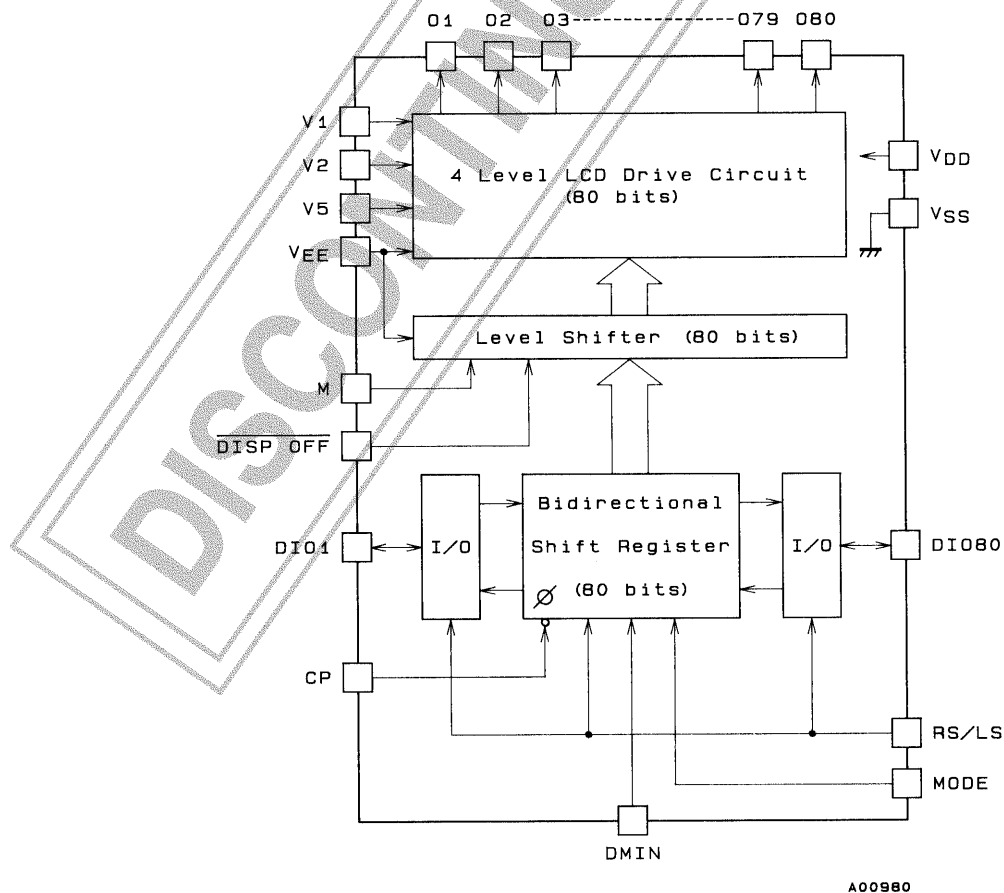
Switching Characteristics at $T_a = 25-2$ °C, $V_{SS} = 0$ V, $V_{DD} = 5$ V -10%

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output delay time	t_{PLH}	$C_L = 15$ pF; CP → DIO1, CP → DIO80			250	ns
	t_{PHL}	$C_L = 15$ pF; CP → DIO1, CP → DIO80			250	ns

Pin Assignment



Equivalent Circuit Block Diagram



Pin Descriptions

Pin No.	Pin name	Input/Output	Functions																												
90	V _{DD}	Power supply	V _{DD} and V _{SS} : Power supply for logic section																												
92	V _{SS}																														
84	V _{EE}		V _{DD} and V _{EE} : Power supply for LCD drive circuit																												
87	V1	Power supply	Power supply for LCD drive level																												
86	V2		V1 and V _{EE} : Select level																												
85	V5		V2 and V5 : Non-select level																												
96	CP	Input	Bidirectional shift register shift clock (triggering on the trailing edge)																												
98	DIO1	Input/Output	<table><tr><th>Mode</th><th>RS/LS</th><th>Data Transfer Direction</th><th>DIO1</th><th>DIO8</th><th>DMIN</th></tr><tr><td rowspan="2">L (Single)</td><td>L (Shift right)</td><td>O1 → O80</td><td>IN</td><td>OUT</td><td>*</td></tr><tr><td>H (Shift left)</td><td>O80 → O1</td><td>OUT</td><td>IN</td><td>*</td></tr><tr><td rowspan="2">H (Dual)</td><td>L (Shift right)</td><td>O1 → O40 O41 → O80</td><td>IN</td><td>OUT</td><td>IN</td></tr><tr><td>H (Shift left)</td><td>O80 → O41 O40 → O1</td><td>OUT</td><td>IN</td><td>IN</td></tr></table> <p>* Don't care (May be set to either "H" or "L")</p>	Mode	RS/LS	Data Transfer Direction	DIO1	DIO8	DMIN	L (Single)	L (Shift right)	O1 → O80	IN	OUT	*	H (Shift left)	O80 → O1	OUT	IN	*	H (Dual)	L (Shift right)	O1 → O40 O41 → O80	IN	OUT	IN	H (Shift left)	O80 → O41 O40 → O1	OUT	IN	IN
Mode	RS/LS	Data Transfer Direction		DIO1	DIO8	DMIN																									
L (Single)	L (Shift right)	O1 → O80		IN	OUT	*																									
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H (Dual)	L (Shift right)	O1 → O40 O41 → O80		IN	OUT	IN																									
	H (Shift left)	O80 → O41 O40 → O1		OUT	IN	IN																									
82	DIO80	Input/Output																													
91	RS/LS	Input																													
95	MODE	Input																													
97	DMIN	Input																													
94	M	Input	LCD drive output alternating signal																												
89	DISP OFF	Input	O1 to O80 output controlling input pins																												
1	O1	Output	LCD drive output																												
80	O80		As shown in the following table, output levels switch in response to the particular combination of scan data, M and DISP OFF signals.																												
			<table><tr><th>M</th><th>Data</th><th>DISP OFF</th><th>Output</th></tr><tr><td>L</td><td>L</td><td>H</td><td>V2</td></tr><tr><td>L</td><td>H</td><td>H</td><td>V_{EE}</td></tr><tr><td>H</td><td>L</td><td>H</td><td>V5</td></tr><tr><td>H</td><td>H</td><td>H</td><td>V1</td></tr><tr><td>*</td><td>*</td><td>L</td><td>V1</td></tr></table>	M	Data	DISP OFF	Output	L	L	H	V2	L	H	H	V _{EE}	H	L	H	V5	H	H	H	V1	*	*	L	V1				
M	Data		DISP OFF	Output																											
L	L		H	V2																											
L	H		H	V _{EE}																											
H	L		H	V5																											
H	H		H	V1																											
*	*		L	V1																											
			* Don't care (May be set to either "H" or "L")																												

Common Driver Multi-Unit Connection Circuits.

* Using single mode DMIN input pins are fixed to either \bar{H} or \bar{L}

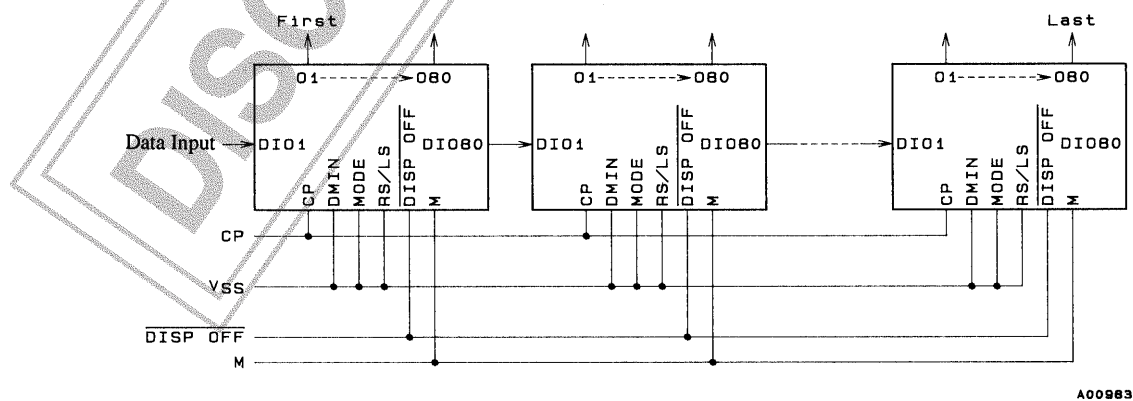


Figure 1 Single Mode (Right Directional Shift)

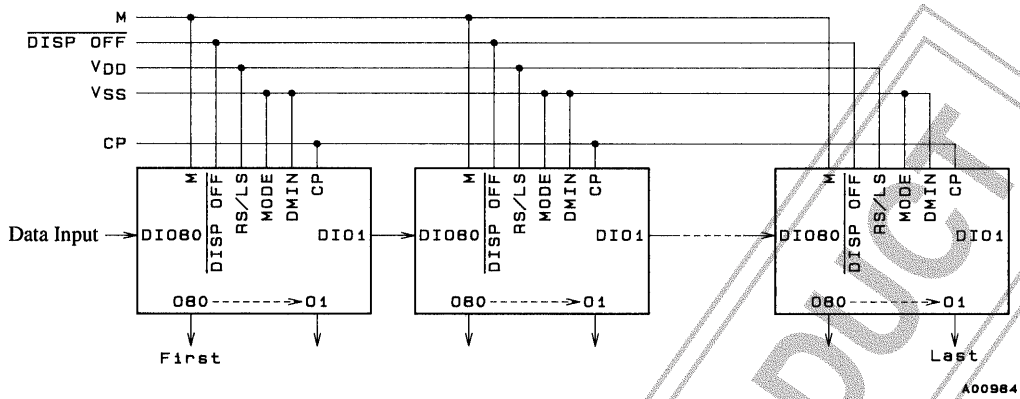


Figure 2 Single Mode (Left Directional Shift)

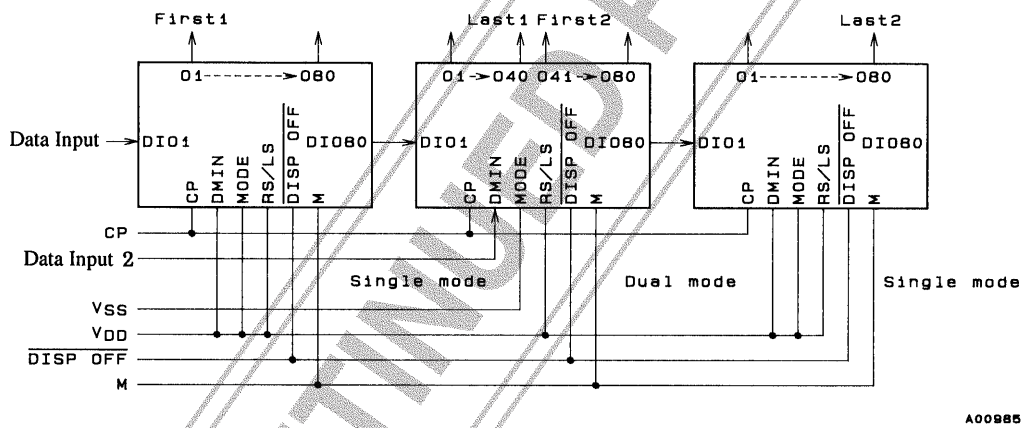


Figure 3 Dual Mode (Right Directional Shift)

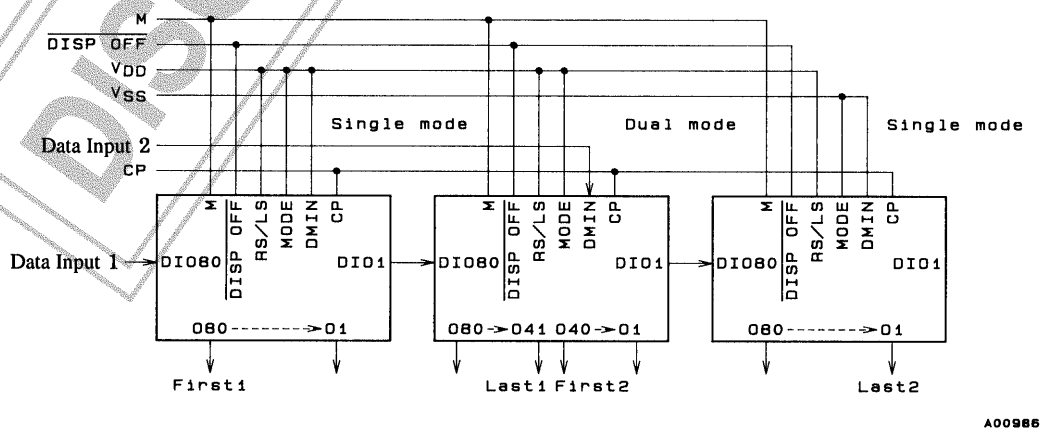
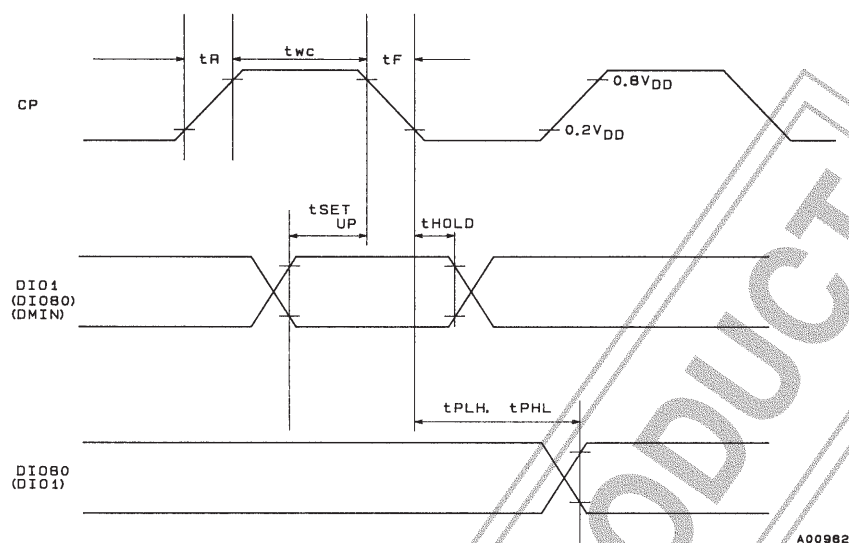


Figure 4 Dual Mode (Left Directional Shift)

Switching Characteristics



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