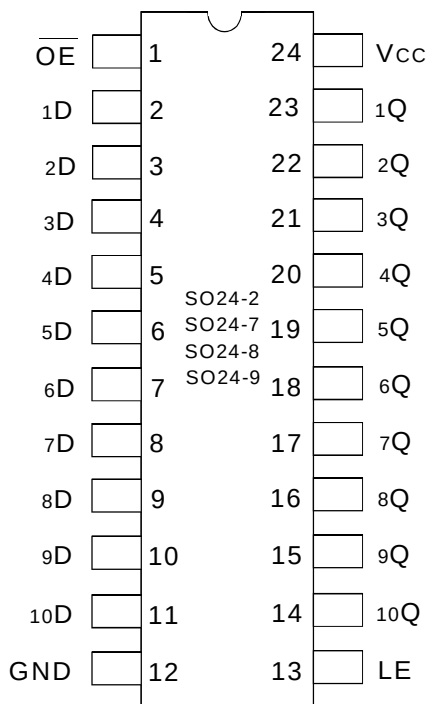


PIN CONFIGURATION



SOIC/ SSOP/ QSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
T _{STG}	Storage Temperature	– 65 to +150	°C
I _{OUT}	DC Output Current	– 50 to +50	mA
I _{IK} I _{OK}	Continuous Clamp Current, V _I < 0 or V _O < 0	– 50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

8LVC

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

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NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
OE	Output-enable Control (Active LOW)
LE	Latch-enable Input
x _D	Latch Data Inputs
x _Q	3-State Latch Data Outputs

FUNCTION TABLE ⁽¹⁾

Inputs			Outputs
OE	LE	x _D	x _Q
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
Q₀ = Level of Q before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ To $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to 5.5V	—	—	± 5	μA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = 0$ to 5.5V	—	—	± 10	μA
I_{OFF}	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}$, V_{IN} or $V_O \leq 5.5\text{V}$		—	—	± 50	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$	$V_{IN} = \text{GND}$ or V_{CC}	—	—	10	μA
			$3.6 \leq V_{IN} \leq 5.5\text{V}^{(2)}$	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$, other inputs at V_{CC} or GND		—	—	500	μA

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NOTES:

- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.
- This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = 2.3\text{V}$ to 3.6V	$I_{OH} = -0.1\text{mA}$	$V_{CC} - 0.2$	—	V
		$V_{CC} = 2.3\text{V}$	$I_{OH} = -6\text{mA}$	2	—	
		$V_{CC} = 2.3\text{V}$	$I_{OH} = -12\text{mA}$	1.7	—	
		$V_{CC} = 2.7\text{V}$		2.2	—	
		$V_{CC} = 3.0\text{V}$		2.4	—	
		$V_{CC} = 3.0\text{V}$	$I_{OH} = -24\text{mA}$	2.2	—	
V_{OL}	Output LOW Voltage	$V_{CC} = 2.3\text{V}$ to 3.6V	$I_{OL} = 0.1\text{mA}$	—	0.2	V
		$V_{CC} = 2.3\text{V}$	$I_{OL} = 6\text{mA}$	—	0.4	
			$I_{OL} = 12\text{mA}$	—	0.7	
		$V_{CC} = 2.7\text{V}$	$I_{OL} = 12\text{mA}$	—	0.4	
		$V_{CC} = 3.0\text{V}$	$I_{OL} = 24\text{mA}$	—	0.55	

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NOTE:

- V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	Vcc = 2.5V±0.2V	Vcc = 3.3V±0.3V	Unit
			Typical	Typical	
CPD	Power dissipation capacitance per latch outputs enabled	CL = 0pF, f = 10Mhz	—	25	pF
CPD	Power dissipation capacitance per latch outputs disabled		—	6	pF

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	Vcc = 2.5V±0.2V		Vcc = 2.7V		Vcc = 3.3V±0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tPLH	Propagation Delay xD to xQ	—	—	—	7.5	2.4	6.7	ns
tPLH tPHL	Propagation Delay LE to xQ	—	—	—	8.6	2.7	7.6	ns
tPZH tPZL	Output Enable Time OE to xQ	—	—	—	8.5	1.3	7.2	ns
tPHZ tPLZ	Output Disable Time OE to xQ	—	—	—	6.6	1.9	5.9	ns
tw	Pulse Duration	—	—	3.3	—	3.3	—	ns
tsu	Setup Time, data before LE↓	—	—	2.1	—	2.1	—	ns
th	Hold Time, data after LE↓	—	—	1	—	1	—	ns
tsk(0)	Output Skew ⁽²⁾	—	—	—	—	—	1	ns

NOTES:

- See test circuits and waveforms. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.
- Skew between any two outputs of the same package and switching in the same direction.

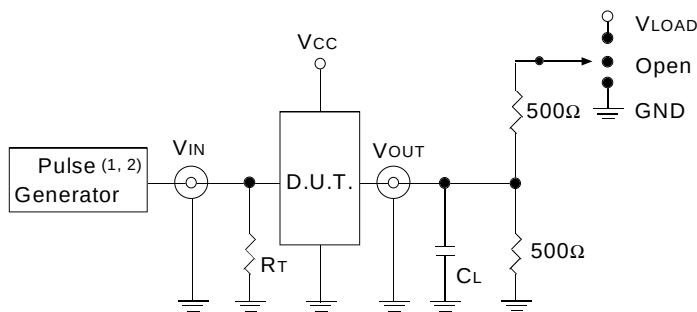
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(1)} = 2.7V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
V_{LOAD}	6	6	$2 \times V_{CC}$	V
V_{IH}	2.7	2.7	V_{CC}	V
V_T	1.5	1.5	$V_{CC} / 2$	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

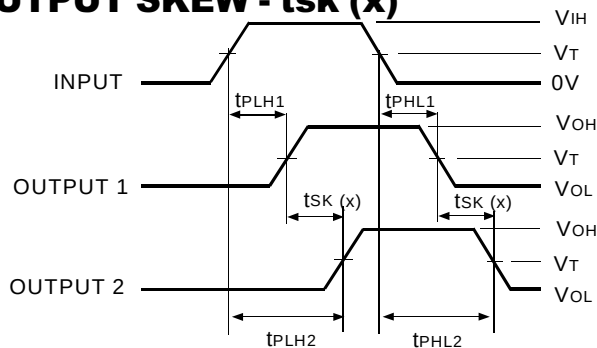
1. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$.
2. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_F \leq 2\text{ns}$; $t_R \leq 2\text{ns}$.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - $t_{SK}(x)$



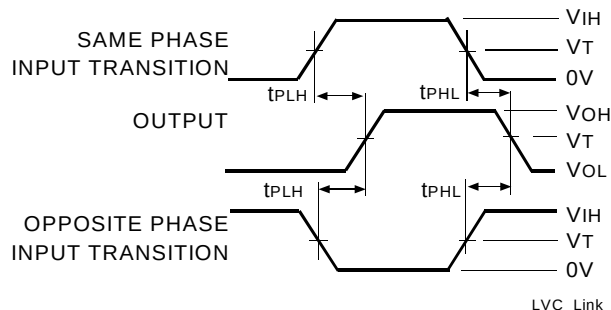
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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NOTES:

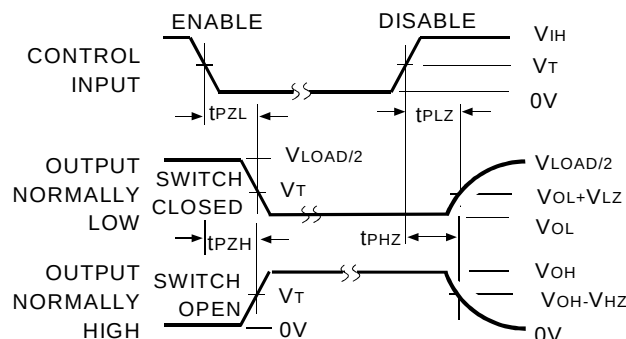
1. For $t_{SK}(o)$ OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK}(b)$ OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

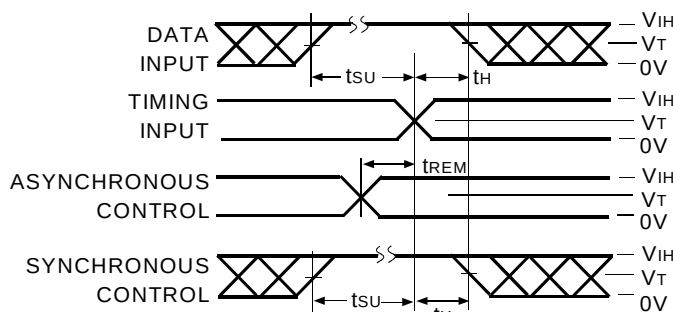


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NOTE:

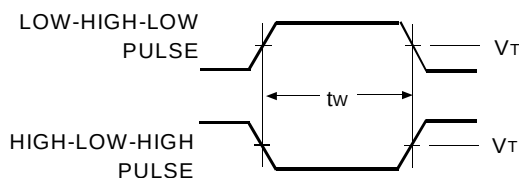
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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PULSE WIDTH



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IDT XX LVC X XXXX XX
Temp. Range Bus-Hold Device Type Package

SO	Small Outline IC (gull wing) (SO24-2)
PY	Shrink Small Outline Package (SO24-7)
Q	Quarter Size Small Outline Package (SO24-8)
PG	Thin Shrink Small Outline Package (SO24-9)
841A	10-Bit Bus-Interface D-Type Latch with 3-State Outputs, $\pm 24\text{mA}$
Blank	No Bus-hold
74	-40°C to $+85^{\circ}\text{C}$



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