



MOTOROLA

MC14051B MC14052B MC14053B

ANALOG MULTIPLEXERS/DEMULPLEXERS

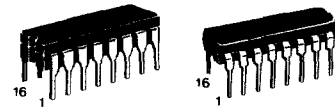
The MC14051B, MC14052B, and MC14053B analog multiplexers are digitally-controlled analog switches. The MC14051B effectively implements an SP8T solid state switch, the MC14052B a DP4T, and the MC14053B a Triple SPDT. All three devices feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range ($V_{DD} - V_{EE}$) = 3 to 18 V
Note: V_{EE} must be $\leq V_{SS}$
- Linearized Transfer Characteristics
- Low-Noise — 12 nV/ $\sqrt{\text{Cycle}}$, $f \geq 1$ kHz typical
- Pin-for-Pin Replacement for CD4051, CD4052, and CD4053
- For 4PDT Switch, See MC14551B
- For Lower R_{ON} , Use the HC4051, HC4052, or HC4053 High-Speed CMOS Devices

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

ANALOG MULTIPLEXERS/ DEMULPLEXERS



CASE 620
L SUFFIX
CERAMIC PACKAGE

CASE 648
P SUFFIX
PLASTIC PACKAGE

ORDERING INFORMATION

A Series: -55°C to $+125^{\circ}\text{C}$
MC14XXXBAL (Ceramic Package Only)

C Series: -40°C to $+85^{\circ}\text{C}$
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{EE} ; $V_{SS} \geq V_{EE}$)	-0.5 to $+18.0$	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient) (Referenced to V_{SS} for Control Inputs and V_{EE} for Switch I/O)	-0.5 to $V_{DD} + 0.5$	V
I_{in}	Input Current: (DC or Transient), per Control Pin	± 10	mA
I_{sw}	Switch Through Current	± 25	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to $+150$	$^{\circ}\text{C}$
T_L	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

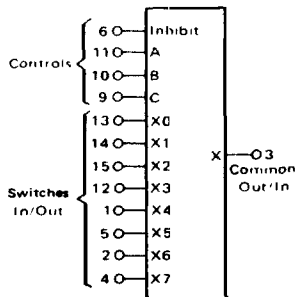
*Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic "P" Package: $-12\text{mW}/^{\circ}\text{C}$ from 65°C to 85°C

Ceramic "L" Package: $-12\text{mW}/^{\circ}\text{C}$ from 100°C to 125°C

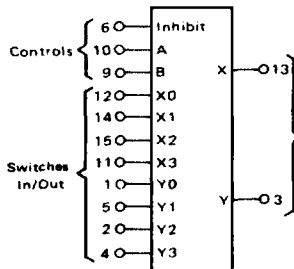
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MC14051B 8-Channel Analog Multiplexer/Demultiplexer



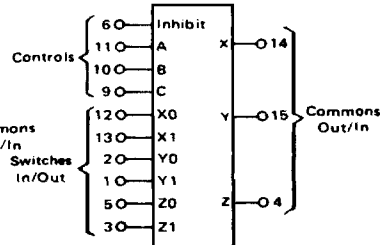
V_{DD} = Pin 16
 V_{SS} = Pin 8
 V_{EE} = Pin 7

MC14052B Dual 4-Channel Analog Multiplexer/Demultiplexer



V_{DD} = Pin 16
 V_{SS} = Pin 8
 V_{EE} = Pin 7

MC14053B Triple 2-Channel Analog Multiplexer/Demultiplexer



V_{DD} = Pin 16
 V_{SS} = Pin 8
 V_{EE} = Pin 7

Note: Control Inputs referenced to V_{SS} , Analog Inputs and Outputs reference to V_{EE} . V_{EE} must be $\leq V_{SS}$.

MC14051B•MC14052B•MC14053B

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V _{DD}	Test Conditions	T _{low} [*]		25°C			T _{high} [*]		Unit
				Min	Max	Min	Typ#	Max	Min	Max	
SUPPLY REQUIREMENTS (Voltages Referenced to V _{EE})											
Power Supply Voltage Range	V _{DD}	—	V _{DD} - 3 ≥ V _{SS} ≥ V _{EE}	3	18	3	—	18	3	18	V
Quiescent Current Per Package (AL Device)	I _{DD}	5	Control Inputs: V _{in} = V _{SS} or V _{DD} .	—	5	—	0.005	5	—	150	μA
		10	Switch I/O: V _{EE} ≤ V _{I/O} ≤ V _{DD} .	—	10	—	0.010	10	—	300	
		15	and ΔV _{switch} ≤ 500 mV**	—	20	—	0.015	20	—	600	
Quiescent Current Per Package (CL/CP Device)	I _{DD}	5	Control Inputs: V _{in} = V _{SS} or V _{DD} .	—	20	—	0.005	20	—	150	μA
		10	Switch I/O: V _{EE} ≤ V _{I/O} ≤ V _{DD} .	—	40	—	0.010	40	—	300	
		15	and ΔV _{switch} ≤ 500 mV**	—	80	—	0.015	80	—	600	
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I _{D(AV)}	5 10 15	T _A = 25°C only (The channel component, (V _{in} - V _{out})/R _{On} , is not included.)	Typical						(0.07 μA/kHz)f + I _{DD} (0.20 μA/kHz)f + I _{DD} (0.36 μA/kHz)f + I _{DD}	μA

CONTROL INPUTS — INHIBIT, A, B, C (Voltages Referenced to V_{SS})

Low-Level Input Voltage	V _{IL}	5	R _{on} = per spec.	—	1.5	—	2.25	1.5	—	1.5	V
		10	I _{off} = per spec	—	3.0	—	4.50	3.0	—	3.0	
		15		—	4.0	—	6.75	4.0	—	4.0	
High-Level Input Voltage	V _{IH}	5	R _{on} = per spec.	3.5	—	3.5	2.75	—	3.5	—	V
		10	I _{off} = per spec	7.0	—	7.0	5.50	—	7.0	—	
		15		11.0	—	11.0	8.25	—	11.0	—	
Input Leakage Current (AL Device)	I _{in}	15	V _{in} = 0 or V _{DD}	—	±0.1	—	±0.0001	±0.1	—	±1.0	μA
Input Leakage Current (CL/CP Device)	I _{in}	15	V _{in} = 0 or V _{DD}	—	±0.3	—	±0.0001	±0.3	—	±1.0	μA
Input Capacitance	C _{in}	—		—	—	—	5.0	7.5	—	—	pF

SWITCHES IN/OUT AND COMMONS OUT/IN - X, Y, Z (Voltages Referenced to V_{EE})

Recommended Peak-to-Peak Voltage Into or Out of the Switch	V _{I/O}	—	Channel On or Off	0	V _{DD}	0	—	V _{DD}	0	V _{DD}	V _{PP}
Recommended Static or Dynamic Voltage Across the Switch** (Figure 5)	ΔV _{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V _{OO}	—	V _{in} = 0 V, No load	—	—	—	10	—	—	—	μV
ON Resistance (AL Device)	R _{on}	5	ΔV _{switch} ≤ 500 mV**, V _{in} = V _{IL} or V _{IH} (Control), and V _{in} = 0 to V _{DD} (Switch)	—	800	—	250	1050	—	1300	Ω
		10		—	400	—	120	500	—	550	
		15		—	220	—	80	280	—	320	
ON Resistance (CL/CP Device)	R _{on}	5	ΔV _{switch} ≤ 500 mV**, V _{in} = V _{IL} or V _{IH} (Control), and V _{in} = 0 to V _{DD} (Switch)	—	880	—	250	1050	—	1200	Ω
		10		—	450	—	120	500	—	520	
		15		—	250	—	80	280	—	300	
Δ ON Resistance Between Any Two Channels in the Same Package	ΔR _{on}	5		—	70	—	25	70	—	135	Ω
		10		—	50	—	10	50	—	95	
		15		—	45	—	10	45	—	65	
Off-Channel Leakage Current (AL Device) (Figure 10)	I _{off}	15	V _{in} = V _{IL} or V _{IH} (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Off-Channel Leakage Current (CL/CP Device) (Figure 10)	I _{off}	15	V _{in} = V _{IL} or V _{IH} (Control) Channel to Channel or Any One Channel	—	±300	—	±0.05	±300	—	±1000	nA
Capacitance, Switch I/O	C _{I/O}	—	Inhibit = V _{DD}	—	—	—	10	—	—	—	pF
Capacitance, Common O/I	C _{O/I}	—	Inhibit = V _{DD} (MC14051B)	—	—	—	60	—	—	—	pF
		—	(MC14052B)	—	—	—	32	—	—	—	
		—	(MC14053B)	—	—	—	17	—	—	—	
Capacitance, Feedthrough (Channel Off)	C _{I/O}	—	Pins Not Adjacent	—	—	—	0.15	—	—	—	pF
		—	Pins Adjacent	—	—	—	0.47	—	—	—	

* T_{low} = -55°C for AL Device, -40° for CL/CP Device

T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance

**For voltage drops across the switch (ΔV_{switch}) > 600 mV (>300 mV at high temperature), excessive V_{DD} current may be drawn, i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

MC14051B•MC14052B•MC14053B

ELECTRICAL CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$) ($V_{EE} \leq V_{SS}$ unless otherwise indicated)

Characteristic	Symbol	$V_{DD}-V_{EE}$ V_{dc}	Typ # All Types	Max	Unit
Propagation Delay Times (Figure 6) Switch Input to Switch Output ($R_L = 10 \text{ k}\Omega$) MC14051 $t_{PLH}, t_{PHL} = (0.17 \text{ ns/pF}) C_L + 26.5 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.08 \text{ ns/pF}) C_L + 11 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.06 \text{ ns/pF}) C_L + 9.0 \text{ ns}$ MC14052 $t_{PLH}, t_{PHL} = (0.17 \text{ ns/pF}) C_L + 21.5 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.08 \text{ ns/pF}) C_L + 8.0 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.06 \text{ ns/pF}) C_L + 7.0 \text{ ns}$ MC14053 $t_{PLH}, t_{PHL} = (0.17 \text{ ns/pF}) C_L + 16.5 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.08 \text{ ns/pF}) C_L + 4.0 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.06 \text{ ns/pF}) C_L + 3.0 \text{ ns}$ Inhibit to Output ($R_L = 10 \text{ k}\Omega$, $V_{EE} = V_{SS}$) Output "1" or "0" to High Impedance, or High Impedance to "1" or "0" Level MC14051B	t_{PLH}, t_{PHL}	5.0 10 15	35 15 12	90 40 30	ns
MC14052B		5.0 10 15	30 12 10	75 30 25	ns
MC14053B		5.0 10 15	25 8.0 6.0	65 20 15	ns
Control Input to Output ($R_L = 10 \text{ k}\Omega$, $V_{EE} = V_{SS}$) MC14051B	$t_{PHZ}, t_{PLZ},$ t_{PZH}, t_{PZL}	5.0 10 15	350 170 140	700 340 280	ns
MC14052B		5.0 10 15	300 155 125	600 310 250	ns
MC14053B		5.0 10 15	275 140 110	550 280 220	ns
Control Input to Output ($R_L = 10 \text{ k}\Omega$, $V_{EE} = V_{SS}$) MC14051B	t_{PLH}, t_{PHL}	5.0 10 15	360 160 120	720 320 240	ns
MC14052B		5.0 10 15	325 130 90	650 260 180	ns
MC14053B		5.0 10 15	300 120 80	600 240 160	ns
Second Harmonic Distortion ($R_L = 10 \text{ k}\Omega$, $f = 1 \text{ kHz}$) $V_{in} = 5 V_{pp}$	—	10	0.07	—	%
Bandwidth (Figure 7) ($R_L = 1 \text{ k}\Omega$, $V_{in} = 1/2 (V_{DD} - V_{EE}) \text{ p-p}$, $C_L = 50 \text{ pF}$) $20 \text{ Log } \frac{V_{out}}{V_{in}} = -3 \text{ dB}$	BW	10	17	—	MHz
Off Channel Feedthrough Attenuation (Figure 7) $R_L = 1 \text{ k}\Omega$, $V_{in} = 1/2 (V_{DD} - V_{EE}) \text{ p-p}$ $f_{in} = 4.5 \text{ MHz} \rightarrow \text{MC14051B}$ $f_{in} = 30 \text{ MHz} \rightarrow \text{MC14052B}$ $f_{in} = 55 \text{ MHz} \rightarrow \text{MC14053B}$	—	10	-50	—	dB
Channel Separation (Figure 8) ($R_L = 1 \text{ k}\Omega$, $V_{in} = 1/2 (V_{DD} - V_{EE}) \text{ p-p}$) $f_{in} = 3.0 \text{ MHz}$	—	10	-50	—	dB
Crosstalk, Control Input to Common O/I (Figure 9) ($R_1 = 1 \text{ k}\Omega$, $R_L = 10 \text{ k}\Omega$) Control $t_{TLH} = t_{THL} = 20 \text{ ns}$, Inhibit = V_{SS})	—	10	75	—	mV

*The formulas given are for the typical characteristics only at 25°C .

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} , V_{EE} , or V_{DD}). Unused outputs must be left open.

MC14051B•MC14052B•MC14053B

FIGURE 1 – SWITCH CIRCUIT SCHEMATIC

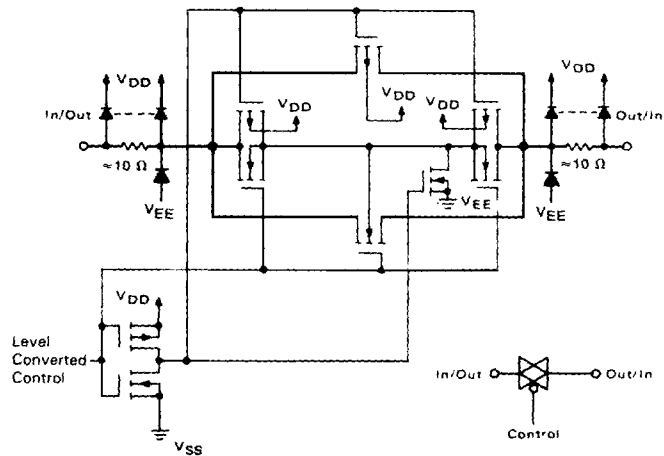
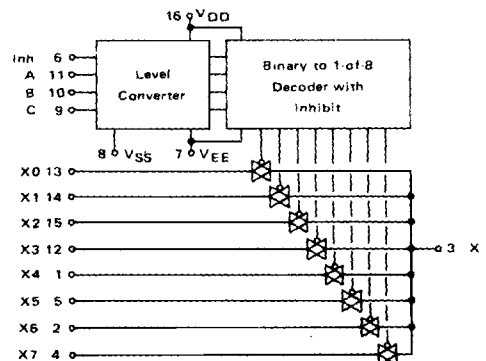


FIGURE 2 – MC14051B FUNCTIONAL DIAGRAM



TRUTH TABLE

Control Inputs			ON Switches					
Inhibit	Select		MC14051B			MC14052B		
	C*	B	A					
0	0	0	0	X0	Y0	X0	Z0	Y0
0	0	0	1	X1	Y1	X1	Z0	Y0
0	0	1	0	X2	Y2	X2	Z0	Y1
0	0	1	1	X3	Y3	X3	Z0	Y1
0	1	0	0	X4			Z1	Y0
0	1	0	1	X5			Z1	Y0
0	1	1	0	X6			Z1	Y1
0	1	1	1	X7			Z1	Y1
1	x	x	x	None	None	None	None	None

*Not applicable for MC14052
x = Don't Care

FIGURE 3 – MC14052B FUNCTIONAL DIAGRAM

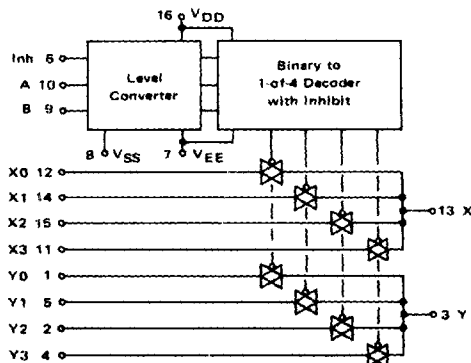
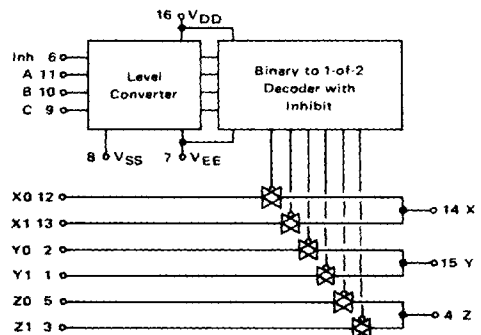


FIGURE 4 – MC14053B FUNCTIONAL DIAGRAM



MC14051B•MC14052B•MC14053B

TEST CIRCUITS

FIGURE 5 — ΔV ACROSS SWITCH

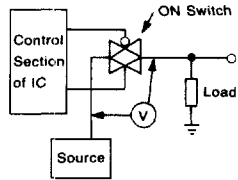


FIGURE 6 — PROPAGATION DELAY TIMES, CONTROL AND INHIBIT TO OUTPUT

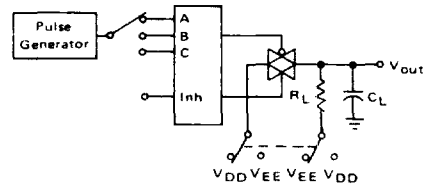


FIGURE 7 — BANDWIDTH AND OFF-CHANNEL FEEDTHROUGH ATTENUATION

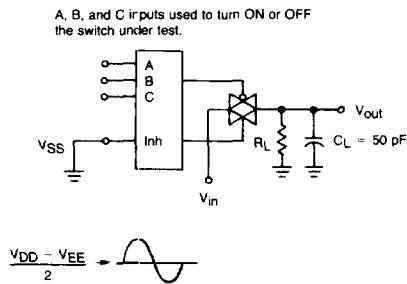


FIGURE 8 — CHANNEL SEPARATION (ADJACENT CHANNELS USED FOR SETUP)

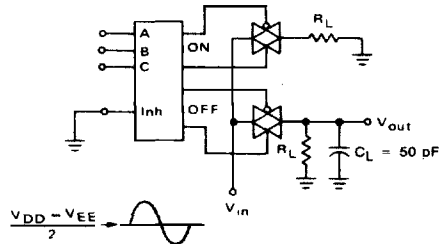


FIGURE 9 — CROSSTALK, CONTROL INPUT TO COMMON O/I

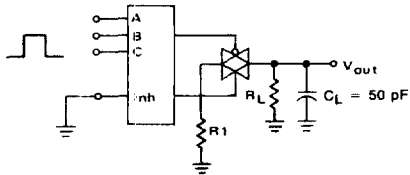
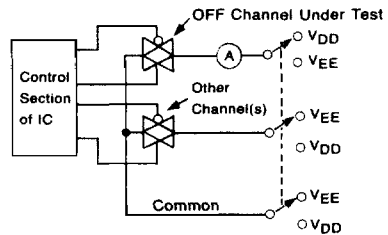
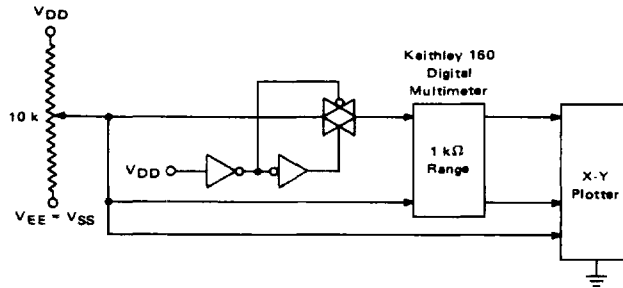


FIGURE 10 — OFF CHANNEL LEAKAGE



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FIGURE 11 – CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 12 – $V_{DD} = 7.5 \text{ V}$, $V_{EE} = -7.5 \text{ V}$

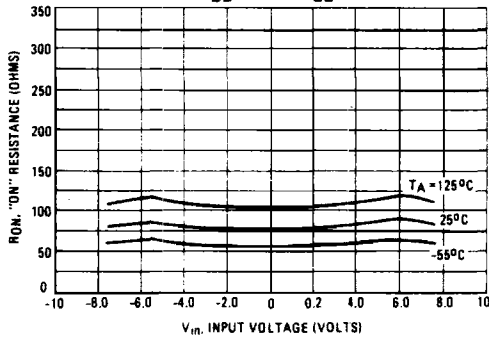


FIGURE 13 – $V_{DD} = 5.0 \text{ V}$, $V_{EE} = -5.0 \text{ V}$

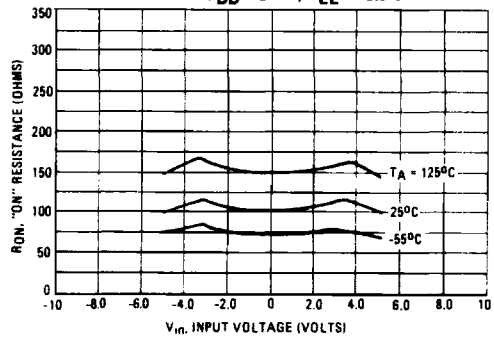


FIGURE 14 – $V_{DD} = 2.5 \text{ V}$, $V_{EE} = -2.5 \text{ V}$

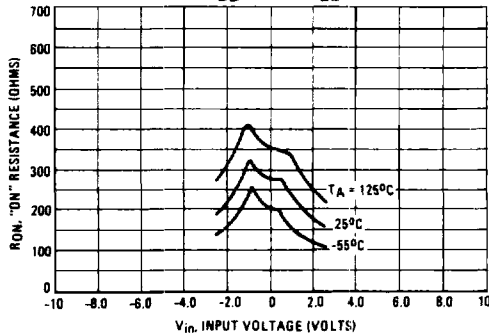
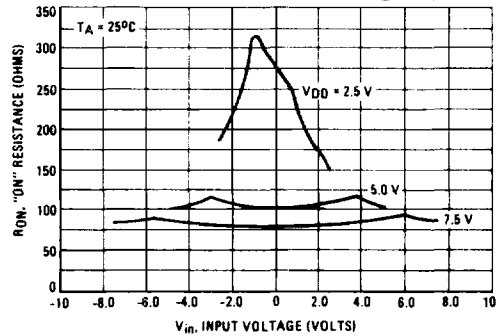
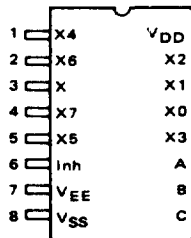


FIGURE 15 – COMPARISON AT 25°C, $V_{DD} = -V_{EE}$

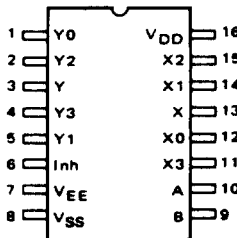


MC14051B

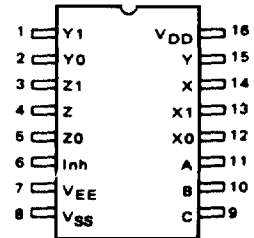


PIN ASSIGNMENT

MC14052B



MC14053B



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APPLICATIONS INFORMATION

Figure A illustrates use of the on-chip level converter detailed in Figures 2, 3, and 4. The 0-to-5 V Digital Control signal is used to directly control a 9 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = +5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{VEE}. The V_{DD} voltage determines the maximum recommended peak above V_{SS}. The V_{VEE} voltage determines the maximum swing below V_{SS}. For the example, V_{DD} - V_{SS} = 5 V maximum swing above V_{SS}; V_{SS} - V_{VEE} = 5 V maximum swing below V_{SS}. The example shows a ± 4.5 V

signal which allows a ½ volt margin at each peak. If voltage transients above V_{DD} and/or below V_{VEE} are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{VEE} is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V_{DD} and V_{VEE}.

Balanced supplies are not required. However, V_{SS} must be greater than or equal to V_{VEE}. For example, V_{DD} = +10 V, V_{SS} = +5 V, and V_{VEE} = -3 V is acceptable. See the Table below.

FIGURE A — APPLICATION EXAMPLE

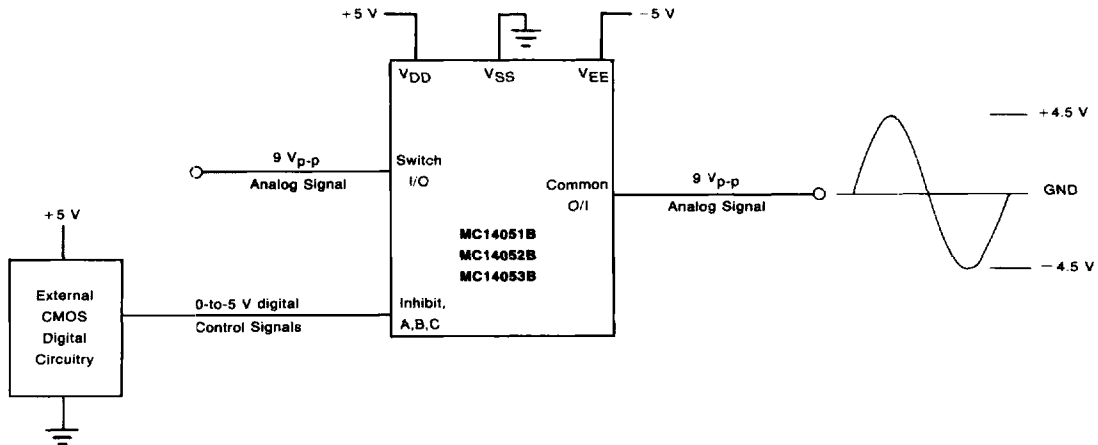
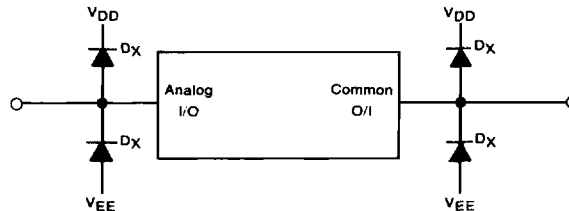


FIGURE B — EXTERNAL GERMANIUM OR SCHOTTKY CLIPPING DIODES



POSSIBLE SUPPLY CONNECTIONS

V _{DD} in Volts	V _{SS} in Volts	V _{VEE} in Volts	Control Inputs Logic High/Logic Low in Volts	Maximum Analog Signal Range in Volts
+8	0	-8	+8/0	+8 to -8 = 16 V _{p-p}
+5	0	-12	+5/0	+5 to -12 = 17 V _{p-p}
+5	0	0	+5/0	+5 to 0 = 5 V _{p-p}
+5	0	-5	+5/0	+5 to -5 = 10 V _{p-p}
+10	+5	-5	+10/+5	+10 to -5 = 15 V _{p-p}