Rochester Electronics

Datasheet

PART NUMBER

54AC377^SSA

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate to MIL-PRF-38535 requirements. Editorial changes throughout. - jak	03-06-11	Thomas M. Hess
B	Update test condition for high level output voltage (V_{OH}) and low level output voltage (V_{OL}) in table I. Update boilerplate paragraphs to MIL-PRF-38535 requirement. - jak	10-02-12	Thomas M. Hess
C	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	18-01-30	Thomas M. Hess
D	Update devices supplier CAGE code 3V146 information to bulletin page. Update boilerplate paragraphs to MIL-PRF-38535 requirements. - TTM	23-07-27	Muhammad A. Akbar

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets

REV																						
SHEET																						
REV	D	D	D	D	D	D	D	D	D	D	D											
SHEET	1	2	3	4	5	6	7	8	9	10	11											

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

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DRAWING APPROVAL DATE
88-09-06

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, OCTAL D-TYPE FLIP-FLOP WITH CLOCK ENABLE, MONOLITHIC SILICON

AMSC N/A	REVISION LEVEL D	SIZE A	CAGE CODE **67268**	**5962-88702**
		SHEET 1 OF 11		

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-88702	01	R	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54AC377	Octal D-type flip-flop with clock enable

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
2	CQCC1-N20	20	Leadless-chip-carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC}) ..... -0.5 V dc to +6.0 V dc maximum
DC input voltage range (V_{IN}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
Clamp diode current (I_{IK}, I_{OK}) ..... ±20 mA
DC output current (per pin) (I_{OUT}) ..... ±50 mA
DC V_{CC} or GND current (I_{CC}, I_{GND}) ..... ±100 mA
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 500 mW
Lead temperature (soldering, 10 seconds) ..... +245°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C 3/

1.4 Recommended operating conditions. 2/

Supply voltage range (V_{CC}) ..... +3.0 V dc to 5.5 V dc 4/
Input voltage range (V_{IN}) ..... 0.0 V dc to V_{CC}
Output voltage range (V_{OUT}) ..... 0.0 V dc to V_{CC}
Case operating temperature range (T_C) ..... -55°C to +125°C
Input rise and fall rate ($\Delta t/\Delta V$):
V_{CC} = 3.6 V or V_{CC} = 5.5 V ..... 0 to 8 ns/V

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise specified, all voltages are referenced to ground.
3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
4/ Operation from 2.0 V dc to 3.0 V dc is provided for compatibility with data retention and battery back-up systems. Data retention implies no input transition and no stored data loss with the following conditions: $V_{IH} \geq 70\%\ V_{CC}$, $V_{IL} \leq 30\%\ V_{CC}$, $V_{OH} \geq 70\%\ V_{CC}$ @ -20 μA, $V_{OL} \leq 30\%\ V_{CC}$ @ 20 μA.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD20 - Standard for Description of 54/74ACXXXXX and 54/74ACTXXXXX Advanced High-Speed CMOS Devices.

(Copies of these documents are available online at https://www.jedec.org/.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Limits 2/		Unit
					Min	Max	
High-level output voltage 3006	V_{OH} 3/	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\ \mu A$	$V_{CC} = 3.0\ V$	1, 2, 3	2.9		V
			$V_{CC} = 4.5\ V$		4.4		
			$V_{CC} = 5.5\ V$		5.4		
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4\ mA$	$V_{CC} = 3.0\ V$		2.4		
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -24\ mA$	$V_{CC} = 4.5\ V$		3.7		
			$V_{CC} = 5.5\ V$		4.7		
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\ mA$	$V_{CC} = 5.5\ V$		3.85		
Low-level output voltage 3006	V_{OL} 3/	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\ \mu A$	$V_{CC} = 3.0\ V$	1, 2, 3		0.1	
			$V_{CC} = 4.5\ V$			0.1	
			$V_{CC} = 5.5\ V$			0.1	
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 12\ mA$	$V_{CC} = 3.0\ V$			0.5	
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 24\ mA$	$V_{CC} = 4.5\ V$			0.5	
			$V_{CC} = 5.5\ V$			0.5	
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\ mA$	$V_{CC} = 5.5\ V$			1.65	
High-level input voltage	V_{IH} 4/		$V_{CC} = 3.0\ V$	1, 2, 3	2.1		V
			$V_{CC} = 4.5\ V$		3.15		
			$V_{CC} = 5.5\ V$		3.85		
Low-level input voltage	V_{IL} 4/		$V_{CC} = 3.0\ V$	1, 2, 3		0.9	
			$V_{CC} = 4.5\ V$			1.35	
			$V_{CC} = 5.5\ V$			1.65	
Input leakage current low 3009	I_{IL}	$V_{IN} = 0.0\ V$	$V_{CC} = 5.5\ V$	1, 2, 3		-1.0	µA
Input leakage current high 3010	I_{IH}	$V_{IN} = 5.5\ V$	$V_{CC} = 5.5\ V$	1, 2, 3		1.0	
Quiescent supply current 3005	I_{CC}	$V_{IN} = V_{CC}$ or GND	$V_{CC} = 5.5\ V$	1, 2, 3		160	µA
Input capacitance 3012	C_{IN}	See 4.3.1c		4		8.0	pF
Power dissipation capacitance	C_{PD} 5/	See 4.3.1c		4		120	pF
Functional tests 3014	6/	Tested at $V_{CC} = 3.0\ V$ and repeated at $V_{CC} = 5.5\ V$, see 4.3.1d		7, 8	L	H	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions -55°C ≤ T_C ≤ +125°C 3.0 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified		Group A subgroups	Limits 2/		Unit
					Min	Max	
Propagation delay time, CP to On 3003	t_{PHL}, t_{PLH} 7/	C_L = 50 pF R_L = 500Ω See figure 4	V_{CC} = 3.0 V	9	1.0	12.0	ns
			V_{CC} = 4.5 V		1.0	9.0	
			V_{CC} = 3.0 V	10, 11	1.0	15.0	
			V_{CC} = 4.5 V		1.0	11.0	
Input set-up time, Dn to CP	t_{s1}		V_{CC} = 3.0 V	9	6.5		ns
			V_{CC} = 4.5 V		5.0		
			V_{CC} = 3.0 V	10, 11	7.5		
			V_{CC} = 4.5 V		6.0		
Input hold time, Dn from CP	t_{h1}		V_{CC} = 3.0 V	9	1.0		ns
			V_{CC} = 4.5 V		2.0		
			V_{CC} = 3.0 V	10, 11	1.5		
			V_{CC} = 4.5 V		2.5		
Input set-up time, $\overline{CE}$ to CP	t_{s2}		V_{CC} = 3.0 V	9	7.0		ns
			V_{CC} = 4.5 V		5.0		
			V_{CC} = 3.0 V	10, 11	9.5		
			V_{CC} = 4.5 V		6.0		
Input hold time, $\overline{CE}$ from CP	t_{h2}		V_{CC} = 3.0 V	9	0.0		ns
			V_{CC} = 4.5 V		1.0		
			V_{CC} = 3.0 V	10, 11	1.0		
			V_{CC} = 4.5 V		2.0		
Pulse width, CP	t_w		V_{CC} = 3.0 V	9	5.5		ns
			V_{CC} = 4.5 V		5.0		
			V_{CC} = 3.0 V	10, 11	6.5		
			V_{CC} = 4.5 V		5.0		
Maximum frequency, CP	f_{MAX}		V_{CC} = 3.0 V	9	85		MHz
			V_{CC} = 4.5 V		95		
			V_{CC} = 3.0 V	10, 11	75		
			V_{CC} = 4.5 V		95		

1/ For tests not listed in the referenced MIL-STD-883 (e.g. C_{PD}), utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table I herein.

2/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

3/ The V_{OH} and V_{OL} tests shall be tested at V_{CC} = 3.0 V and 4.5 V. The V_{OH} and V_{OL} tests are guaranteed, if not tested, for other values of V_{CC}. Limits shown apply to operation at V_{CC} = 3.3 V ±0.3 V and V_{CC} = 5.0 V ±0.5 V. Tests with input current at +50 mA or -50 mA are performed on only one input at a time with duration not to exceed 2 ms. Transmission driving tests may be performed using V_{IN} = V_{CC} or GND. When V_{IN} = V_{CC} or GND is used, the test is guaranteed for V_{IN} = V_{IH} minimum and V_{IL} maximum.

4/ V_{IH} and V_{IL} tests are not required, and shall be applied as forcing functions for V_{OH} and V_{OL} tests.

TABLE I. Electrical performance characteristics – Continued.

5/ Power dissipation capacitance (C_{PD}) determines both the power consumption (P_D) and dynamic current consumption (I_S). Where:

$P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC})$

$I_S = (C_{PD} + C_L) V_{CC}f + I_{CC}$

f is the frequency of the input signal and C_L is the external output load capacitance.

6/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. For V_{OUT} measurements, $L \leq 0.3V_{CC}$ and $H \geq 0.7V_{CC}$.

7/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. AC limits at V_{CC} = 3.6 V are equal to limits at V_{CC} = 3.0 V and guaranteed by testing at V_{CC} = 3.0 V. Minimum propagation delay limits for V_{CC} = 5.5 V and V_{CC} = 3.6V are 1.0 ns and guaranteed by guardbanding the V_{CC} = 4.5 V and V_{CC} = 3.0 V, respectively, minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.

Device type	01
Case outline	R, S and 2
Terminal number	Terminal symbol
1	$\overline{CE}$
2	O0
3	D0
4	D1
5	O1
6	O2
7	D2
8	D3
9	O3
10	GND
11	CP
12	O4
13	D4
14	D5
15	O5
16	O6
17	D6
18	D7
19	O7
20	V_{CC}

FIGURE 1. Terminal connections.

	Inputs		Outputs
CP	$\overline{CE}$	Dn	On
↑	l	h	H
↑	l	l	L
↑	h	X	NC
X	H	X	NC

H = High voltage level (steady state)
L = Low voltage level (steady state)
l = Low one setup time prior to clock pulse
h = High one setup time prior to clock pulse
X = Immaterial
↑ = Low-to-high transition of the clock
NC = No change

FIGURE 2. Truth table.

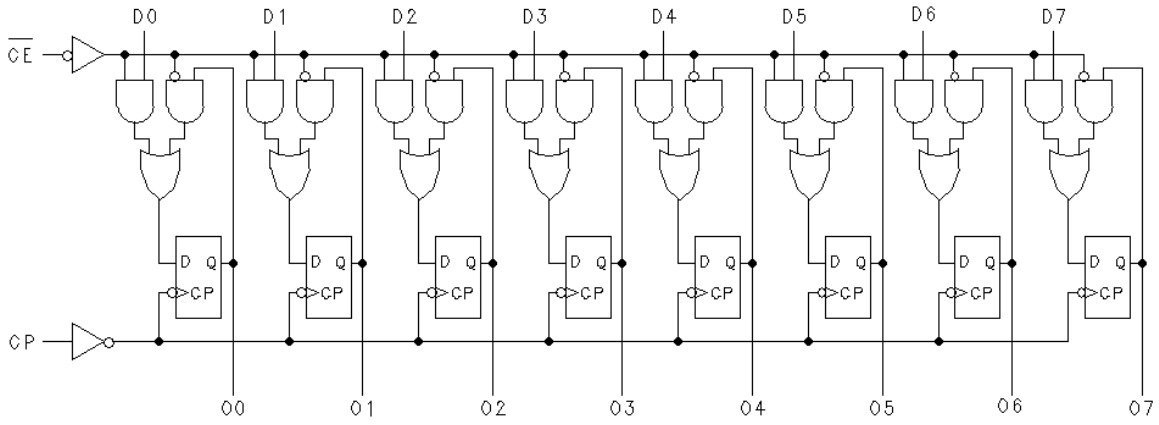
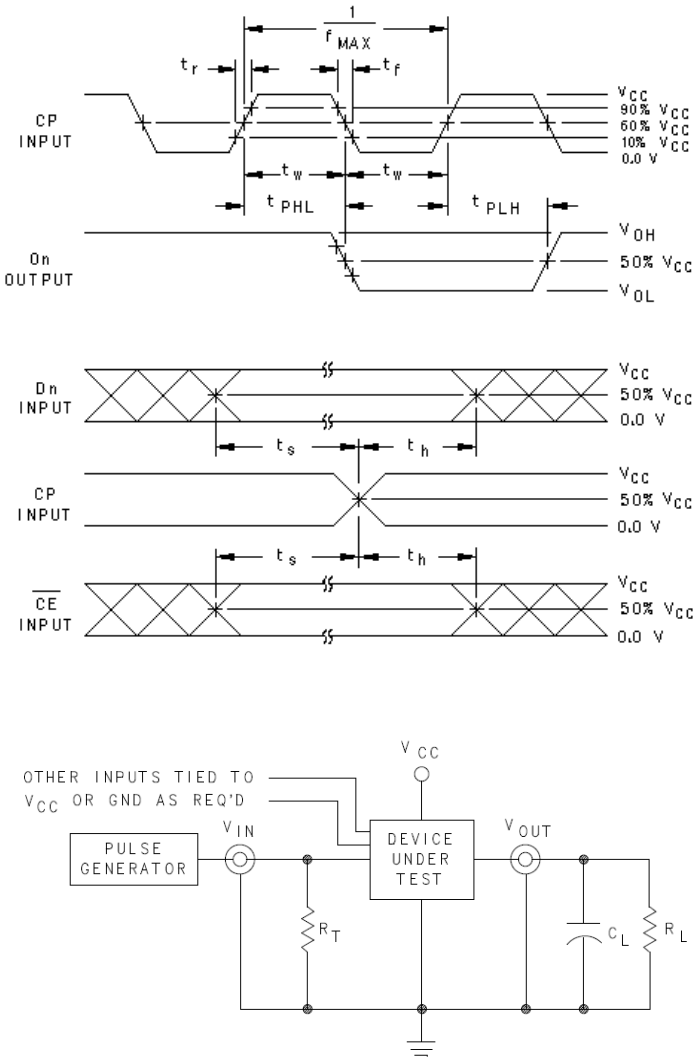


FIGURE 3. Logic diagram.



NOTES:

1. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
2. R_T = 50Ω or equivalent. R_L = 500Ω or equivalent.
3. Input signal from pulse generator: V_{IN} = 0.0 V to V_{CC}; PRR ≤ 10 MHz; t_r ≤ 3 ns; t_f ≤ 3 ns; t_r and t_f shall be measured from 10% of V_{CC} to 90% of V_{CC} and from 90% of V_{CC} to 10% of V_{CC}, respectively; duty cycle = 50 percent.
4. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
5. Outputs are measured one at a time with one output per measurement.

FIGURE 4. Switching waveforms and test circuit.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

1/ PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{PD} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Test all applicable pins on 5 devices with zero failures.

d. Subgroups 7 and 8 shall verify the truth table as specified in figure 2 herein.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 23-07-27

Approved sources of supply for SMD 5962-88702 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at: https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8870201RA	3/	54AC377DMQB
	3V146	54AC377/QRA
5962-8870201SA	3/	54AC377FMQB
	3V146	54AC377/QSA
5962-88702012A	3/	54AC377LMQB
	3V146	54AC377/Q2A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
3V146	Rochester Electronics, LLC 16 Malcolm Hoyt Drive Newburyport, MA 01950