

General Description

The AGM308MA combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

This device is ideal for load switch and battery protection applications.

Features

- Advance high cell density Trench technology
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance
- 100% Avalanche tested
- 100% DVDS tested

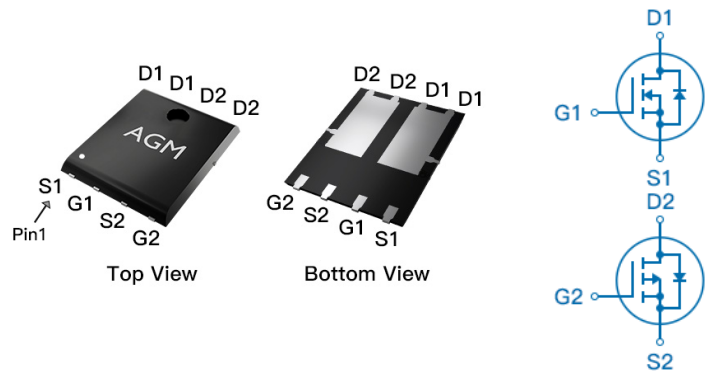
Application

- MB/VGA Vcore
- SMPS 2nd Synchronous Rectifier
- POL application
- BLDC Motor driver

Product Summary

BVDSS	RDSON	ID
30V	11mΩ	30A
-30V	12mΩ	-30A

PDFN5*6 Pin Configuration



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
AGM308MA	AGM308MA	PDFN5*6	330mm	12mm	3000

Table 1. Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$)

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
V_{DS}	Drain-Source Voltage ($V_{GS}=0V$)	30	-30	V
V_{GS}	Gate-Source Voltage ($V_{DS}=0V$)	± 20	± 20	V
I_D	Drain Current-Continuous($T_C=25^{\circ}\text{C}$) (Note 1)	30	-30	A
	Drain Current-Continuous($T_C=100^{\circ}\text{C}$)	18	-18	A
IDM (pluse)	Drain Current-Pulsed (Note 2)	120	-120	A
P_D	Total Power Dissipation($T_C=25^{\circ}\text{C}$)	37	37	W
	Total Power Dissipation($T_C=100^{\circ}\text{C}$)	15	15	W
EAS	Avalanche energy (Note 3)	45	65	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 150	-55 To 150	$^{\circ}\text{C}$

Table 2. Thermal Characteristic

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient (Steady State) ¹	---	20	$^{\circ}\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	3.4	$^{\circ}\text{C/W}$

Table 3. N- Channel Electrical Characteristics (TJ=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BVDSS	Drain-Source Breakdown Voltage	VGS=0V ID=250μA	30	--	--	V
IDSS	Zero Gate Voltage Drain Current	VDS=30V,VGS=0V	--	--	1	μA
IGSS	Gate-Body Leakage Current	VGS=±20V,VDS=0V	--	--	±100	nA
VGS(th)	Gate Threshold Voltage	VDS=VGS,ID=250μA	1.2	1.6	2.2	V
gFS	Forward Transconductance	VDS=5V,ID=10A	--	12	--	S
RDS(on)	Drain-Source On-State Resistance	VGS=10V, ID=20A	--	11	14	mΩ
		VGS=4.5V, ID=10A	--	15	22	mΩ
Dynamic Characteristics						
Ciss	Input Capacitance	VDS=15V,VGS=0V, F=1MHZ	--	850	--	pF
Coss	Output Capacitance		--	130	--	pF
Crss	Reverse Transfer Capacitance		--	98	--	pF
Rg	Gate resistance	VGS=0V, VDS=0V,f=1.0MHz	--	1.9	--	Ω
Switching Times						
td(on)	Turn-on Delay Time	VGS=10V,VDS=15V, RL=0.75Ω,RGEN=3Ω	--	4.7	--	nS
tr	Turn-on Rise Time		--	11	--	nS
td(off)	Turn-Off Delay Time		--	17	--	nS
tf	Turn-Off Fall Time		--	5.6	--	nS
Qg	Total Gate Charge	VGS=10V, VDS=15V, ID=10A	--	16	--	nC
Qgs	Gate-Source Charge		--	3.0	--	nC
Qgd	Gate-Drain Charge		--	3.8	--	nC
Source-Drain Diode Characteristics						
ISD	Source-Drain Current(Body Diode)		--	--	28	A
VSD	Forward on Voltage	VGS=0V,IS=20A	--	--	1.2	V
trr	Reverse Recovery Time	IF=20A , dI/dt=100A/μs , TJ=25℃	--	--	--	ns
Qrr	Reverse Recovery Charge		--	--	--	nc

Notes 1.The maximum current rating is package limited.

Notes 2.Repetitive Rating: Pulse width limited by maximum junction temperature

Notes 3.EAS condition: TJ=25°C

Table 3. P-Channel Electrical Characteristics (TJ=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BVDSS	Drain-Source Breakdown Voltage	VGS=0V ID=-250μA	-30	--	--	V
IDSS	Zero Gate Voltage Drain Current	VDS=-30V,VGS=0V	--	--	-1	μA
IGSS	Gate-Body Leakage Current	VGS=±20V,VDS=0V	--	--	±100	nA
VGS(th)	Gate Threshold Voltage	VDS=VGS,ID=-250μA	-1.2	-1.7	-2.2	V
gFS	Forward Transconductance	VDS=-10V,ID=-10A	--	12	--	S
RDS(on)	Drain-Source On-State Resistance	VGS=-10V, ID=-10A	--	12	14.5	mΩ
		VGS=-4.5V, ID=-5A	--	17	22	mΩ
Dynamic Characteristics						
Ciss	Input Capacitance	VDS=-15V,VGS=0V, F=1MHZ	--	1500	--	pF
Coss	Output Capacitance		--	200	--	pF
Crss	Reverse Transfer Capacitance		--	300	--	pF
Rg	Gate resistance	VGS=0V, VDS=0V,f=1.0MHz	--	4.5	--	Ω
Switching Times						
td(on)	Turn-on Delay Time	VGS=-10V,VDS=-15V, ID=-15A,RGEN=3.3Ω	--	10	--	nS
tr	Turn-on Rise Time		--	10.6	--	nS
td(off)	Turn-Off Delay Time		--	31.8	--	nS
tf	Turn-Off Fall Time		--	10.4	--	nS
Qg	Total Gate Charge	VGS=-10V, VDS=-15V, ID=-12A	--	39	--	nC
Qgs	Gate-Source Charge		--	7.0	--	nC
Qgd	Gate-Drain Charge		--	13	--	nC
Source-Drain Diode Characteristics						
ISD	Source-Drain Current(Body Diode)		--	--	-28	A
VSD	Forward on Voltage	VGS=0V,IS=-20A	--	--	-1.2	V
trr	Reverse Recovery Time	IF=-20A , dI/dt=100A/μs , TJ=25℃	--	--	--	ns
Qrr	Reverse Recovery Charge		--	--	--	nc

Notes 1. The maximum current rating is package limited.

Notes 2. Repetitive Rating: Pulse width limited by maximum junction temperature

Notes 3. EAS condition: TJ=25°C

•N Channel characteristics curve

Fig.1 Power Dissipation Derating Curve

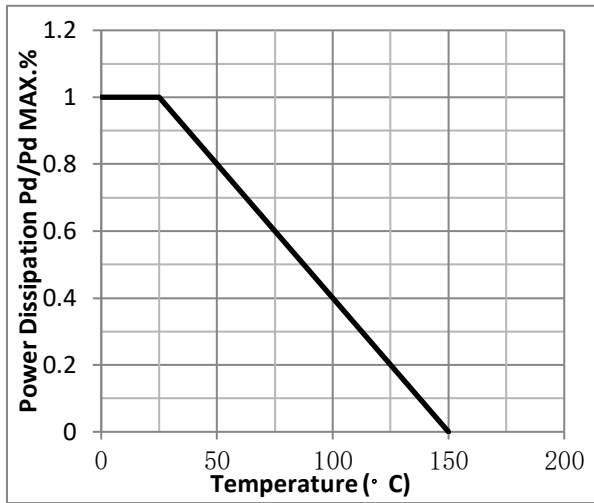


Fig.2 Typical output Characteristics

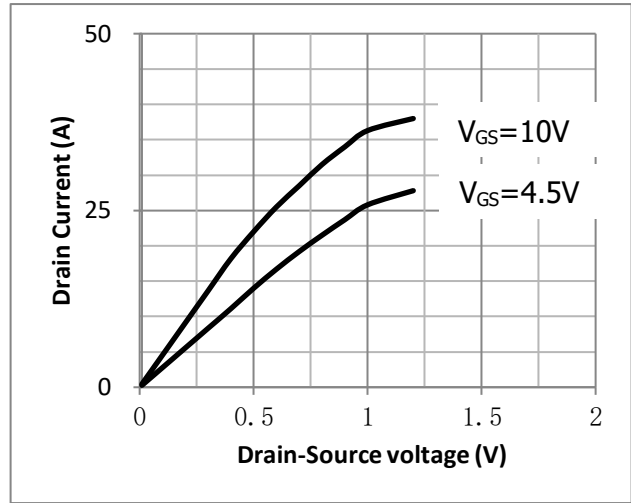


Fig.3 Threshold Voltage V.S Junction Temperature

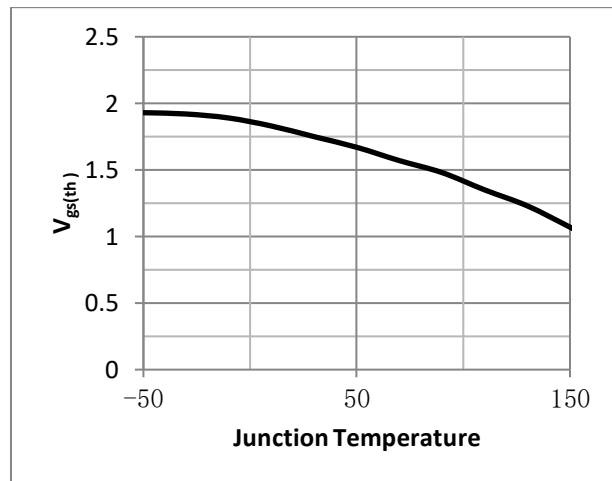


Fig.4 Resistance V.S Drain Current

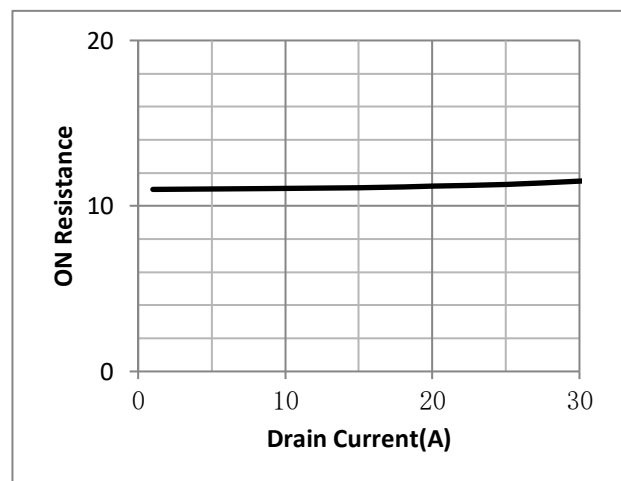


Fig.5 On-Resistance VS Gate Source Voltage

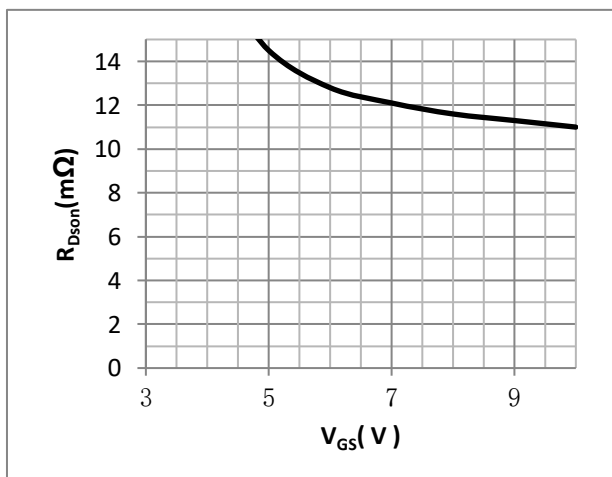
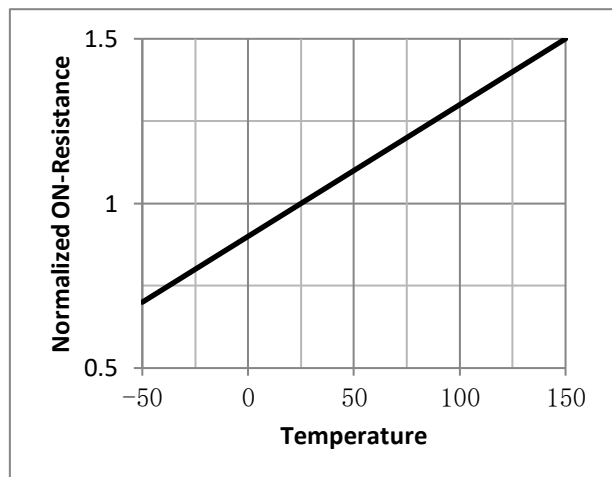


Fig.6 On-Resistance V.S Junction Temperature



•P Typical Characteristics

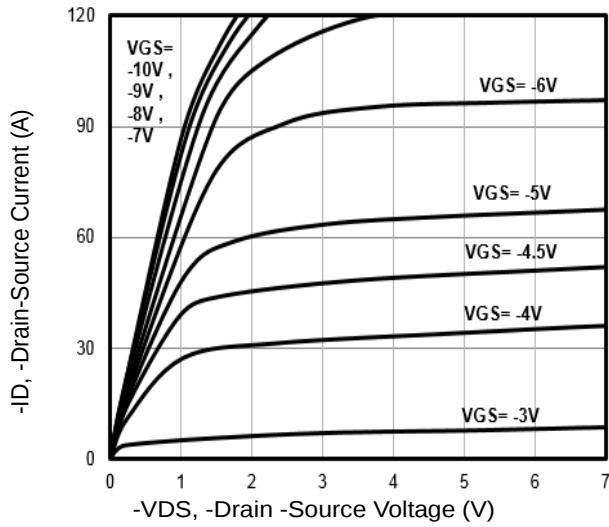


Fig1. Typical Output Characteristics

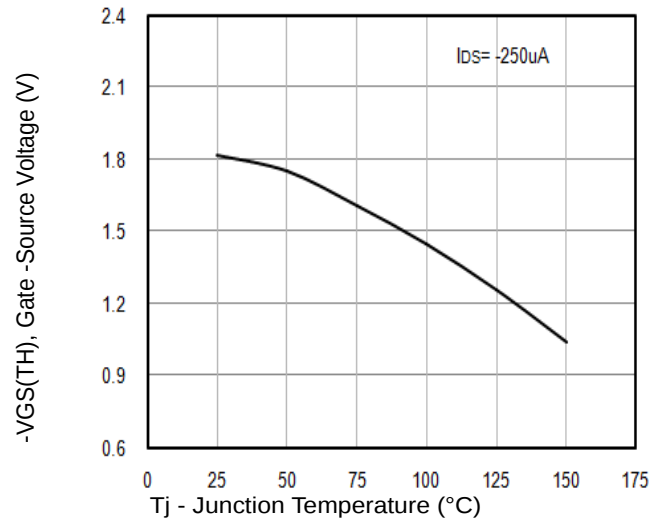


Fig2. $-V_{GS(TH)}$ Gate -Source Voltage Vs. T_j

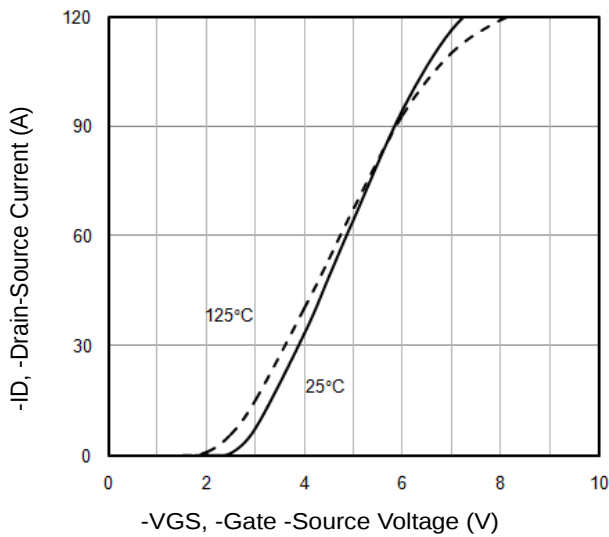


Fig3. Typical Transfer Characteristics

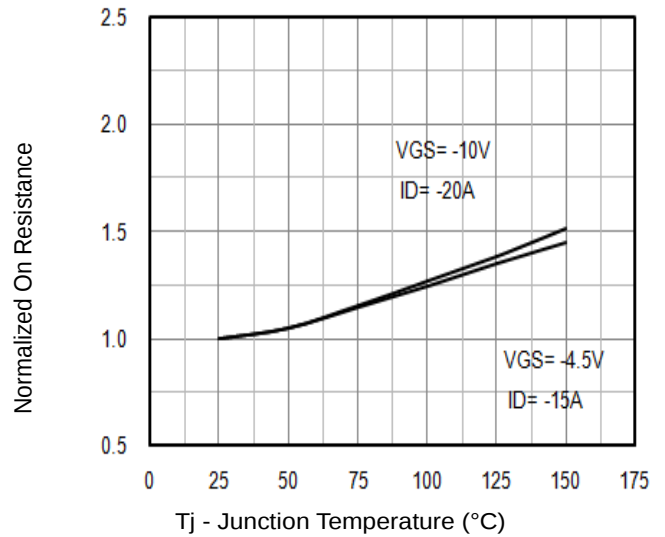


Fig4. Normalized On-Resistance Vs. T_j

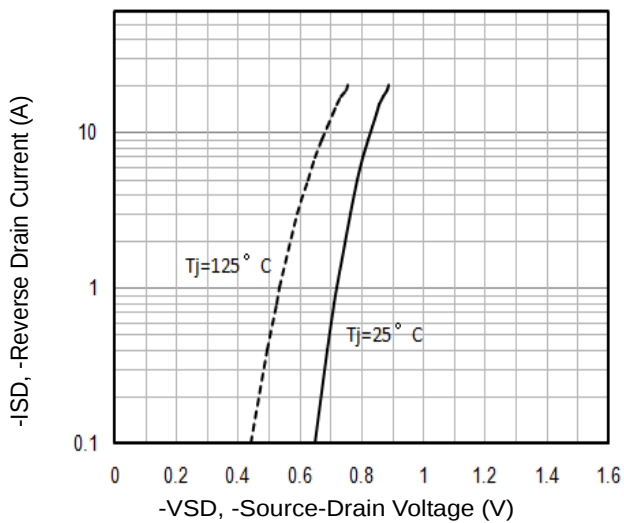


Fig5. Typical Source-Drain Diode Forward Voltage

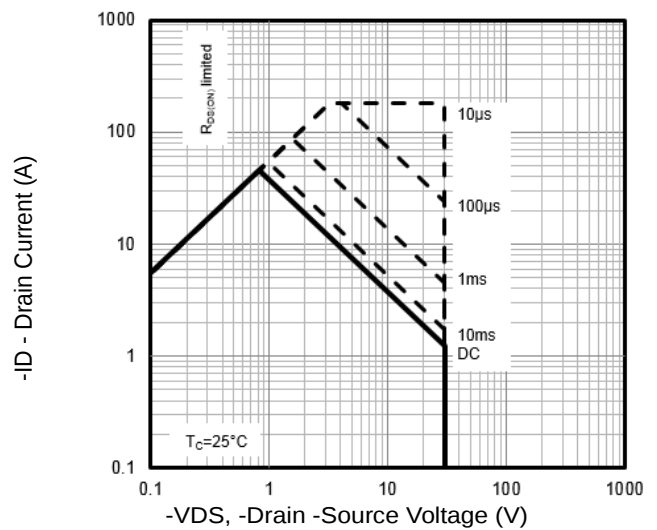


Fig6. Maximum Safe Operating Area

•P Typical Characteristics

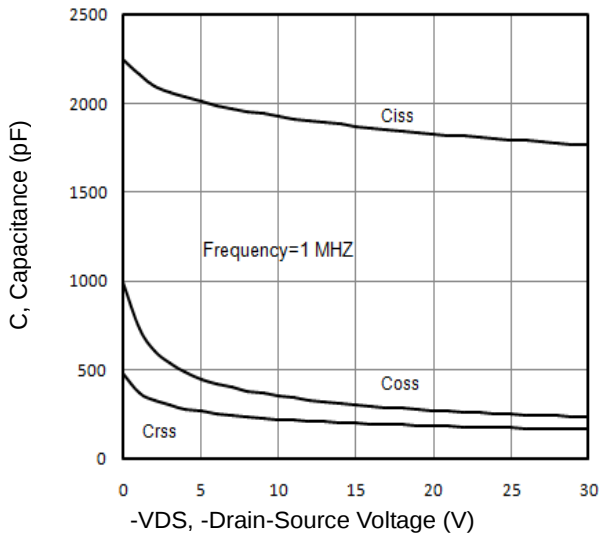


Fig7. Typical Capacitance Vs. Drain-Source Voltage

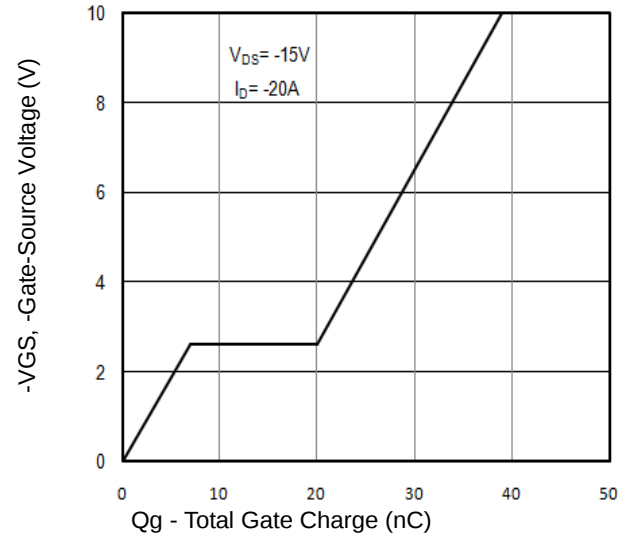


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

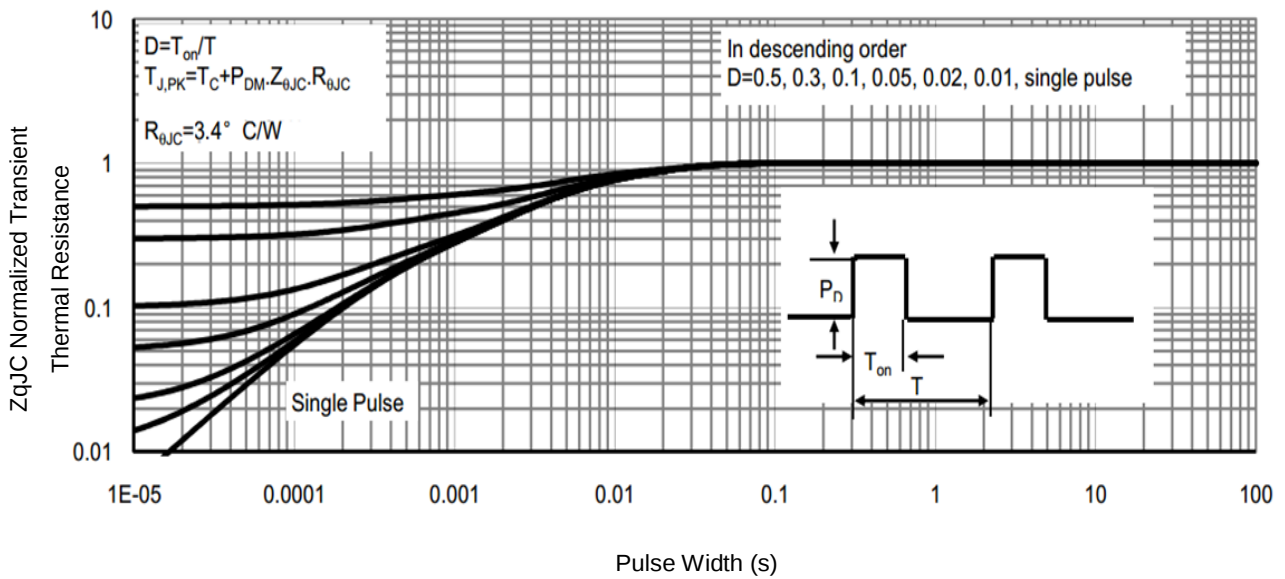


Fig9. Normalized Maximum Transient Thermal Impedance

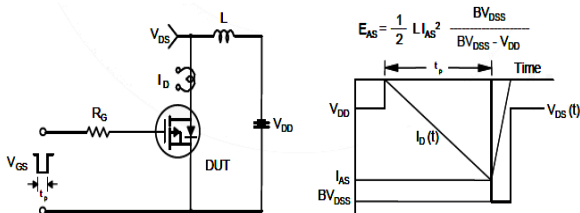


Fig10. Unclamped Inductive Test Circuit and Waveforms

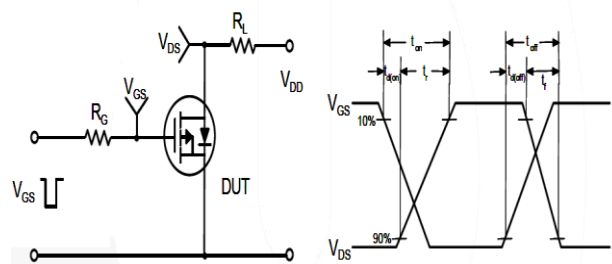


Fig11. Switching Time Test Circuit and waveforms

•Test Circuit

Fig.1 Switching Time Measurement Circuit

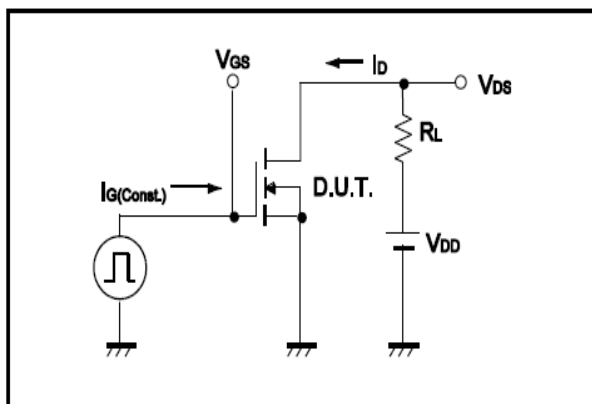


Fig.2 Gate Charge Waveform

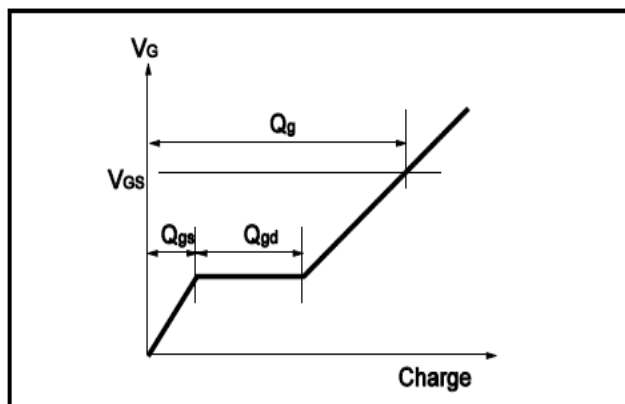


Fig.3 Switching Time Measurement Circuit

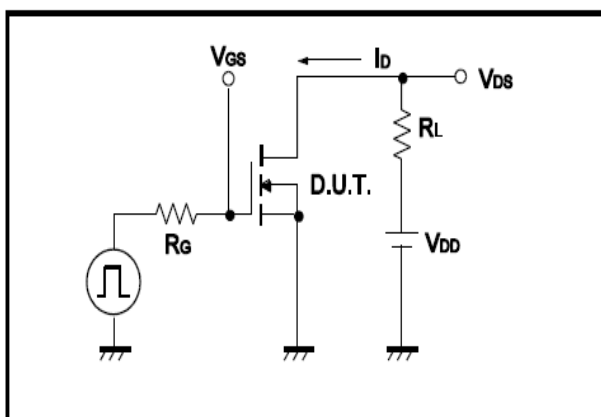


Fig.4 Gate Charge Waveform

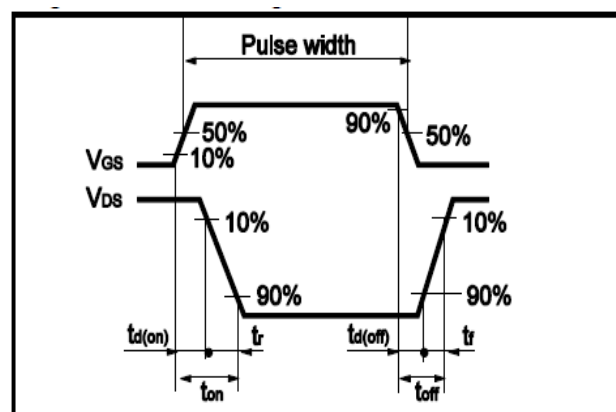


Fig.5 Avalanhe Measurement Circuit

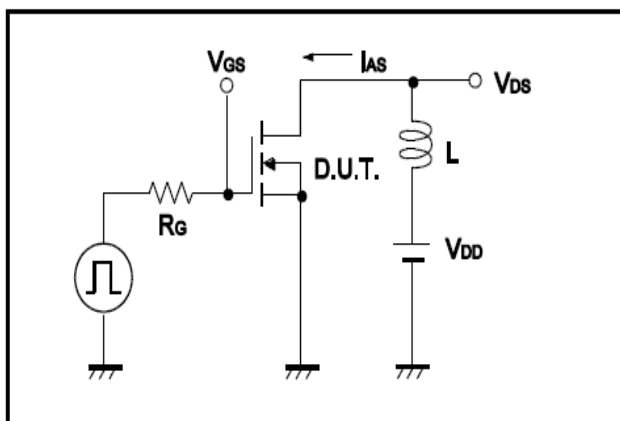
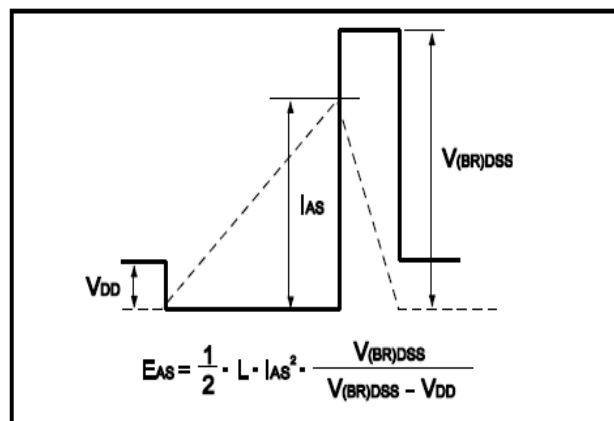


Fig.6 Avalanhe Waveform



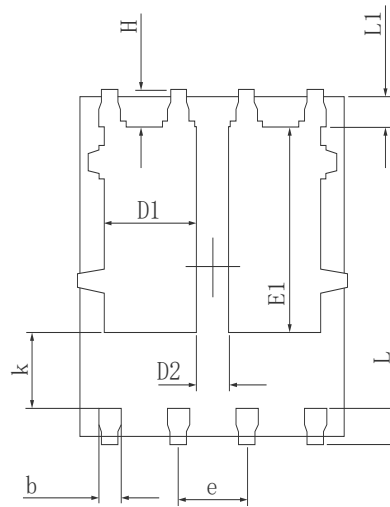
Technical drawing of a rectangular plate with a central hole. The drawing includes two views: a top view and a side view.

Top View:

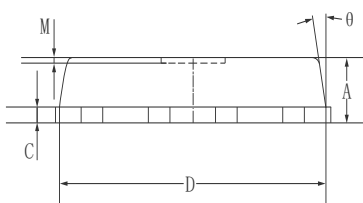
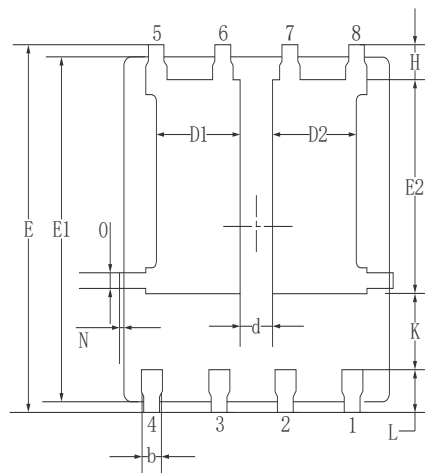
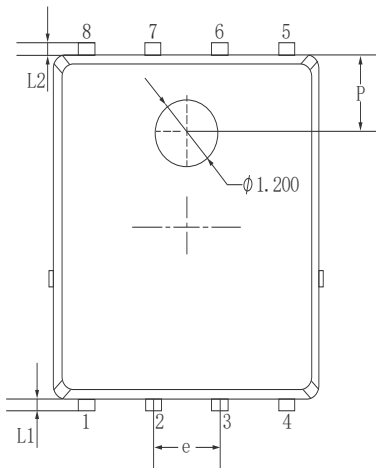
- The overall width is labeled $D3$.
- The overall height is labeled E .
- The inner rectangular area has a width labeled D and a height labeled $E2$.
- A central circular hole has a diameter labeled $\varnothing$.
- The distance from the center of the hole to the right edge of the inner rectangle is labeled $L2$.
- There are four small rectangular features (possibly mounting holes or slots) located at the corners of the inner rectangle.

Side View:

- The overall height is labeled A .
- The height of the main body is labeled $A1$.
- The thickness of the plate is labeled $A2$.
- The distance from the top surface to the center of the hole is labeled d .
- The angle of the top surface relative to the horizontal is labeled θ .
- The side view shows the profile of the plate, including the central hole and the four corner features.



SYMBOL	MILLIMETER		
	MIN	Typ.	MAX
A	0.900	1.000	1.100
A1	0.254 REF.		
A2	0~0.05		
D	4.824	4.900	4.976
D1	1.605	1.705	1.805
D2	0.500	0.600	0.700
D3	4.924	5.000	5.076
E	5.924	6.000	6.076
E1	3.375	3.475	3.575
E2	5.674	5.750	5.826
b	0.350	0.400	0.450
e	1.270 TYP.		
L	0.534	0.610	0.686
L1	0.424	0.500	0.576
L2	1.800 REF.		
k	1.190	1.290	1.390
H	0.549	0.625	0.701
θ	8°	10°	12°
Φ	1.100	1.200	1.300
d			0.100

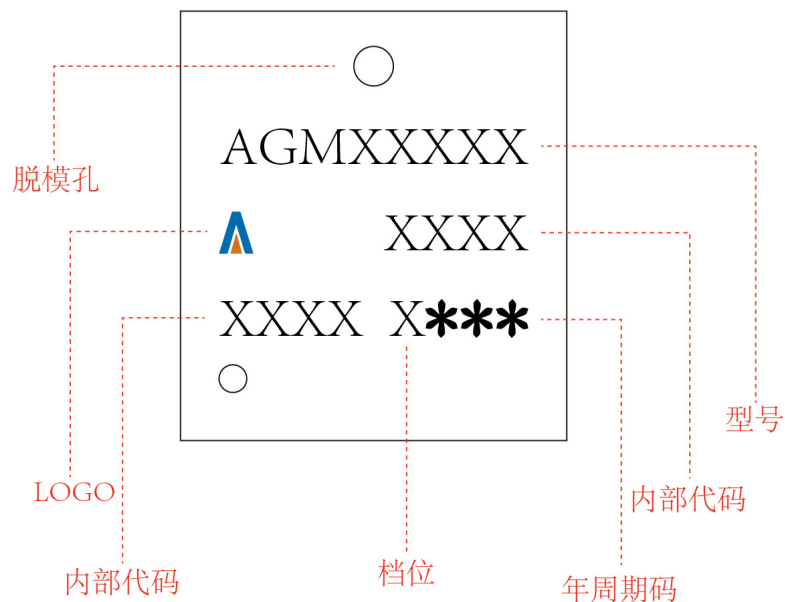


Symbol	Millimeters		
	MIN.	NOM.	MAX.
A	0.90	1.05	1.20
b	0.35	0.40	0.50
C	0.20	0.25	0.35
D	4.90	5.05	5.20
D1/D2	1.51	1.61	1.71
d	0.50	0.60	0.70
E	6.00	6.15	6.30
E1	5.60	5.75	5.90
E2	3.47	3.57	3.67
e	1.27 BSC.		
H	0.48	0.58	0.68
K	1.17	1.27	1.37
L	0.64	0.74	0.84
L1/L2	0.20 REF.		
θ	8°	10°	12°
M	0.08 REF.		
N	0	—	0.15
O	0.25 REF.		
P	1.28 REF.		

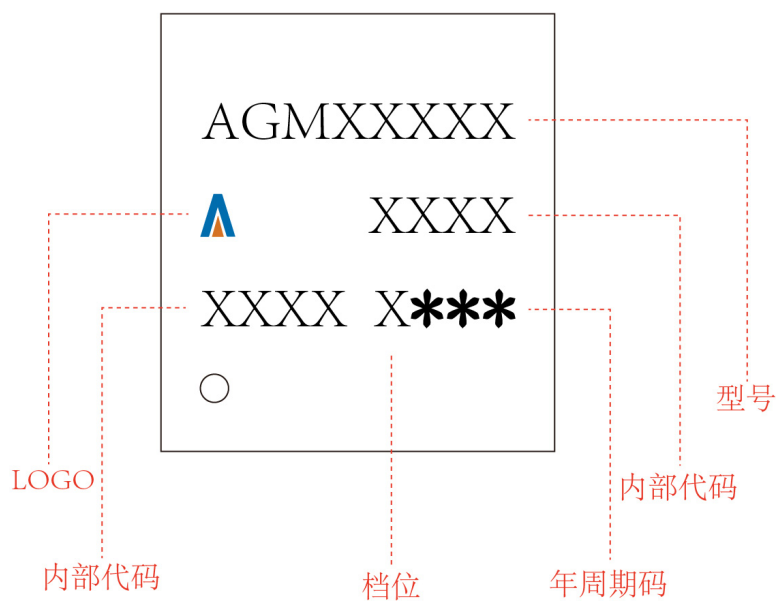
PDFN5*6

Marking Instructions:

Model1:



Model2:



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