Rochester Electronics

Datasheet

PART NUMBER

MD2114AL-3B-ROC

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

M2114A
1024 X 4 BIT STATIC RAM

MILITARY

	M2114AL-3	M2114AL-4	M2114A-4	M2114A-5
Max. Access Time (ns)	150	200	200	250
Max. Current (mA)	50	50	70	70

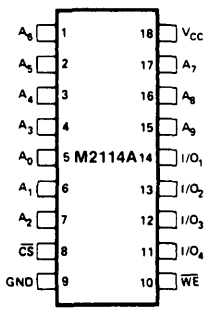
- **HMOS Technology**
- **Low Power, High Speed**
- **Identical Cycle and Access Times**
- **Single +5V Supply ±10%**
- **High Density 18 Pin Package**
- **Completely Static Memory - No Clock or Timing Strobe Required**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**
- **M2114 Upgrade**
- **Military Temperature Range -55°C to +125°C**

The Intel® M2114A is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using HMOS a high performance MOS technology It uses fully DC stable (static) circuitry throughout in both the array and the decoding therefore it requires no clocks or refreshing to operate Data access is particularly simple since address setup times are not required The data is read out nondestructively and has the same polarity as the input data Common input/output pins are provided

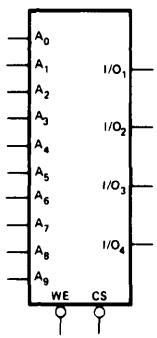
The M2114A is designed for memory applications where the high performance and high reliability of HMOS low cost large bit storage and simple interfacing are important design objectives The M2114A is placed in an 18-pin package for the highest possible density

It is directly TTL compatible in all respects inputs outputs and a single +5V supply A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are or-tied

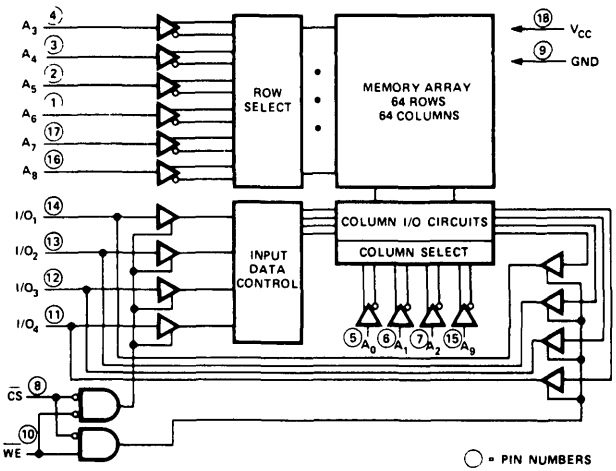
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_9	ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND GROUND
$\overline{CS}$	CHIP SELECT	
I/O_1–I/O_4	DATA INPUT/OUTPUT	

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-65°C to 135°C
Storage Temperature	-65°C to 150°C
Voltage on any Pin With Respect to Ground	-3 5V to +7V
Power Dissipation	1 0W
D C Output Current	5mA

*COMMENT Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability

D.C. AND OPERATING CHARACTERISTICS

T_A = -55°C to +125°C V_{CC} = 5V ±10% unless otherwise noted

SYMBOL	PARAMETER	M2114AL-3/L-4 Min	Typ [1]	Max	M2114A-4/-5 Min	Typ [1]	Max	UNIT	CONDITIONS
I_{LI}	Input Load Current (All Input Pins)			10			10	μA	V_{IN} = 0 to 5 5V
$\|I_{LO}\|$	I/O Leakage Current			10			10	μA	$\overline{CS}$ = V_{IH} $V_{I/O}$ – GND to V_{CC}
I_{CC}	Power Supply Current		25	50		50	70	mA	V_{CC} = max $I_{I/O}$ = 0 mA T_A = -55°C
V_{IL}	Input Low Voltage	-3 0		0 8	-3 0		0 8	V	
V_{IH}	Input High Voltage	2 0		6 0	2 0		6 0	V	
I_{OL}	Output Low Current	2 1	9 0		2 1	9 0		mA	V_{OL} = 0 4V
I_{OH}	Output High Current	-1 0	-2 5		-1 0	-2 5		mA	V_{OH} = 2 4V
I_{OS}[2]	Output Short Circuit Current			40			40	mA	V_{OUT} = GND

NOTE 1 Typical values are for T_A = 25°C and V_{CC} 5 0V
2 Duration not to exceed 30 seconds

CAPACITANCE

T_A = 25°C f = 1 0 MHz

SYMBOL	TEST	MAX	UNIT	CONDITIONS
$C_{I/O}$	Input/Output Capacitance	5	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0V

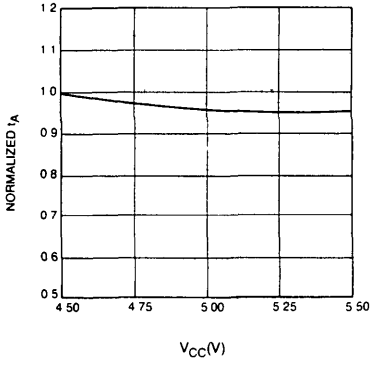
NOTE This parameter is periodically sampled and not 100% tested

A.C. CONDITIONS OF TEST

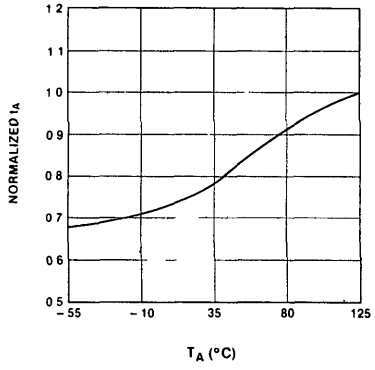
Input Pulse Levels	0 8 Volt to 2 0 Volt
Input Rise and Fall Times	10 nsec
Input and Output Timing Levels	1 5 Volts
Output Load	1 TTL Gate and C_L = 100 pF

TYPICAL D.C. AND A.C. CHARACTERISTICS

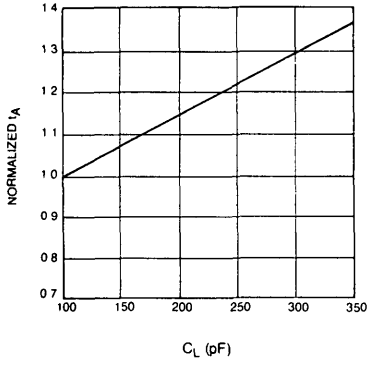
NORMALIZED ACCESS TIME VS SUPPLY VOLTAGE



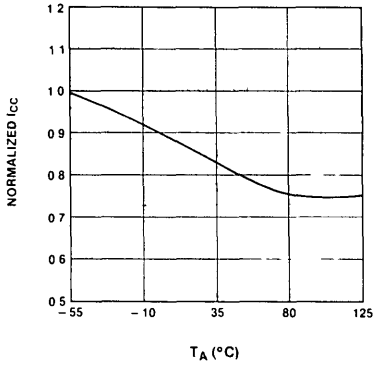
NORMALIZED ACCESS TIME VS AMBIENT TEMPERATURE



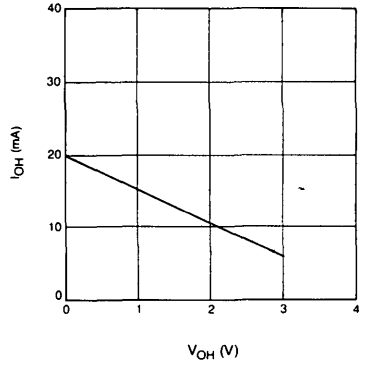
NORMALIZED ACCESS TIME VS OUTPUT LOAD CAPACITANCE



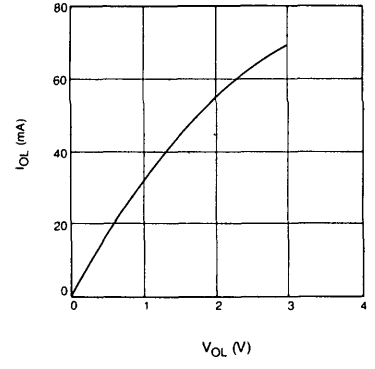
NORMALIZED POWER SUPPLY CURRENT VS AMBIENT TEMPERATURE



OUTPUT SOURCE CURRENT VS OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS OUTPUT VOLTAGE



A.C. CHARACTERISTICS T_A = -55°C to +125°C, V_{CC} = 5V ±10%, unless otherwise noted

READ CYCLE [1]

SYMBOL	PARAMETER	M2114AL-3 Min.	M2114AL-3 Max.	M2114A-4/L-4 Min.	M2114A-4/L-4 Max.	M2114A-5 Min.	M2114A-5 Max.	UNIT
t_{RC}	Read Cycle Time	150		200		250		ns
t_A	Access Time		150		200		250	ns
t_{CO}	Chip Selection to Output Valid		70		70		85	ns
t_{CX}	Chip Selection to Output Active	10		10		10		ns
t_{OTD}	Output 3-state from Deselection		40		50		60	ns
t_{OHA}	Output Hold from Address Change	15		15		15		ns

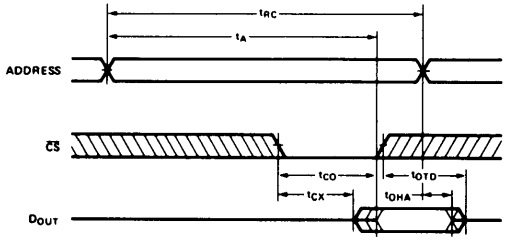
WRITE CYCLE [2]

SYMBOL	PARAMETER	M2114AL-3 Min.	M2114AL-3 Max.	M2114A-4/L-4 Min.	M2114A-4/L-4 Max.	M2114A-5 Min.	M2114A-5 Max.	UNIT
t_{WC}	Write Cycle Time	150		200		250		ns
t_W	Write Time	90		120		135		ns
t_{WR}	Write Release Time	0		0		0		ns
t_{OTW}	Output 3-state from Write		40		50		60	ns
t_{DW}	Data to Write Time Overlap	90		120		135		ns
t_{DH}	Data Hold from Write Time	0		0		0		ns

NOTES
1 A Read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2 A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high

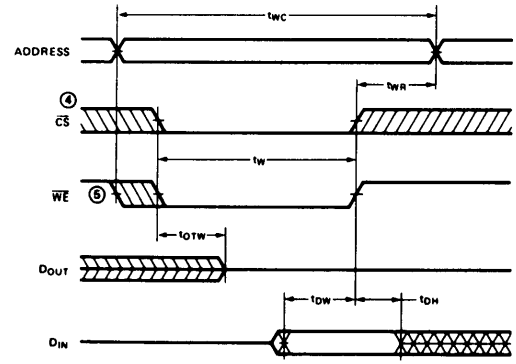
WAVEFORMS

READ CYCLE ③



NOTES
3 $\overline{WE}$ is high for a Read Cycle
4 If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition, the output buffers remain in a high impedance state
5 $\overline{WE}$ must be high during all address transitions

WRITE CYCLE

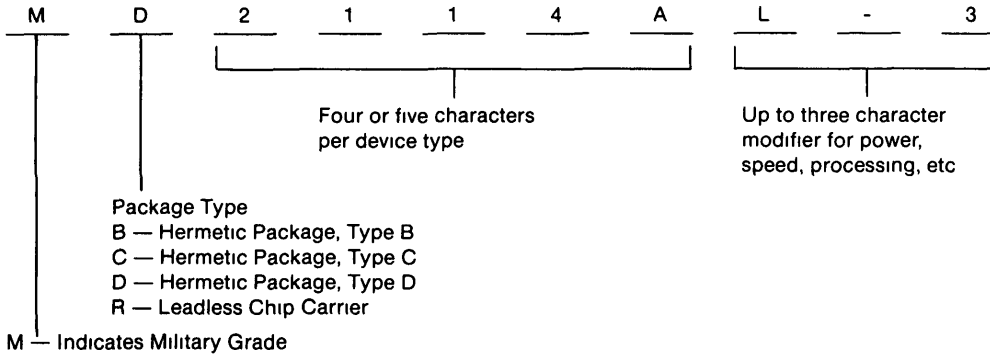


ORDERING INFORMATION

Status Notices
PRELIMINARY—Indicates some electrical parameters are subject to change
ADVANCE INFORMATION—Indicates some functional characteristics are subject to change

Semiconductor components are identified as follows

Example



For Military products, MIL-STD-883 Class B processing is indicated by a /B suffix, all others should be specified by the "s" number suffix

Examples

MD2147H/B	4K x 1 Static RAM, hermetic package Type D, military temperature range, MIL-STD-883 Class B processing
MD8080A/B	8080A microprocessor, hermetic package Type D, military temperature range, MIL-STD-883 Class B processing

The latest Intel OEM price book should be consulted for availability of various options These may be obtained from your local Intel representative or by writing directly to Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051