e.MMC Memory

MTFC32GBCAQTC-IT, MTFC64GBCAQTC-IT, MTFC128GBCAQTC-IT, MTFC256GBCAQTC-IT, MTFC32GBCAQTC-WT, MTFC64GBCAQTC-WT, MTFC128GBCAQTC-WT, MTFC256GBCAQTC-WT

Features

- MultiMediaCard (MMC) controller and NAND flash
- JEDEC/MMC standard version 5.1-compliant (JEDEC Standard No. JESD84-B51)[1]
- V_{CC}: 2.7–3.6V
- V_{CCQ}: 1.70–1.95V; 2.7-3.6V
- Storage temperature range:
  - IT: From –40°C to +95°C
- Advanced 12-signal interface
- ×1, ×4, and ×8 I/Os, selectable by host
- e.MMC I/F boot frequency: 0 to 52 MHz
- e.MMC I/F clock frequency: 0 to 200 MHz
- HS200/HS400 mode
- Command classes: Class 0 (basic); Class 2 (block read); Class 4 (block write); Class 5 (erase); Class 6 (write protection); Class 7 (lock card)
- Command queue
- BKOPS control
- Auto initiated refresh
- Host initiated refresh
- Packed commands
- Temporary write protection
- Boot operation (high-speed boot)
- Sleep mode
- Replay-protected memory block (RPMB)
- Hardware reset signal
- Multiple partitions with enhanced attribute
- Multiple partitions with ultra endurance attribute
- Permanent and power-on write protection
- High-priority interrupt (HPI)
- Data strobe pin
- Field firmware update (FFU)
- Device health report
- Sleep notification
- Background operation
- Production state awareness
- Reliable write
- Discard and sanitize
- Power-off notification
- Backward compatible with previous MMC
- ECC and block management implemented
- Enhanced strobe
- Extended reflow capability
- Retention:
  - 1 year @ 55°C at maximum PE
  - 2 years @ 55°C at 10% of maximum PE

Options	Marking
• Density	
– 32GB	32G
– 64GB	64G
– 128GB	128G
– 256GB	256G
• NAND component	
– 512Gb	BC
• Controller	AQ
• Packages – JEDEC-standard, RoHS-compliant	
– 153-ball LFBGA	TC
• Operating temperature range[2]	
– From –40°C to +95°C	IT
– From –25°C to +85°C	WT

Notes: 1. The JEDEC specification is available at www.jedec.org/sites/default/files/docs/JESD84-B51.pdf.
2. Operating temperature (T_{OPER}) is the case surface temperature on the center/top of the package.

Part Numbering Information

Micron® e.MMC memory devices are available in different configurations and densities.

Figure 1: e.MMC Part Numbering

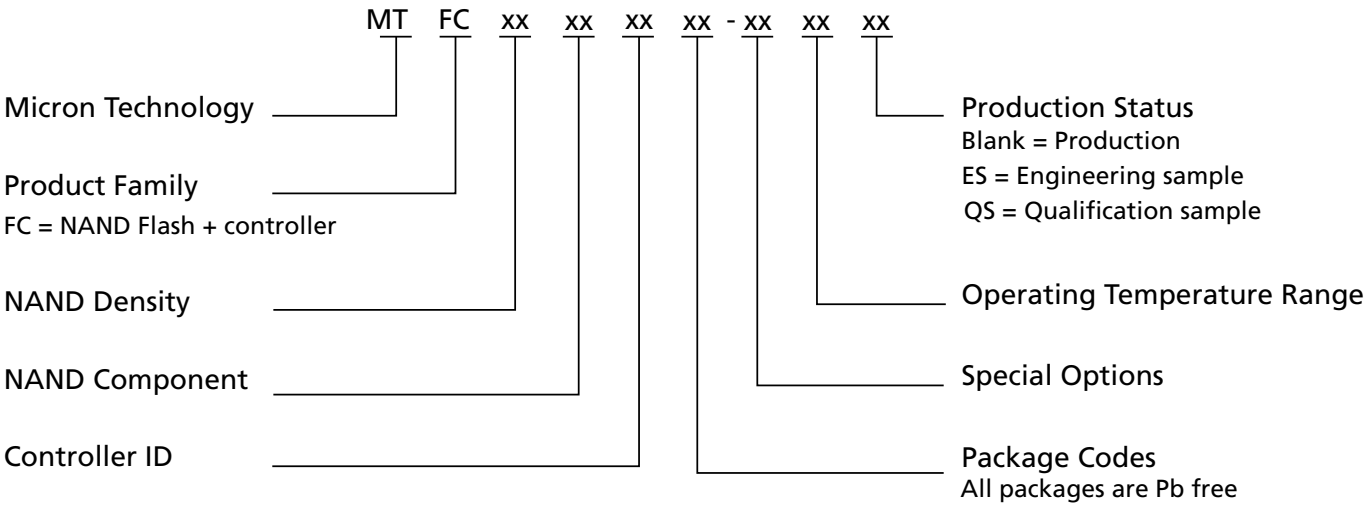

Table 1: Ordering Information

Base Part Number	Density	Package
MTFC32GBCAQTC-IT	32GB	153-ball LFBGA 11.5mm × 13mm × 1.3mm
MTFC32GBCAQTC-WT		
MTFC64GBCAQTC-IT	64GB	
MTFC64GBCAQTC-WT		
MTFC128GBCAQTC-IT	128GB	
MTFC128GBCAQTC-WT		
MTFC256GBCAQTC-IT	256GB	
MTFC256GBCAQTC-WT		

Device Marking

Due to the size of the package, the Micron-standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a 5-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at the FBGA Part Marking Decoder site: www.micron.com/decoder.

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Performance and Consumption

e.MMC Performance

Burst performances in the following tables are retrieved with these conditions: Bus in x8 I/O; Temperature 25°C; Sequential access of 512KB chunk; Cache on (write); Command queueing enabled with queue depth 32 commands.

Additional performance data, such as sustained and system performance on a specific application board, is provided in a separate document upon customer request.

Table 2: HS400 Performance

Condition	Typical Values				Unit
	32GB	64GB	128GB	256GB	
Sequential write	185	185	235	260	MB/s
Sequential read	335	335	335	335	MB/s

Table 3: HS200 Performance

Condition	Typical Values				Unit
	32GB	64GB	128GB	256GB	
Sequential write	130	130	150	155	MB/s
Sequential read	180	180	180	180	MB/s

e.MMC Current Consumption

Current consumption in the following tables are retrieved with these conditions: Bus in x8 I/O; V_{CC} = 3.6V and V_{CCQ} = 1.8V; Temperature 25°C; Measurements done as average RMS current consumption; I_{CCQ} in READ operation measurements with tester load disconnected.

Table 4: HS400 Current Consumption

Condition	Typical Values (I_{CC}/I_{CCQ})				Unit
	32GB	64GB	128GB	256GB	
Write[1]	37/102	37/102	45/102	44/103	mA
Read[1]	35/149	35/149	37/152	37/157	mA
Sleep (V_{CC} off)	0/730	0/730	0/664	0/759	µA
Auto standby	33/816	33/816	44/733	83/813	µA

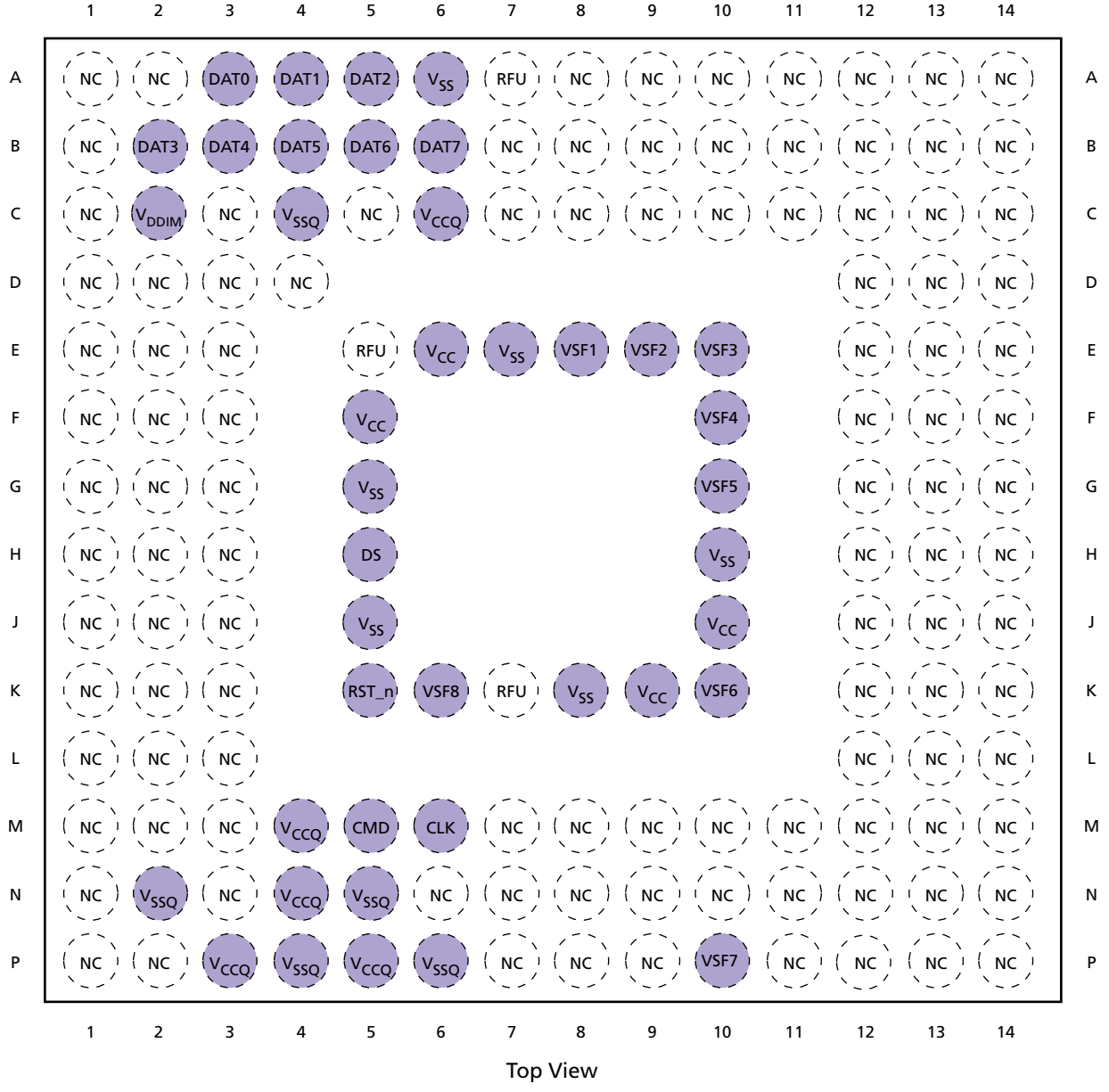
Note: 1. Command queueing enabled with queue depth 32 commands.

Table 5: HS200 Current Consumption

Condition	Typical Values (I_{CC}/I_{CCQ})				Unit
	32GB	64GB	128GB	256GB	
Write	34/97	34/97	38/96	37/97	mA
Read	25/119	25/119	26/119	26/123	mA
Sleep (V_{CC} off)	0/730	0/730	0/664	0/759	µA
Auto standby	33/816	33/816	44/733	83/813	µA

153-Ball Signal Assignments

Figure 2: 153 Ball (Top View, Ball Down)



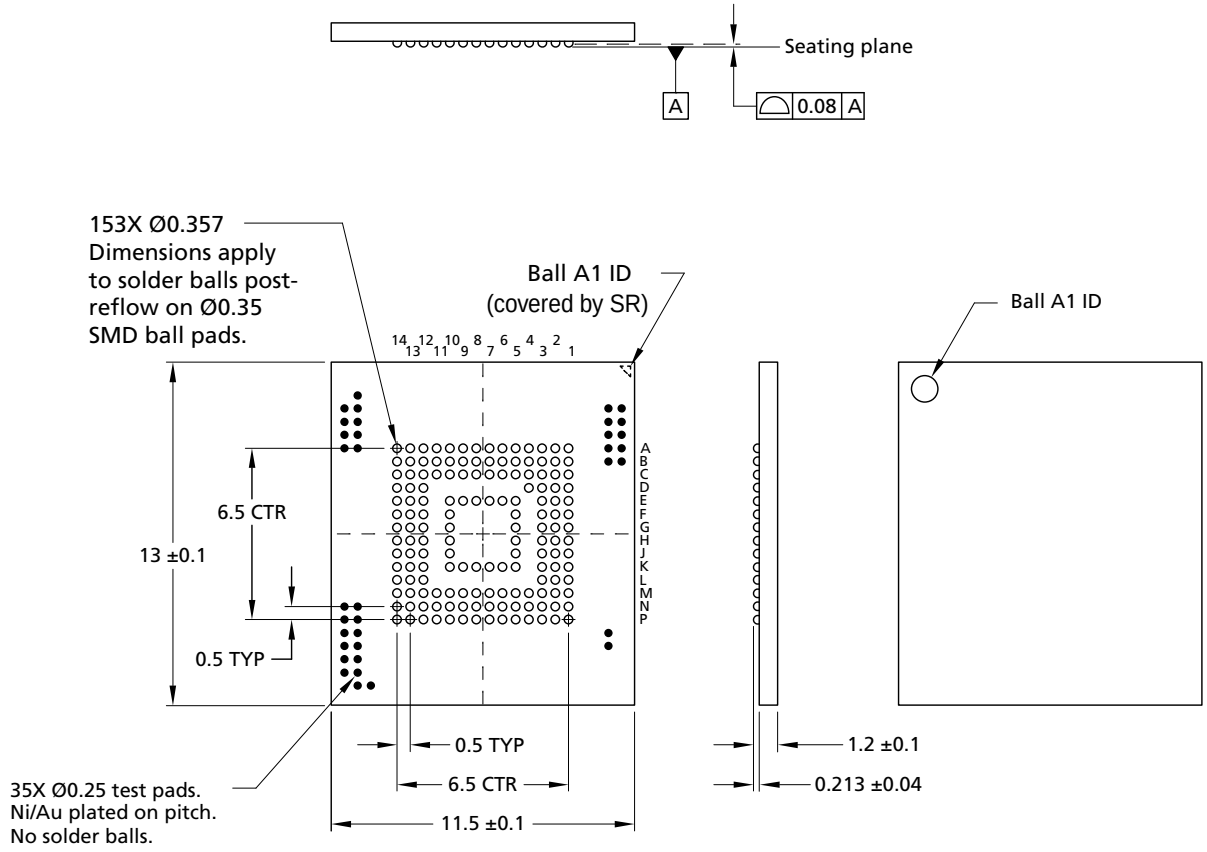
Top View

Notes: 1. Some previous versions of the JEDEC product or mechanical specification had defined reserved for future use (RFU) balls as no connect (NC) balls. NC balls assigned in the previous specifications could have been connected to ground on the system board. To enable new feature introduction, some of these balls are assigned as RFU in the v4.4 mechanical specification. Any new PCB footprint implementations should use the new ball assignments and leave the RFU balls floating on the system board.

2. V_{CC}, V_{CCQ}, V_{SS}, and V_{SSQ} balls must all be connected on the system board.

Package Dimensions

Figure 3: 153/196-Ball LFBGA – 11.5mm x 13.0mm x 1.3mm

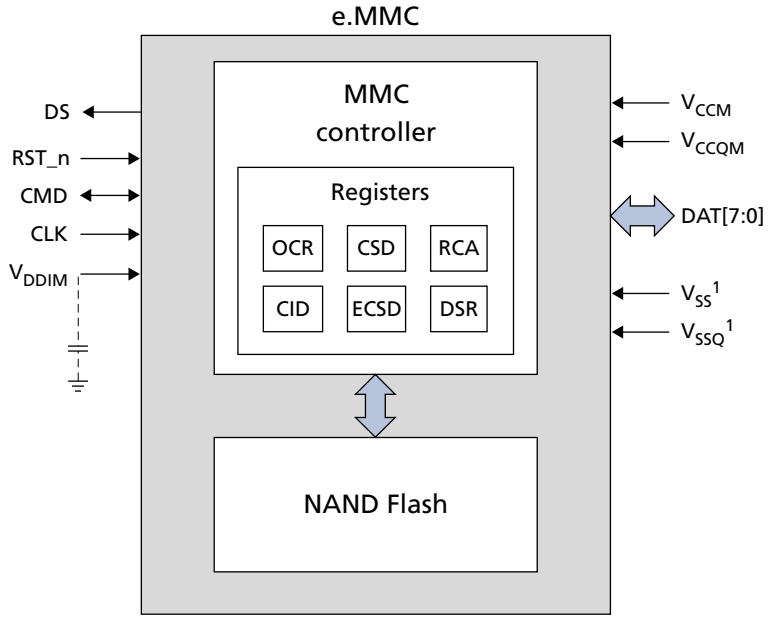


Notes: 1. Dimensions are in millimeters.
2. The package height does not include room temperature warpage.
3. In the whole eMMC package area, solder mask is recommended to cover the via pad in the PCB in order to avoid possible contact with Ni/Au plated test pads on the eMMC package. The Ni/Au plated test pads are reserved for Micron internal use only.
4. Solder ball composition: SACQ with CuOSP pads (Sn, 4.0%; Ag, 0.5%; Cu, 3%; Bi, 0.05% Ni).

Architecture

Block Diagram

Figure 4: e.MMC Functional Block Diagram



Note: 1. V_{SS} and V_{SSQ} are internally connected.

MMC Protocol Independent of NAND Flash Technology

The MMC specification defines the communication protocol between a host and a device. The protocol is independent of the NAND flash features included in the device. The device has an intelligent on-board controller that manages the MMC communication protocol.

The controller also handles block management functions such as logical block allocation and wear leveling. These management functions require complex algorithms and depend entirely on NAND flash technology (generation or memory cell type). The device handles these management functions internally, making them invisible to the host processor.

Defect and Error Management

Micron e.MMC incorporates advanced technology for defect and error management. If a defective block is identified, the device completely replaces it with a spare block. This process is invisible to the host and does not affect user-allocated data space.

The device also includes a built-in error correction code (ECC) algorithm to ensure data integrity is maintained. To best implement these advanced technologies and ensure proper data loading and storage over the life of the device, the host must follow these precautions:

- Check the status after WRITE, READ, and ERASE operations.
- Avoid power-down during WRITE and ERASE operations.

As best practice, Micron recommends the usage of Power Off Notification (PON) and refresh mechanism.

OCR Register

The 32-bit operation conditions register (OCR) stores the voltage profile of the card and the access mode indication. In addition, this register includes a status information bit.

Table 6: OCR Parameters

OCR Bits	OCR Value	Description
[31]	1b (ready)/0b (busy)[1]	Device power-on status bit
[30:29]	10b	Sector mode
[28:24]	0 0000b	Reserved
[23:15]	1 1111 1111b	2.7–3.6V voltage range
[14:8]	000 0000b	2.0–2.7V voltage range
[7]	1b	1.70–1.95V voltage range
[6:0]	000 0000b	Reserved

Note: 1. OCR = C0FF8080h after the device has completed power-up.

CID Register

The card identification (CID) register is 128 bits wide. It contains the device identification information used during the card identification phase as required by e.MMC protocol. Each device is created with a unique identification number.

Table 7: CID Register Field Parameters

Name	Field	Width	CID Bits	CID Value
Manufacturer ID	MID	8	[127:120]	13h
Reserved	–	6	[119:114]	–
Card/BGA	CBX	2	[113:112]	01h
OEM/application ID	OID	8	[111:104]	–
Product name	PNM	48	[103:56]	32GB WT: 30574D323045h (0WM20E)
				32GB IT: 30494D323045h (0IM20E)
				64GB WT: 30574D323046h (0WM20F)
				64GB IT: 30494D323046h (0IM20F)
				128GB WT: 30574D323047h (0WM20G)
				128GB IT: 30494D323047h (0IM20G)
				256GB WT: 30574D323048h (0WM20H)
				256GB IT: 30494D323048h (0IM20H)
Product revision	PRV	8	[55:48]	–
Product serial number	PSN	32	[47:16]	–
Manufacturing date	MDT	8	[15:8]	–
CRC7 checksum	CRC	7	[7:1]	–
Not used; Always 1	–	1	[0]	–

CSD Register

The card-specific data (CSD) register provides information about accessing the device contents. The CSD register defines the data format, error correction type, maximum data access time, and data transfer speed, as well as whether the DS register can be used. The programmable part of the register (entries marked with W or E in the following table) can be changed by the PROGRAM_CSD (CMD27) command.

Table 8: CSD Register Field Parameters

Note 1 applies to entire table.

Name	Field	Density	Size (Bits)	Cell Type	CSD (Bits)	CSD Value	Notes
CSD structure	CSD_STRUCTURE	–	2	R	[127:126]	3h	–
System specification version	SPEC_VERS	–	4	R	[125:122]	4h	–
Reserved	–	–	2	R	[121:120]	–	2
Data read access time 1	TAAC	–	8	R	[119:112]	7Fh	3
Data read access time 2 in CLK cycles (NSAC × 100)	NSAC	–	8	R	[111:104]	01h	3
Maximum bus clock frequency	TRAN_SPEED	–	8	R	[103:96]	32h	–
Card command classes	CCC	–	12	R	[95:84]	8F5h	–
Maximum read data block length	READ_BL_LEN	–	4	R	[83:80]	09h	–
Partial blocks for reads supported	READ_BL_PARTIAL	–	1	R	[79]	0h	–
Write block misalignment	WRITE_BLK_MISALIGN	–	1	R	[78]	0h	–
Read block misalignment	READ_BLK_MISALIGN	–	1	R	[77]	0h	–
DSR implemented	DSR_IMP	–	1	R	[76]	1h	–
Reserved	–	–	2	R	[75:74]	–	2
Device size	C_SIZE	–	12	R	[73:62]	FFFh	–
Maximum read current at $V_{DD,min}$	VDD_R_CURR_MIN	–	3	R	[61:59]	7h	–
Maximum read current at $V_{DD,max}$	VDD_R_CURR_MAX	–	3	R	[58:56]	7h	–
Maximum write current at $V_{DD,min}$	VDD_W_CURR_MIN	–	3	R	[55:53]	7h	–
Maximum write current at $V_{DD,max}$	VDD_W_CURR_MAX	–	3	R	[52:50]	7h	–
Device size multiplier	C_SIZE_MULT	–	3	R	[49:47]	7h	–
Erase group size	ERASE_GRP_SIZE	–	5	R	[46:42]	1Fh	–
Erase group size multiplier	ERASE_GRP_MULT	–	5	R	[41:37]	1Fh	–

Table 8: CSD Register Field Parameters (Continued)

Name	Field	Density	Size (Bits)	Cell Type	CSD (Bits)	CSD Value	Notes
Write protect group size	WP_GRP_SIZE	–	5	R	[36:32]	0Fh	–
Write protect group enable	WP_GRP_ENABLE	–	1	R	[31]	1h	–
Manufacturer default ECC	DEFAULT_ECC	–	2	R	[30:29]	0h	–
Write-speed factor	R2W_FACTOR	–	3	R	[28:26]	03h	3
Maximum write data block length	WRITE_BL_LEN	–	4	R	[25:22]	09h	–
Partial blocks for writes supported	WRITE_BL_PARTIAL	–	1	R	[21]	0h	–
Reserved	–	–	4	R	[20:17]	–	–
Content protection application	CONTENT_PROT_APP	–	1	R	[16]	0h	–
File-format group	FILE_FORMAT_GRP	–	1	R/W	[15]	0h	–
Copy flag (OTP)	COPY	–	1	R/W	[14]	0h	
Permanent write protection	PERM_WRITE_PROTECT	–	1	R/W	[13]	0h	
Temporary write protection	TMP_WRITE_PROTECT	–	1	R/W/E	[12]	0h	
File format	FILE_FORMAT	–	2	R/W	[11:10]	0h	
ECC	ECC	–	2	R/W/E	[9:8]	0h	
CRC	CRC	–	7	R/W/E	[7:1]	–	
Not used: always 1	–	–	1	–	[0]	–	

Notes: 1. R = Read-only;
R/W = One-time programmable and readable;
R/W/E = Multiple writable with value kept after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable
2. Reserved bits should be read as 0.
3. Host should calculate the write time-out conditions as per JEDEC specification, using CSD register values TAAC, NSAC, and R2W_FACTOR, or higher. Lower time out values may result in application hang, loop forced reset, or re-boot. Additional information is provided in a separate document upon customer request.

ECSD Register

The 512-byte extended card-specific data (ECSD) register defines device properties and selected modes. The most significant 320 bytes are the properties segment. This segment defines device capabilities and cannot be modified by the host. The lower 192 bytes are the modes segment. The modes segment defines the configuration in which the device is working. The host can change the properties of modes segments using the SWITCH command.

Table 9: ECSD Register Field Parameters

Note 1 applies to entire table.

Name	Field	Density	Size (Bytes)	Cell Type	ECSD Bytes	ECSD Values	Notes
Properties Segment							–
Reserved	–		6	TBD	[511:506]	–	2
Extended security error support	EXT_SECURITY_ERR		1	R	[505]	00h	–
Supported command sets	S_CMD_SET		1	R	[504]	01h	–
HPI features	HPI_FEATURES		1	R	[503]	01h	–
Background operations support	BKOPS_SUPPORT		1	R	[502]	01h	–
Max-packed READ commands	MAX_PACKED_READS		1	R	[501]	3Ch	–
Max-packed WRITE commands	MAX_PACKED_WRITES		1	R	[500]	20h	–
Data tag support	DATA_TAG_SUPPORT		1	R	[499]	01h	–
Tag unit size	TAG_UNIT_SIZE		1	R	[498]	03h	–
Tag resources size	TAG_RES_SIZE		1	R	[497]	00h	–
Context management capabilities	CONTEXT_CAPABILITIES		1	R	[496]	05h	–
Large unit size	LARGE_UNIT_SIZE_M1		1	R	[495]	18h	–
Extended partitions attribute support	EXT_SUPPORT		1	R	[494]	03h	–
Supported modes	SUPPORTED_MODES		1	R	[493]	03h	–
Field firmware update features	FFU_FEATURES		1	R	[492]	00h	–
Operation code timeout	OPERATION_CODE_TIMEOUT		1	R	[491]	00h	–
Field firmware update arguments	FFU_ARG		4	R	[490:487]	0000FFFFh	–
Barrier support	BARRIER_SUPPORT		1	R	[486]	01h	–
Reserved	–		177	TBD	[485:309]	–	2
CMD queuing support	CMDQ_SUPPORT		1	R	[308]	1Fh	–
CMD queuing depth	CMDQ_DEPTH		1	R	[307]	–	–
Reserved	–		1	TBD	[306]	–	2

Table 9: ECSD Register Field Parameters (Continued)

Name	Field	Density	Size (Bytes)	Cell Type	ECSD Bytes	ECSD Values	Notes
Number of firmware sectors correctly programmed	NUMBER_OF_FW_SECTORS_ CORRECTLY_PROGRAMMED		4	R	[305:302]	00h	–
Vendor proprietary health report	VENDOR_PROPRIETARY_ HEALTH_REPORT		32	R	[301:270]	00h	–
Device life time estimate type B[6]	DEVICE_LIFE_TIME_EST_TYP_B		1	R	[269]	01h	–
Device life time estimate type A[6]	DEVICE_LIFE_TIME_EST_TYP_A		1	R	[268]	01h	–
Pre-end of life information[6]	PRE_EOL_INFO		1	R	[267]	01h	–
Optimal read size	OPTIMAL_READ_SIZE		1	R	[266]	01h	–
Optimal write size	OPTIMAL_WRITE_SIZE		1	R	[265]	01h	–
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE		1	R	[264]	01h	–
Device version	DEVICE_VERSION		2	R	[263:262]	0000h	–
Firmware version	FIRMWARE_VERSION		8	R	[261:254]	–	–
Power class for 200 MHz DDR at V_{CC} = 3.6V	PWR_CL_DDR_200_360		1	R	[253]	00h	–
Cache size	CACHE_SIZE	32GB 64GB 128GB 256GB	4	R	[252:249]	00000C00h	–
Generic CMD6 timeout	GENERIC_CMD6_TIME		1	R	[248]	0Ah	–
Power-off notification (long) timeout	POWER_OFF_LONG_TIME		1	R	[247]	32h	–
Background operations status	BKOPS_STATUS		1	R	[246]	00h	–
Number of correctly programmed sectors	CORRECTLY_PROG_ SECTORS_NUM		4	R	[245:242]	00000000h	–
First initialization time after partitioning (first CMD1 to device ready)	INI_TIMEOUT_AP		1	R	[241]	1Eh	–
Cache flushing policy	CACHE_FLUSH_POLICY		1	R	[240]	01h	–
Power class for 52 MHz, DDR at 3.6V	PWR_CL_DDR_52_360		1	R	[239]	00h	–
Power class for 52 MHz, DDR at 1.95V	PWR_CL_DDR_52_195		1	R	[238]	00h	–

Table 9: ECSD Register Field Parameters (Continued)

Name	Field	Density	Size (Bytes)	Cell Type	ECSD Bytes	ECSD Values	Notes
Power class for 200 MHz at 1.95V	PWR_CL_200_195		1	R	[237]	00h	–
Power class for 200 MHz, at 1.3V	PWR_CL_200_130		1	R	[236]	00h	–
Minimum write performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_W_8_52		1	R	[235]	00h	–
Minimum read performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_R_8_52		1	R	[234]	00h	–
Reserved	–		1	TBD	[233]	–	2
TRIM multiplier	TRIM_MULT		1	R	[232]	07h	–
Secure feature support	SEC_FEATURE_SUPPORT		1	R	[231]	51h	–
Secure erase multiplier	SEC_ERASE_MULT		1	R	[230]	07h	–
Secure trim multiplier	SEC_TRIM_MULT		1	R	[229]	07h	–
Boot information	BOOT_INFO		1	R	[228]	07h	–
Reserved	–		1	TBD	[227]	–	2
Boot partition size	BOOT_SIZE_MULT		1	R	[226]	FCh	3
Access size	ACC_SIZE		1	R	[225]	00h	–
High-capacity erase unit size	HC_ERASE_GRP_SIZE		1	R	[224]	01h	–
High-capacity erase timeout	ERASE_TIMEOUT_MULT		1	R	[223]	07h	–
Reliable write-sector count	REL_WR_SEC_C		1	R	[222]	01h	–
High-capacity write protect group size	HC_WP_GRP_SIZE	32GB 64GB 128GB 256GB	1	R	[221]	10h 20h 40h 80h	–
Sleep current (V_{CC})	S_C_VCC		1	R	[220]	00h	–
Sleep current (V_{CCQ})	S_C_VCCQ		1	R	[219]	00h	–
Production state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT		1	R	[218]	00h	–
Sleep/awake timeout	S_A_TIMEOUT		1	R	[217]	14h	–
Sleep notification timeout	SLEEP_NOTIFICATION_TIME		1	R	[216]	0Ch	–
Sector count	SEC_COUNT	32GB 64GB 128GB 256GB	4	R	[215:212]	03B48000h 07690000h 0ED20000h 1DA40000h	–

Table 9: ECSD Register Field Parameters (Continued)

Name	Field	Density	Size (Bytes)	Cell Type	ECSD Bytes	ECSD Values	Notes
Secure write protect information	SECURE_WP_INFO		1	R	[211]	01h	–
Minimum write performance for 8-bit at 52 MHz	MIN_PERF_W_8_52		1	R	[210]	00h	–
Minimum read performance for 8-bit at 52 MHz	MIN_PERF_R_8_52		1	R	[209]	00h	–
Minimum write performance for 8-bit at 26 MHz and 4-bit at 52 MHz	MIN_PERF_W_8_26_4_52		1	R	[208]	00h	–
Minimum read performance for 8-bit at 26 MHz and 4-bit at 52 MHz	MIN_PERF_R_8_26_4_52		1	R	[207]	00h	–
Minimum write performance for 4-bit at 26 MHz	MIN_PERF_W_4_26		1	R	[206]	00h	–
Minimum read performance for 4-bit at 26 MHz	MIN_PERF_R_4_26		1	R	[205]	00h	–
Reserved	–		1	TBD	[204]	–	2
Power class for 26 MHz at 3.6V	PWR_CL_26_360		1	R	[203]	00h	–
Power class for 52 MHz at 3.6V	PWR_CL_52_360		1	R	[202]	00h	–
Power class for 26 MHz at 1.95V	PWR_CL_26_195		1	R	[201]	00h	–
Power class for 52 MHz at 1.95V	PWR_CL_52_195		1	R	[200]	00h	–
Partition switching timing	PARTITION_SWITCH_TIME		1	R	[199]	06h	–
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME		1	R	[198]	0Ah	–
I/O driver strength	DRIVER_STRENGTH		1	R	[197]	1Fh	–
Device type	DEVICE_TYPE		1	R	[196]	57h	–
Reserved	–		1	TBD	[195]	–	2
CSD structure version	CSD_STRUCTURE		1	R	[194]	02h	–
Reserved	–		1	TBD	[193]	–	2
Extended CSD revision	EXT_CSD_REV		1	R	[192]	08h	–
Modes Segment							–
Command set	CMD_SET		1	R/W/E_P	[191]	00h	–
Reserved	–		1	TBD	[190]	–	2

Table 9: ECSD Register Field Parameters (Continued)

Name	Field	Density	Size (Bytes)	Cell Type	ECSD Bytes	ECSD Values	Notes
Command set revision	CMD_SET_REV		1	R	[189]	00h	–
Reserved	–		1	TBD	[188]	–	2
Power class	POWER_CLASS		1	R/W/E_P	[187]	00h	–
Reserved	–		1	TBD	[186]	–	2
High-speed interface timing	HS_TIMING		1	R/W/E_P	[185]	00h	–
Strobe support	STROBE_SUPPORT		1	R	[184]	01h	–
Bus width mode	BUS_WIDTH		1	W/E_P	[183]	00h	–
Reserved	–		1	TBD	[182]	–	2
Erased memory content	ERASED_MEM_CONT		1	R	[181]	00h	–
Reserved	–		1	TBD	[180]	–	–
Partition configuration	PARTITION_CONFIG		1	R/W/E, R/W/E_P	[179]	00h	–
Boot configuration protection	BOOT_CONFIG_PROT		1	R/W, R/W/C_P	[178]	00h	–
Boot bus conditions	BOOT_BUS_CONDITIONS		1	R/W/E	[177]	00h	–
Reserved	–		1	TBD	[176]	–	2
High-density erase group definition	ERASE_GROUP_DEF		1	R/W/E_P	[175]	00h	–
Boot write protection status registers	BOOT_WP_STATUS		1	R	[174]	00h	–
Boot area write protection register	BOOT_WP		1	R/W, R/W/C_P	[173]	00h	–
Reserved	–		1	TBD	[172]	–	–
User write protection register	USER_WP		1	R/W, R/W/C_P, R/W/E_P	[171]	00h	–
Reserved	–		1	TBD	[170]	–	2
Firmware configuration	FW_CONFIG		1	R/W	[169]	00h	–
RPMB size	RPMB_SIZE_MULT		1	R	[168]	20h	–
Write reliability setting register	WR_REL_SET		1	R/W	[167]	1Fh	4
Write reliability parameter register	WR_REL_PARAM		1	R	[166]	15h	–
SANITIZE START operation	SANITIZE_START		1	W/E_P	[165]	00h	–
Manually start background operations	BKOPS_START		1	W/E_P	[164]	00h	–

Table 9: ECSD Register Field Parameters (Continued)

Name	Field	Density	Size (Bytes)	Cell Type	ECSD Bytes	ECSD Values	Notes
Enable background operations handshake	BKOPS_EN		1	R/W, R/W/E	[163]	02h	–
Hardware reset function	RST_n_FUNCTION		1	R/W	[162]	00h	–
HPI management	HPI_MGMT		1	R/W/E_P	[161]	00h	–
Partitioning support	PARTITIONING_SUPPORT		1	R	[160]	07h	–
Maximum enhanced area size	MAX_ENH_SIZE_MULT	32GB 64GB 128GB 256GB	3	R	[159:157]	0004F0h 0004F0h 0004F0h 0004F0h	–
Partitions attribute	PARTITIONS_ATTRIBUTE		1	R/W	[156]	00h	–
Partitioning setting	PARTITION_SETTING_ COMPLETED		1	R/W	[155]	00h	–
General-purpose partition size	GP_SIZE_MULT		12	R/W	[154:143]	00h	–
Enhanced user data area size	ENH_SIZE_MULT		3	R/W	[142:140]	000000h	–
Enhanced user data start address	ENH_START_ADDR		4	R/W	[139:136]	00000000h	–
Reserved	–		1	TBD	[135]	–	–
Bad block management mode	SEC_BAD_BLK_MGMNT		1	R/W	[134]	00h	–
Production state awareness	PRODUCTION_ STATE_AWARENESS		1	R/W/E	[133]	00h	5
Package case temperature is controlled	TCASE_SUPPORT		1	W/E_P	[132]	00h	–
Periodic wake-up	PERIODIC_WAKEUP		1	R/W/E	[131]	00h	–
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_ DDR_SUPPORT		1	R	[130]	01h	–
Reserved	–		2	TBD	[129:128]	–	2
Vendor specific fields	VENDOR_SPECIFIC_FIELD		64	<vendor specific>	[127:64]	–	–
Native sector size	NATIVE_SECTOR_SIZE		1	R	[63]	00h	–
Sector size emulation	USE_NATIVE_SECTOR		1	R/W	[62]	00h	–
Sector size	DATA_SECTOR_SIZE		1	R	[61]	00h	–
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU		1	R	[60]	00h	–
Class 6 commands control	CLASS_6_CTRL		1	R/W/E_P	[59]	00h	–

Table 9: ECSD Register Field Parameters (Continued)

Name	Field	Density	Size (Bytes)	Cell Type	ECSD Bytes	ECSD Values	Notes
Number of addressed group to be released	DYNCAP_NEEDED		1	R	[58]	00h	–
Exception events control	EXCEPTION_EVENTS_CTRL		2	R/W/E_P	[57:56]	0000h	–
Exception events status	EXCEPTION_EVENTS_STATUS		2	R	[55:54]	0000h	–
Extended partitions attribute	EXT_PARTITIONS_ATTRIBUTE		2	R/W	[53:52]	0000h	–
Context configuration	CONTEXT_CONF		15	R/W/E_P	[51:37]	–	–
Packed command status	PACKED_COMMAND_STATUS		1	R	[36]	00h	–
Packed command failure index	PACKED_FAILURE_INDEX		1	R	[35]	00h	–
Power-off notification	POWER_OFF_NOTIFICATION		1	R/W/E_P	[34]	00h	–
Control to turn the cache on/off	CACHE_CTRL		1	R/W/E_P	[33]	00h	–
Flushing of the cache	FLUSH_CACHE		1	W/E_P	[32]	00h	–
Control to turn the barrier on/off	BARRIER_CTRL		1	R/W	[31]	00h	–
Mode configuration	MODE_CONFIG		1	R/W/E_P	[30]	00h	–
Mode operation codes	MODE_OPERATION_CODES		1	W/E_P	[29]	00h	–
Reserved	–		2	TBD	[28:27]	–	–
Field firmware update status	FFU_STATUS		1	R	[26]	00h	–
Pre-loading data size	PRE_LOADING_DATA_SIZE		4	R/W/E_P	[25:22]	00h	–
Maximum pre-loading data size	MAX_PRE_LOADING_ DATA_SIZE	32GB 64GB 128GB 256GB	4	R	[21:18]	0342AE18h 06855C28h 0D0AB858h 1A1570A8h	–
Product state awareness enablement	PRODUCT_STATE_ AWARENESS_ENABLEMENT		1	R/W/E&R	[17]	43h	–
Secure removal type	SECURE_REMOVAL_TYPE		1	R/W&R	[16]	01h	–
Command queue mode enable	CMDQ_MODE_EN		1	R/W/E_P	[15]	00h	–
Reserved	–		15	TBD	[14:0]	–	2

Notes: 1. Cell type:
R = Read-only;
R/W = One-time programmable and readable;
R/W/E = Multiple writable with the value kept after a power cycle, assertion of the RST_n signal, and any CMD0

reset, and readable;
R/W/C_P = Writable after the value is cleared by a power cycle and assertion of the RST_n signal (the value not cleared by CMD0 reset) and readable;
R/W/E_P = Multiple writable with the value reset after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable;
W/E_P = Multiple writable with the value reset after power cycle, assertion of the RST_n signal, and any CMD0 reset, and not readable

2. Reserved bits should be read as 0.
3. Boot partition size is configurable by host. Refer to local Micron support for information.
4. Micron has tested power failure under best-application knowledge conditions with positive results. Customers may request a dedicated test for their specific application condition. Micron set this register during factory test and used the one-time programming option.
5. Production State Awareness flow is mandatory if content is loaded into the device prior to soldering; programming operations are supported in 20-55°C temperature range.
6. Product NAND endurance is limited as further specified under the applicable device qualification document and Technical Note health information sheets, which are incorporated herein by reference. The applicable Qualification and Reliability Report is available on customer request at the qualification release milestone. The health information, as specified by JEDEC, must be used to monitor a device's memory usage and to retrieve the usage percentage. Refer to Technical Note Health Information for Micron Embedded e.MMC Devices TN-FC-74.

DC Electrical Specifications – Device Power

The device current consumption for various device configurations is defined in the power class fields of the ECSD register.

V_{CC} is used for the NAND Flash device ; V_{CCQ} is used for the controller and for the e.MMC and NAND interface voltage.

Figure 5: Device Power Diagram

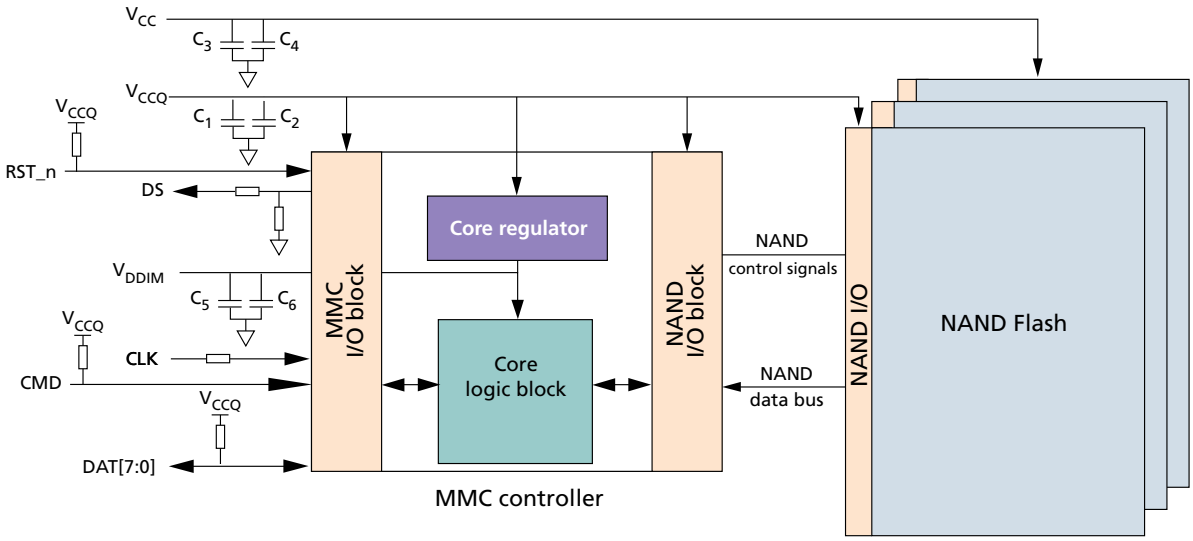


Table 10: Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
V_{CC} = 3.3V, V_{CCQ} = 1.8V nominal	V_{IN}	–0.2	2.4	V
	V_{CC}	–0.6	4.6	V
	V_{CCQ}	–0.2	2.4	V
V_{CC} = 3.3V, V_{CCQ} = 3.3V nominal	V_{IN}	–0.6	4.6	V
	V_{CC}	–0.6	4.6	V
	V_{CCQ}	–0.6	4.6	V

Note: 1. Voltage on any pin relative to V_{SS}.

Table 11: Capacitor and Resistance Specifications

Parameter	Symbol	Min	Max	Typ	Units	Notes
Pull-up resistance: CMD	R_CMD	4.7	50	10	kΩ	1
Pull-up resistance: DAT[7:0]	R_DAT	10	50	50	kΩ	1
Pull-up resistance: RST_n	R_RST_n	4.7	50	50	kΩ	2
CLK/CMD/DS/DAT[7:0] impedance		45	55	50	Ω	3
Serial resistance on CLK	SR_CLK	0	47	22	Ω	
Serial resistance on DS	SR_DS	0	47	22	Ω	4
Pull-down resistance: DS	R_DS	10	100	–	kΩ	
V_{CCQ} capacitor	C1	2.2	4.7	2.2	µF	5
	C2	0.1	0.22	0.1		
V_{CC} capacitor	C3	2.2	4.7	2.2	µF	6
	C4	0.1	0.22	0.1		
V_{DDIM} capacitor (C_{reg})	C5	1	4.7	1	µF	7
	C6	0.1	0.1	0.1		

Notes: 1. Used to prevent bus floating.
2. If host does not use H/W RESET (RST_n), pull-up resistance is not needed on RST_n line (Extended_CSD[162] = 00h).
3. Impedance match.
4. Recommended in order to compensate eventual impedance mismatch on the PCB.
5. The coupling capacitor should be connected with V_{CCQ} and V_{SSQ} as closely as possible.
6. The coupling capacitor should be connected with V_{CC} and V_{SS} as closely as possible.
7. The coupling capacitor should be connected with V_{DDIM} and V_{SS} as closely as possible.

Product Features

The list below shows the JEDEC features not supported. See the full JEDEC/MMC Standard No. 84-B51 available at www.jedec.org/sites/default/files/docs/JESD84-B51.pdf

- Context ID/Data tag (this feature is implemented at the protocol level)
- Dynamic device capacity
- Thermal spec
- Large sector size - 4KB (<256GB)
- Extended security protocol
- Secure erase/secure trim*
- Forced erase*

The list below shows, instead, the main Micron features supported:

- Ultra endurance partitions
- Host initiated refresh
- Auto initiated refresh
- Device health report

* The feature implements as logical erase mode: It moves the mapped host address range to the unmapped host address range. When the operation is complete, the data still exists, but the mapped device address range behaves as if overwritten with all 0s.

Revision History

Rev. F – 10/2023

- Added 32GB IT and WT MPN
- Updated Features section: Added auto initiated refresh, host initiated refresh, multiple partitions with ultra endurance attribute, and production state awareness
- Updated ECSD Register Field Parameters table: Added note
- Removed Temperature Specification table
- Updated Product Features section

Rev. E – 08/2023

- Added 128GB and 256GB WT MPN

Rev. D – 07/2023

- Added 64GB WT MPN

Rev. C – 03/2023

- Updated legal status to Production

Rev. B – 02/2023

- Updated Ordering Information Table (removed ES from MPNs)
- Updated HS400 and HS200 Performance Tables
- Updated HS400 and HS200 Current Consumption Tables
- Updated CID Register Field Parameters Table
- Updated ECSD Register Field Parameters Table

Rev. A – 09/2022

- Initial release

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