PFC Direct current resonance type White LED Driver for Large LCD

BD9412F

General Description

BD9412F is a current resonance type LED Driver with frequency-controlled LED current. It can connect to PFC directly and can use half-bridge structure reducing the number of external components.
It incorporates some protection functions against fault conditions such as Over-Voltage Protection, LED Short Detection (IS High Detection) and LED Open Detection (IS Low Detection).

Key Specifications

- Operating Power Supply Voltage Range: 9.0V to 18.0V
- Oscillator Frequency: 60kHz (R_{RT}=100kΩ)
- Operating Current: 2.3mA (Typ)
- Operating Temperature Range: -40°C to +85°C

Package

	W(Typ) x D(Typ) x H(Max)
SOP18	11.20mm x 7.80mm x 2.01mm
	Pin pitch 1.27mm

Features

- 20V High Rating Process
- 1 Channel Push-pull Control
- Current and Voltage Feedback by Driving Frequency
- Adjustable Soft Start
- Adjustable Timer Latch
- Under-Voltage Detection for IC's Power Line
- Output Over-Voltage Protection
- Output Error Signal from FAIL Terminal
- Shift to Save Mode by STB Terminal
- Burst Control by External PWM Signal
- Analog Dimming by External DC Signal
- Conversion Function from Pulse to DC

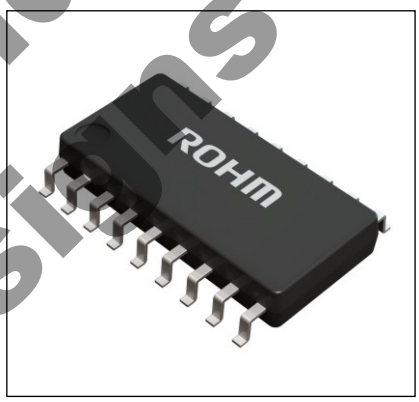


Figure. 1 SOP18

Applications

- TV, Computer Display, LCD Backlighting.

Typical Application Circuit

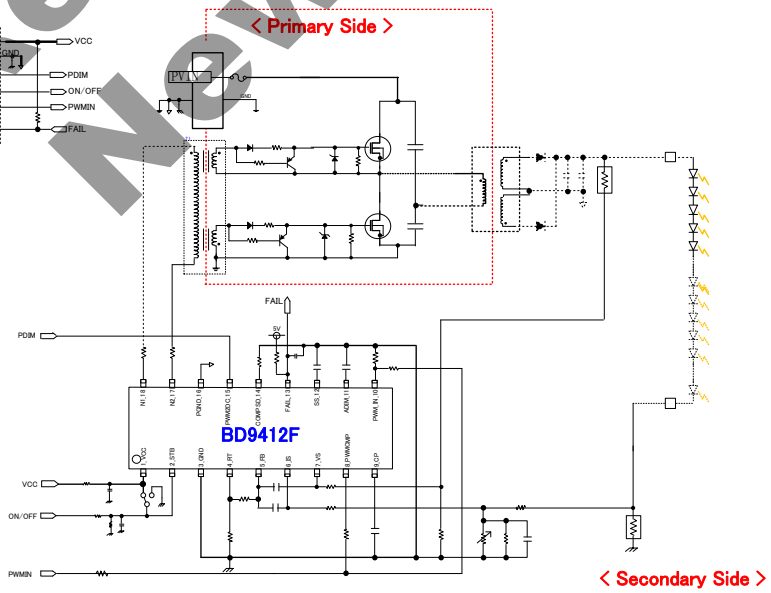


Figure. 2 Typical Application Circuit(s)

Contents

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	20	V
STB, PWM2DC, N2, N1 Terminal Voltage	V_{STB},V_{PWM2DC},V_{N2},V_{N1}	20	V
RT, FB, IS, VS, PWMCMP, CP, PWMIN, ADIM, SS, FAIL, COMPSD Terminal Voltage	V_{RT},V_{FB},V_{IS},V_{VS},V_{PWMCMP}, V_{CP},V_{PWMIN},V_{ADIM},V_{SS}, V_{FAIL},V_{COMPSD}	5.5	V
Power Dissipation	Pd	0.69 (Note 1)	W
Operating Temperature Range	Topr	-40 to +85	°C
Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

(Note 1) Derating in done 5.5 mW/°C for operating above Ta≥25°C (Mount on 1-layer 70.0mm x 70.0mm x 1.6mm board)
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta= -40°C to +85°C)

Parameter	Symbol	Range	Unit
Power Supply Voltage	V_{CC}	9.0 to 18.0	V
PWMIN Input Frequency Range	f_{PWMIN}	60 to 500	Hz
Oscillation Frequency	f_{OUT}	30 to 300	kHz
PWM2DC Input Voltage Range	f_{PWM2DC}	0.09 to 30	kHz
ADIM Input Voltage Range	V_{ADIM}	0 to 5	V
ADIM Range with Linearity IS	$V_{ADIMLIN}$	0.5 to 2.1	V

External Components Recommended Range (Ta= -40°C to +85°C)

Parameter	Symbol	Range	Unit
RT Connection Resistance	R_{RT}	20 to 200	kΩ
CP Connection Capacitance	C_{CP}	0.01 to 2.2 (Note 2)	µF
ADIM Connection Capacitance	C_{ADIM}	0.22 to 10 (Note 2)	µF
SS Connection Capacitance	C_{SS}	0.01 to 0.1 (Note 2)	µF

(Note 2) Please set connection capacitance above Min value of Recommended Range according to temperature characteristic and DC bias characteristic.

Pin Configuration

(TOP VIEW)

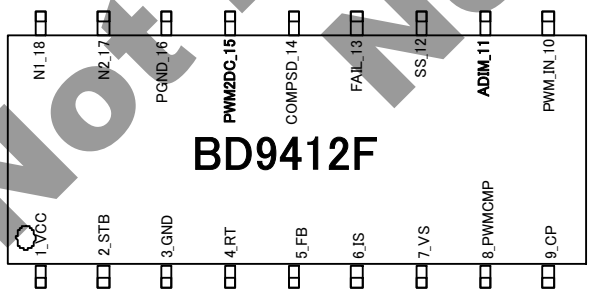
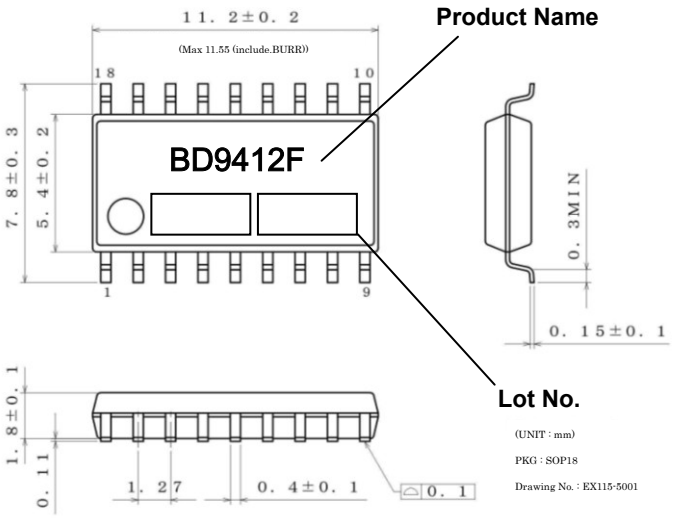


Figure. 3 Pin Configuration

Physical Dimension and Marking Diagram



SOP18(Unit:mm)

Figure. 4 Physical Dimension and Marking Diagram

Electrical Characteristics (Unless otherwise specified Ta=25°C, V_{CC}=12V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
【Whole Device】						
Circuit Current	I_{CC1}	-	2.3	5.0	mA	f_{OUT}=60kHz, $V_{PWMCOMP}$=0V
Circuit Current at Stand-by	I_{CC2}	-	0	20	μA	V_{STB}=0V
【STB Block】						
STB Pin High Voltage	V_{STH}	2.0	-	V_{CC}	V	System ON
STB Pin Low Voltage	V_{STL}	-0.3	-	+0.8	V	System OFF
【VCC UVLO Block】						
VCC Operation Voltage	V_{VCCUVP}	7.5	8.0	8.5	V	
VCC UVLO Hysteresis	ΔV_{VCCUVP}	0.37	0.50	0.63	V	
【OSC Block】						
RT Terminal voltage	V_{RT}	1.05	1.50	1.95	V	
【PWMIN Block】						
PWMIN Pin High Voltage	V_{PWMINH}	1.8	-	5.0	V	
PWMIN Pin Low Voltage	V_{PWMINL}	-0.3	-	+0.8	V	
【Soft Start Block】						
Setting Current for Soft Start Timer and COMPSD Timer	I_{SS}	1.5	2.0	2.5	μA	
Soft Start Ended Voltage	V_{SSEND}	2.30	2.50	2.70	V	
Setting Voltage for COMPSD Timer	V_{SDON}	1.90	2.00	2.10	V	
【Feed Back Block】						
IS Threshold Voltage 1	V_{IS1}	0.466	0.477	0.488	V	V_{ADIM}=2.1V, V_{PWM2DC}=12V
IS Threshold Voltage 2	V_{IS2}	0.239	0.250	0.261	V	V_{ADIM}=1.1V, V_{PWM2DC}=12V
IS Threshold Voltage 3	V_{IS3}	0.102	0.114	0.126	V	V_{ADIM}=0.5V, V_{PWM2DC}=12V
IS Threshold Voltage 4	V_{VS}	1.212	1.250	1.288	V	
IS Source Current 1	I_{IS1}	-	-	0.9	μA	V_{PWMIN}=2.5V
IS Source Current 2	I_{IS2}	40	50	60	μA	V_{PWMIN}=0V, V_{IS}=0.8V
VS Source Voltage	I_{VS}	-	-	0.9	μA	
IS COMP Detection Voltage 1	$V_{ISCOMP1}$	0.020	0.050	0.080	V	IS sweep down V_{ADIM}=0.4V
IS COMP Detection Voltage 2	$V_{ISCOMP2}$	0.90	1.00	1.10	V	IS sweep up

Electrical Characteristics – continued (Unless otherwise specified Ta=25°C, V_{CC}= 12V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Min		
【Output Block】						
N1 Output Sink Resistance	R_{N1SI}	1.5	3.0	6.0	Ω	
N1Output Source Resistance	R_{N1SO}	4.5	9.0	18.0	Ω	
N2 Output Sink Resistance	R_{N2SI}	1.5	3.0	6.0	Ω	
N2 Output Source Resistance	R_{N2SO}	4.5	9.0	18.0	Ω	
MAX DUTY	MAX DUTY	43.0	45.0	47.0	%	f_{OUT}=60kHz
N1-N2,N2-N1Dead Time	t_{OFF}	100	200	400	ns	
Output Frequency	f_{OUT}	57.9	60.0	62.1	kHz	R_{RT}=100kΩ
【Timer Block】						
Setting Voltage for CP Time	V_{CP}	1.90	2.00	2.10	V	
Setting Current for CP Time	I_{CP}	0.85	1.00	1.15	μA	
【ADIM Block】						
ADIM Pin Inflow Current 1	I_{ADIM1}	-5	0	+5	μA	V_{ADIM}=2.2V, V_{PWM2DC}=12V
ADIM Pin Inflow Current 2	I_{ADIM2}	19	28	37	μA	V_{ADIM}=5V, V_{PWM2DC}=12V
PWM2DC Pin Inflow Current	I_{PWM2DC}	4	6	8	μA	V_{PWM2DC}=3V
PWM2DC Pin High Voltage	$V_{PWM2DCH}$	1.8	-	5.0	V	
PWM2DC Pin Low Voltage	$V_{PWM2DCL}$	-0.3	-	+0.8	V	
PWM2DC Pin Selected Voltage to High Impedance	$V_{PWM2DCZ}$	7.5	8.0	8.5	V	PWM2DC=sweep up
【COMPSD Block】						
COMPSD Detection Voltage	V_{COMPSD}	3.88	4.00	4.12	V	
【FAIL Block】						
FAIL Pin ON-Resistance	R_{FAIL}	-	100	200	Ω	

Pin Description

Pin No.	Pin Name	IN/OUT	Function	Rating [V]
1	VCC	IN	Power Supply Pin for IC (Built-In UVLO Function)	-0.3 to +20
2	STB	IN	Power ON/OFF Control Pin for IC Power OFF when STB=L and Power ON when STB=H.	-0.3 to +20
3	GND	IN	Ground Pin for Internal Signal in IC	-
4	RT	OUT	Drive Frequency Setting Pin Basic Frequency is set by the resistor between RT and GND and Drive Frequency Modulation Range is set by the resistor between RT and FB.	-0.3 to +5.5
5	FB	OUT	Error Amplifier Output pin for LED Current feedback and LED Voltage feedback	-0.3 to +5.5
6	IS	IN	Error Amplifier Input pin for LED Current feedback	-0.3 to +5.5
7	VS	IN	Error Amplifier Input pin for LED Open Voltage feedback	-0.3 to +5.5
8	PWMCMP	IN	PWM Comparator Input Pin which controls PWM operation during brightness adjustment. N1 and N2 output stop when PWMCMP=L, and they output Max Duty when PWMCMP=H	-0.3 to +5.5
9	CP	OUT	Timer Latch Setting Pin In abnormal case, 1μA (Typ) will be charged to the capacitor connected to CP, and IC becomes latch status after output operation stops at CP>2V(Typ)	-0.3 to +5.5
10	PWMIN	IN	PWM Signal Input Pin for burst brightness adjustment	-0.3 to +5.5
11	ADIM	IN	DC Signal Input Pin for analog dimming	-0.3 to +5.5
12	SS	OUT	Soft Start timer and COMPSD timer Setting Pin During start-up, 2μA (Typ) will be charged to connected capacitor. At SS>2.0V(typ), COMPSD can start to detect. At SS>2.5V (typ), CP can accept charge operation.	-0.3 to +5.5
13	FAIL	OUT	Error Indication Signal Output Pin Normal : L, Error : Open	-0.3 to +5.5
14	COMPSD	IN	Abnormal Over Voltage Detection Pin When detecting abnormality, output operation stops and IC becomes latch status after 2 clocks.	-0.3 to +5.5
15	PWM2DC	IN	Pulse to DC converting pin Pulse Signal is translated to flat dc level by 100kΩ resistor in IC and the capacitor connected to ADIM.	-0.3 to +20
16	PGND	IN	Power Ground for external MOSFET drive	-
17	N2	OUT	Output pin for external FET drive circuit (Channel N2)	-0.3 to +20
18	N1	OUT	Output pin for external FET drive circuit (Channel N1)	-0.3 to +20

I/O Equivalent Circuits

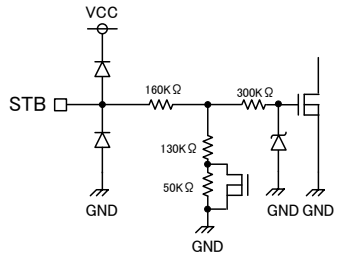
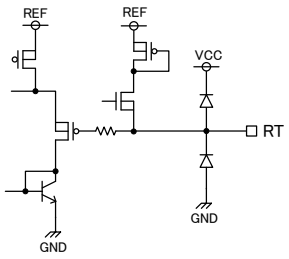
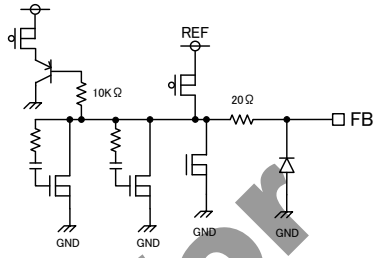
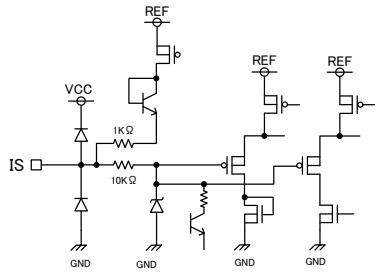
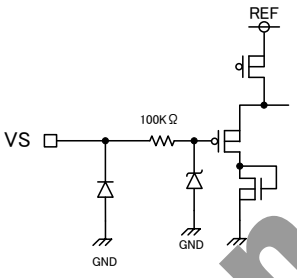
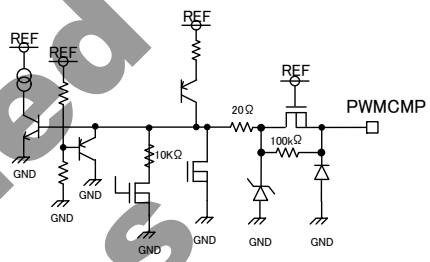
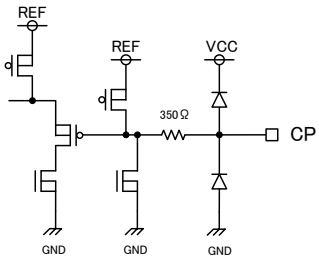
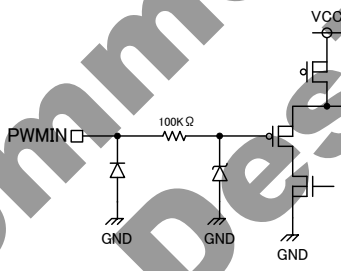
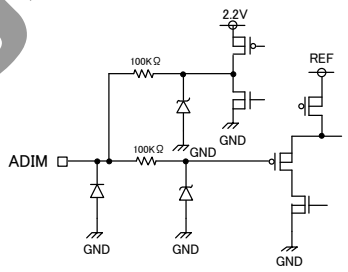
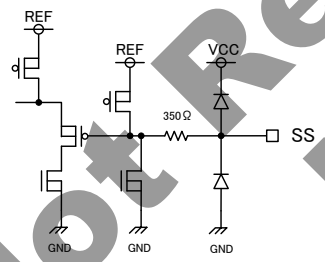
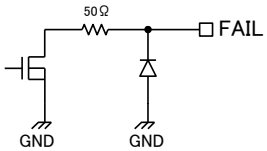
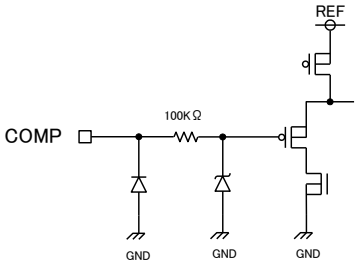
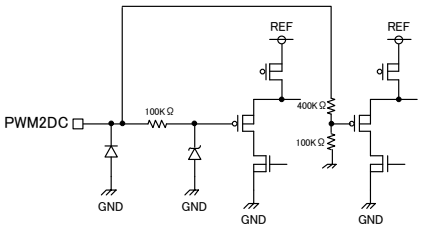
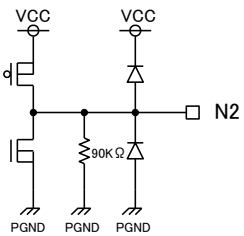
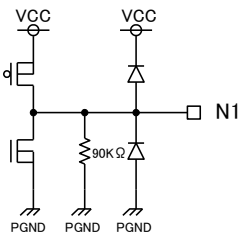
STB	RT	FB
		
IS	**VS**	**PWMCMP**
		
CP	**PWMIN**	**ADIM**
		
SS	**FAIL**	**COMPSD**
		
PWM2DC	**N2**	**N1**
		

Figure. 5 I/O equivalent circuit

Block Diagram

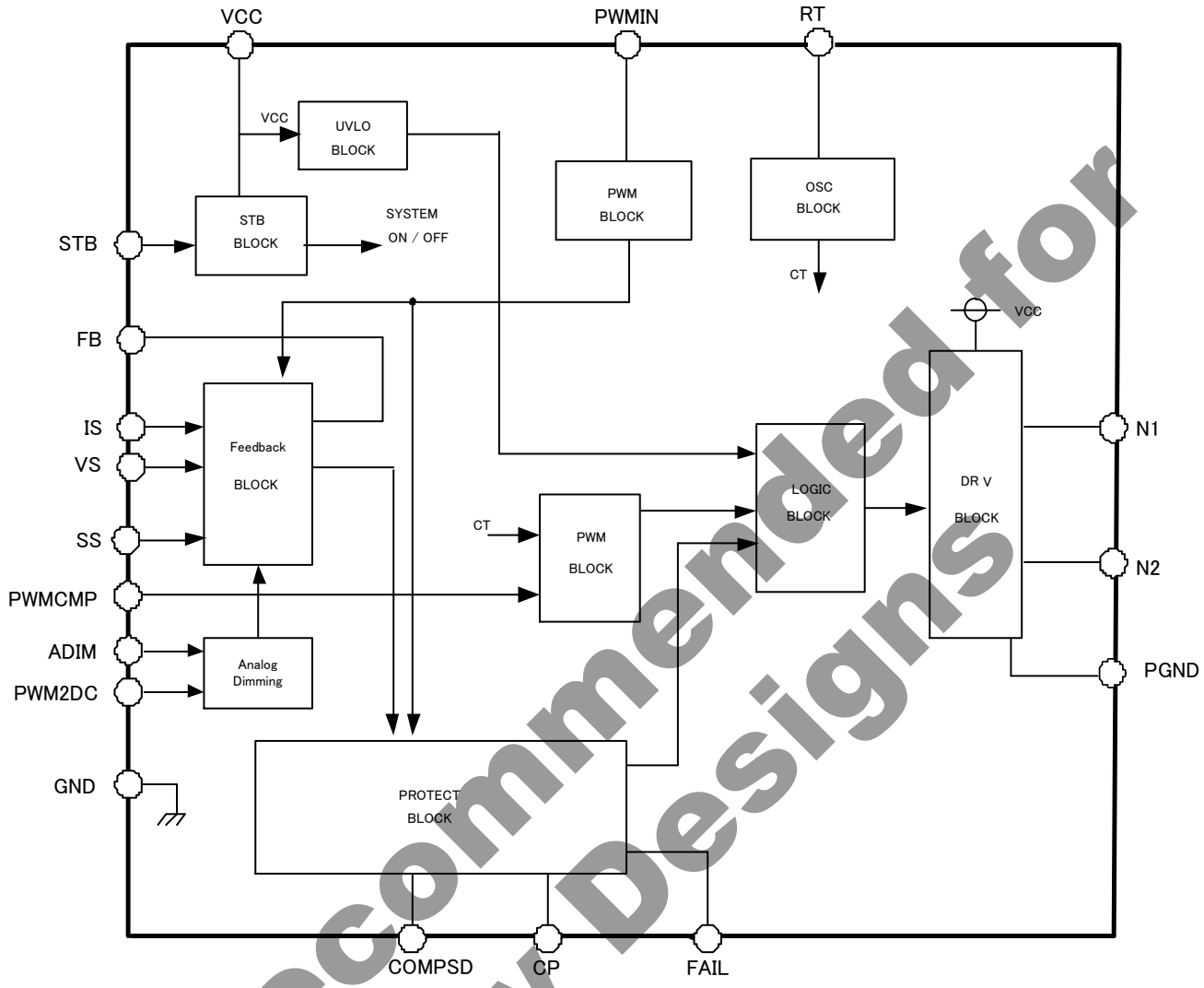


Figure. 6 Block Diagram

Typical Performance Curves

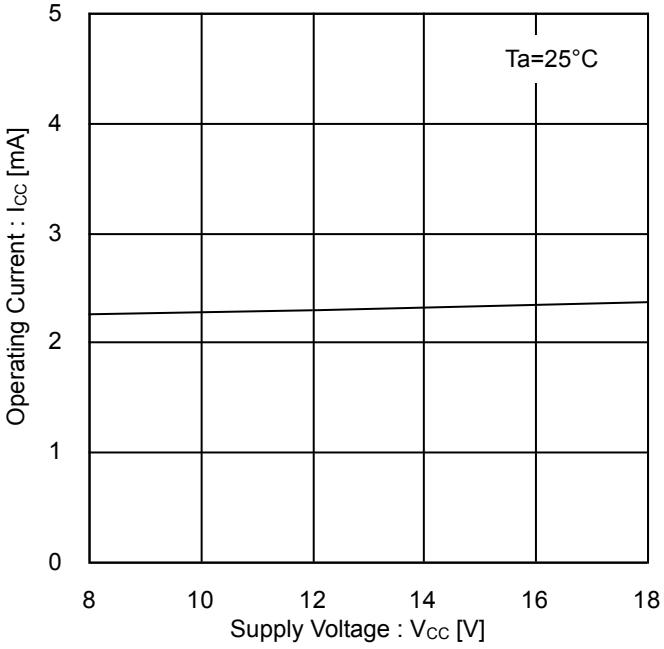


Figure 7. Operating Current vs Power Supply Voltage

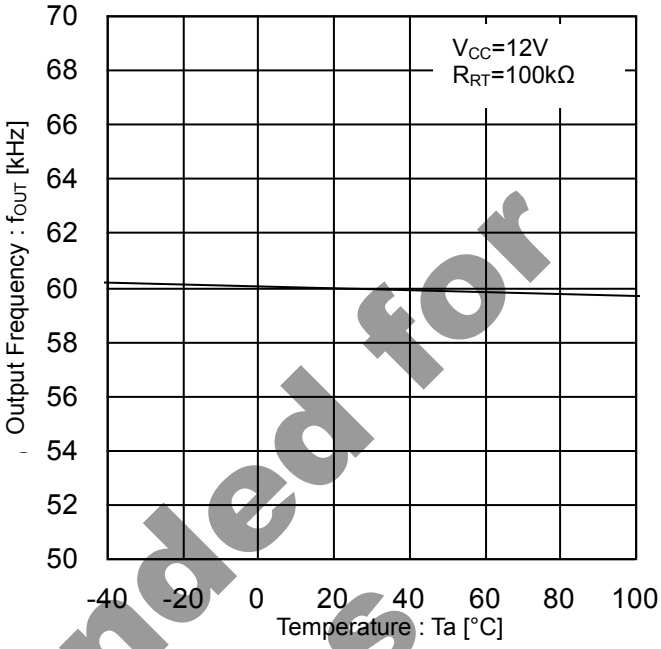


Figure 8. Output Frequency vs Temperature

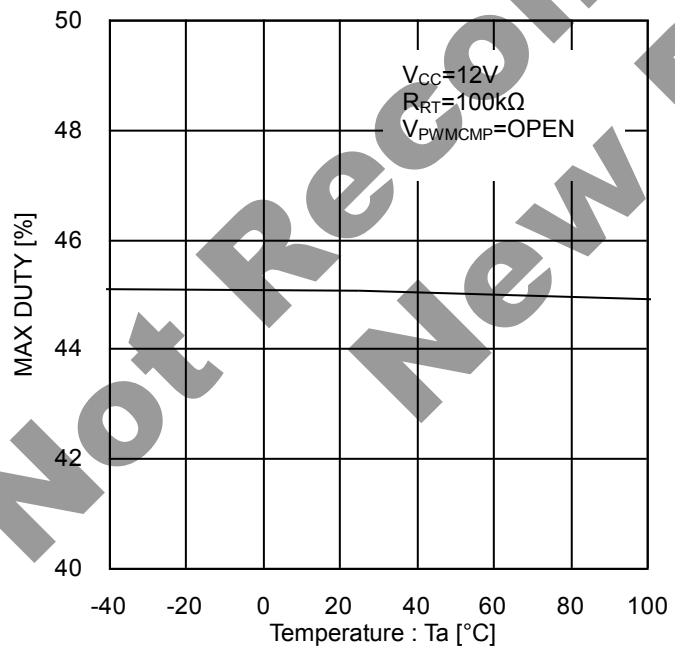


Figure 9. MAX DUTY vs Temperature

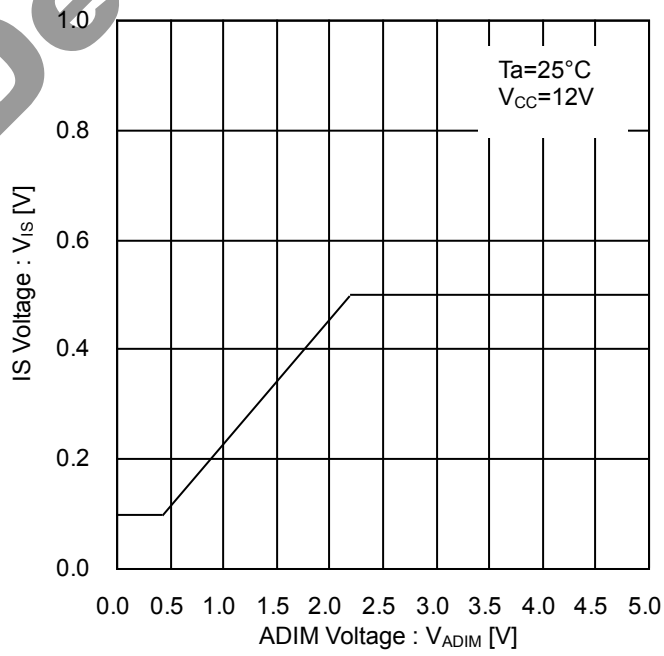


Figure 10. IS Voltage vs ADIM Voltage

Pin Function Description

PIN.1 VCC

This is power supply pin for the IC. Normal operation range (Typ) is from 9V to 18V. Please place ceramic capacitor bigger than 0.1μF as bypass capacitor between VCC and GND. It is for noise elimination.

PIN.2 STB

This PIN is for setting of ON/OFF. It is possible to use as reset when shutting down.
Please set the STB terminal voltage below VCC voltage. In addition, please set below 4V if the voltage is applied earlier than VCC.
Depending on input voltage to STB pin, the status of IC might be switched (ON/OFF). Please avoid using between the two status (0.8V to 2.0V)

PIN.3 GND

This is signal system GND for IC inside. Please make it independent from PGND as much as possible (We recommend this because it has less influence with switching noise which comes from short circuit of PGND and GND at connector close to GND pin.

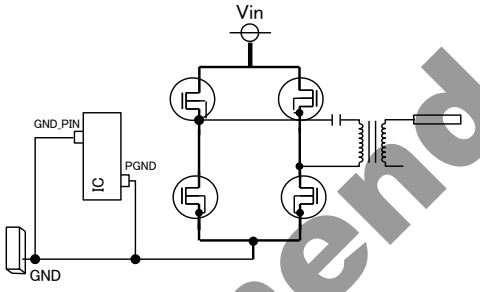


Figure. 11

PIN.4 RT

Set up the charge/discharge current by frequency of IC inside.
By changing the resistance value of resistor between RT pin and GND, it is possible to set up basic drive frequency as following formula;
Basic frequency means output N1, N2 frequency which is determined only with resistor between RT pin and GND.

$$f_{OUT} = \frac{6000}{R_{RT}[k\Omega]}[kHz] \qquad (f_{OUT} < 200kHz)$$

$$f_{OUT} = \frac{6673}{R_{RT}[k\Omega] + 3.336}[kHz] \qquad (f_{OUT} > 200kHz)$$

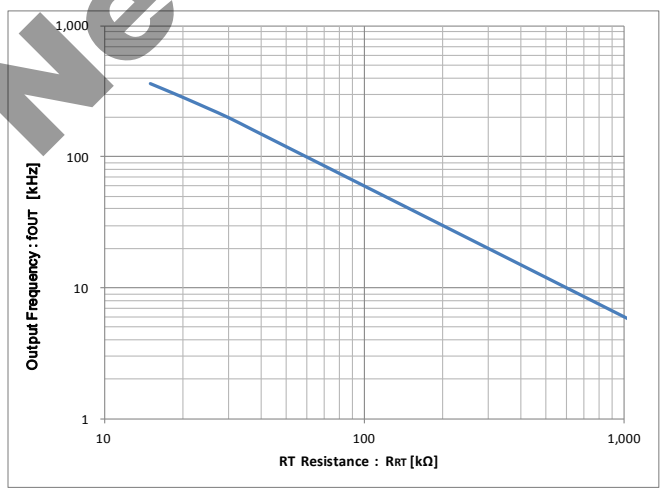
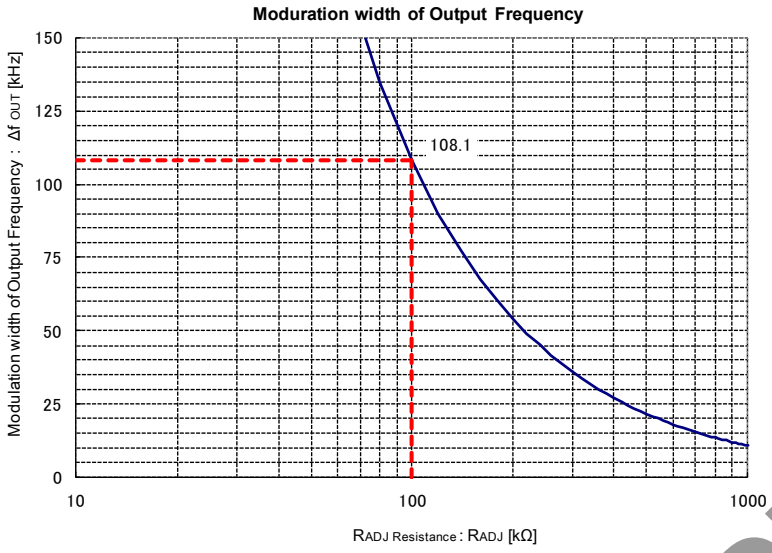


Figure. 12 RT Resistance vs Output Frequency

There is a discrepancy between theoretical formula and actual device. For frequency setting, please thoroughly verify it with actual application. In addition, frequency may change upon resistor RADJ which is placed between RT and FB pins

PIN.5 FB

This is output pin for LED current feedback (IS pin) error amplifier and open LED voltage feedback (VS pin) error amplifier. The capacitance between FB and IS (1500pF to 0.01μF) also determines start up time of LED current necessary during phase compensation and brightness adjustment. Capacitance between FB and VS (1500pF to 0.01μF) is for phase compensation of error amplifier.

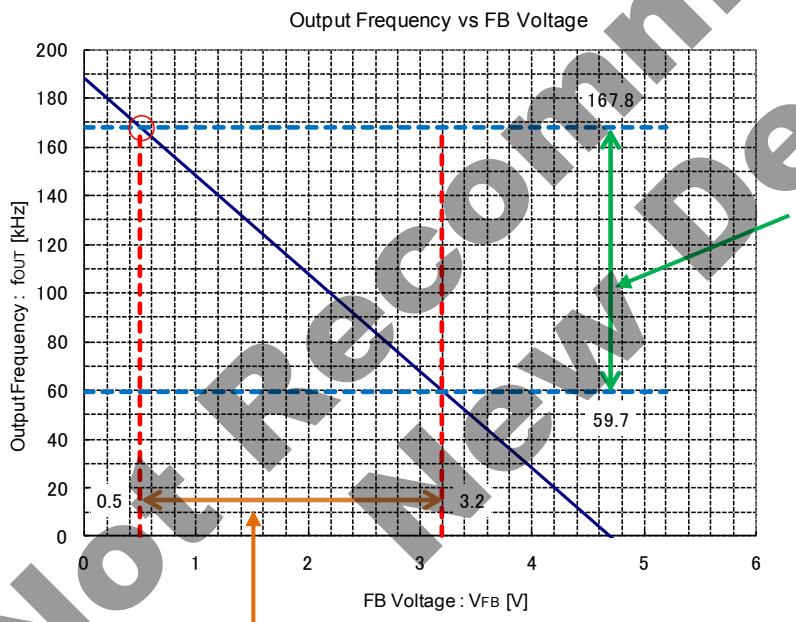


As shown by left graph, by changing resistor R_{ADJ} between RB and RT, it is possible to determine the modulation width of frequency.

Modulation width of frequency determined by the resistor between RB and RT resistor (Theoretical formula : Example)

When R_{ADJ}=100kΩ , Δ f_{OUT}=108.1kHz

Figure. 13 Modulation width of Output Frequency vs R_{ADJ} Resistance



Modulation width of frequency determined by the resistor between RB and RT resistor (Theoretical formula : Example)

When R_{ADJ}=100kΩ , Δ f_{OUT}=108.1kHz

Figure. 14 Output Frequency vs FB Voltage

The basic drive frequency is determined by resistor R_{RT} which is connected from RT pin to GND. The basic frequency is the one at V_{FB}=1.5V, and operation frequency range will be fixed with frequency modulation width that is determined by R_{ADJ} under this condition. When R_{RT}=51kΩ, f_{OUT}=127.7kHz becomes to basic drive frequency.

PIN.6 IS

This is input pin of LED current feedback (IS pin) error amplifier. Please set up as normal voltage (ADIM/4.4)V (Typ). When IS pin voltage becomes less than (ADIM/8.8)V (Typ) or higher than 1.0V, the output will be stopped and latched.

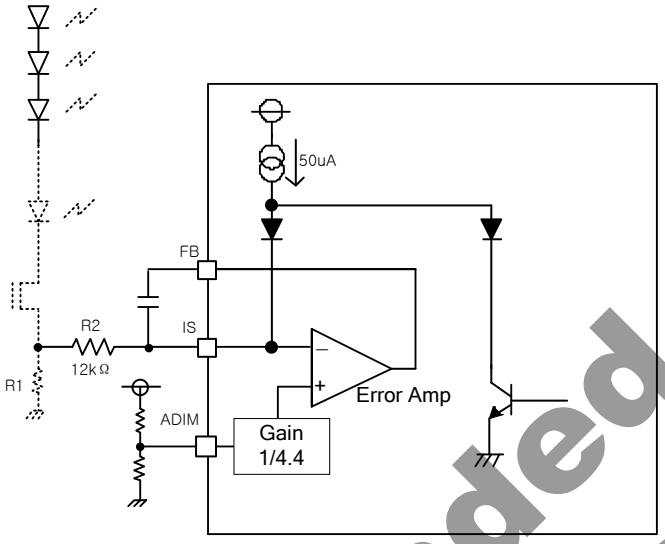


Figure. 15 IS Block Diagram

50μA (Typ) current flows from IS pin to external resistor during OFF period of burst brightness adjustment.

Considering Min value of IS source current during burst brightness adjustment, please set that total resistance from IS Pin to GND is from 8kΩ to 22kΩ. When R_2 is 12kΩ in above diagram, please set 8kΩ < R_1 + R_2 < 22Kω

PIN.7 VS

This is input pin of Open LED voltage feedback (VS pin) error amplifier. It has to be 1.25V during LED is open. When LED is ON, it will be 0.5V to 1.0V. When VS pin becomes over 1.25V, protection circuit will start operation, and if it becomes more than CP timer set up time (Timer Latch), it will shut down.

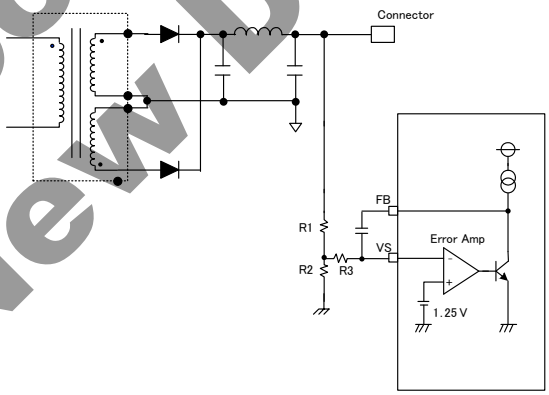


Figure. 16 VS Block Diagram

Please set C_1, C_2, R_1, R_2, and R_3 value to input 1.25V to VS pin during LED bar's connector disconnects.

PIN.8 PWMCMP

PWMCOMP pin voltage is fixed by DUTY of drive output N1, N2 in comparison with a saw wave of IC inside. This pin has 100μA sink/source current capability and when external capacitor is connected between PWMCMP and GND, IC will operate PWM at brightness start up stage. When N1 and N2 only drive at MaxDuty, please set PWMCMP=open.

PIN.9 CP

This pin sets up the time from the point of abnormal detection till shut down (Timer Latch). Having 1μA constant current charges at external capacitor connected to CP pin, it will shut down when it becomes over 2.0V. During soft start, there is no charge to CP external capacitor even fulfilling CP pin charge condition (timer latch). External capacitor is set around 0.01μF to 2.2μF).

$$T_{CP} = C_{CP} \times \frac{V_{CP}}{I_{CP}} = \frac{C_{CP} \times 2.0}{1.0 \times 10^{-6}} = 2.0 \times 10^{6} \times C_{CP} \quad [\text{sec}]$$

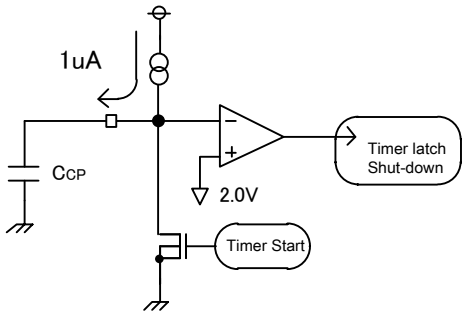


Figure. 17 CP Block Diagram

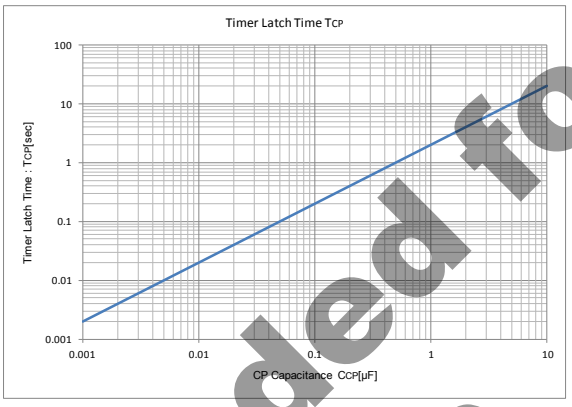


Figure. 18 Timer Latch Time vs CP Capacitance

PIN.10 PWMIN

By inputting PWM pulse signal at PWMIN pin, it is possible to adjust burst brightness. (High level: over 1.8V, Low level: below 0.8V).

condition	LED condition
PWMIN : 1.8V to 5.0V	Turn On
PWMIN : -0.3V to 0.8V	Turn Off

PIN.11 ADIM

ADIM pin is Input and Output Pin of DC signal for analog dimming. According to ADIM Input level, each pin's function is changed as the followings. Pulse-DC translation Circuit is shown in Figure.20.

PWM2DCinput level	PWM2DC function	ADIM function	Needed Signal from External
-0.3V<PWM2DC<6.5V	Pulse Signal Input for Analog Dimming	DC Signal Output for Analog Dimming	DUTY Signal for Analog Dimming
8.5V<PWM2DC<20V	Mask PWM2DC's Function	DC Signal Input for Analog Dimming	DC Signal Output for Analog Dimming

The voltage that ADIM voltage multiplies by (1/4.4) becomes IS threshold voltage and it has linear characteristic. But, ADIM voltage becomes under 0.44V(Typ), IS threshold voltage is clamped at 0.44V/0.44=0.1V(Typ). And ADIM voltage becomes over 2.2V(Typ), IS threshold voltage is clamped at 2.2V/0.44=0.5V(Typ). When you want to use linear characteristic range, please set ADIM voltage from 0.5V to 2.1V.
And pulse signal inputs to PWM2DC terminal and IC can average it by IC internal 100kΩ and the capacitor connected to ADIM terminal (This means pulse to DC signal transfer circuit.). At this time, ADIM ripple level is changed by ADIM's capacitance, therefore please set suitable capacitance according to set specification.

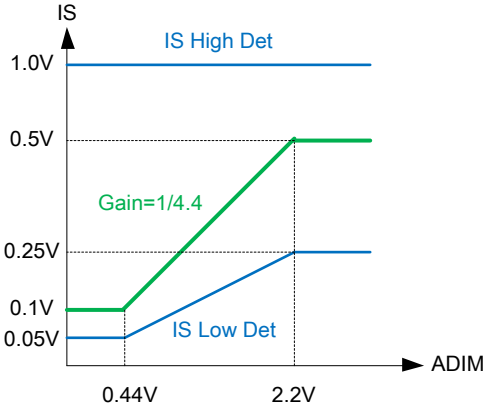


Figure. 19 IS threshold voltage vs ADIM voltage

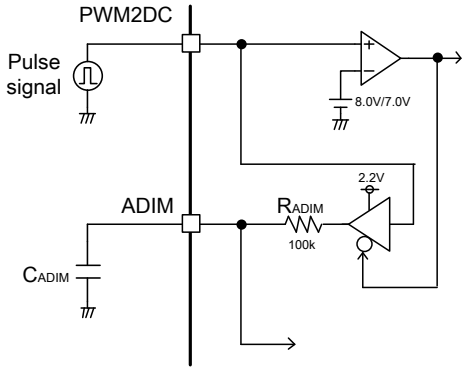
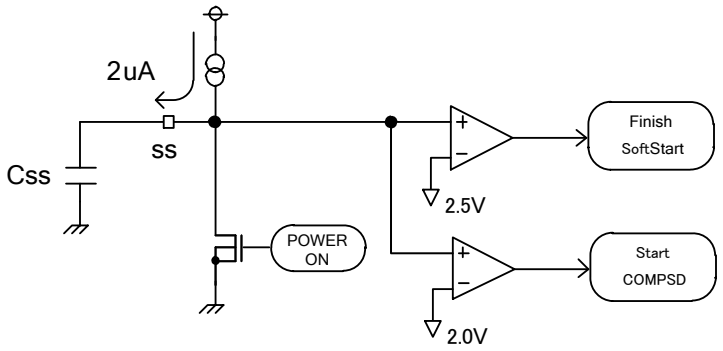


Figure. 20 Pulse to DC transfer block diagram

PIN.12 SS

This is soft start time and SDON time set up pin. Constant current 2.0μA(Typ) is charged to external capacitor (0.01μF to 0.1μF). When SS terminal voltage is higher than 2.0V, COMPSD can be detected. When SS terminal voltage is less than 2.0V, latch protection circuit will not operate. When SS terminal voltage is higher than 2.5V, soft start completes. When soft start is under operation (SS pin voltage is less than 2.5V), timer latch protection circuit by CP charge will not operate.



Where:
C_{SS} is the capacitance of SS pin

Figure. 21 SS Block Diagram

$$T_{SSEND} = C_{SS} \times \frac{V_{SSEND}}{I_{SS}} = \frac{C_{SS} \times 2.5}{2.0 \times 10^{-6}} = 1.25 \times 10^{6} \times C_{SS} \quad [\text{sec}]$$

$$T_{SDON} = C_{SS} \times \frac{V_{SDON}}{I_{SS}} = \frac{C_{SS} \times 2.0}{2.0 \times 10^{-6}} = 1.0 \times 10^{6} \times C_{SS} \quad [\text{sec}]$$

PIN.13 FAIL

This is fail signal output pin of IC. At normal situation, it outputs GND Level and it becomes Open after timer latch in case any abnormality is detected. The pull up voltage during Open must be set less than rated voltage 5.5V of FAIL pin.

Condition	FAILOutput
Normal operation	GND Level
Abnormal operation	Open

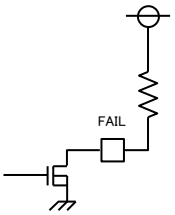


Figure. 22 FAIL Block Diagram

PIN.14 COMPSD

This is input pin for over voltage protection circuit comparator. The detection voltage of comparator is 4.0V(Typ),and will start charging to CP pin after over voltage detection. After CP is charged, it will shut down by timer latch.

PIN.15 PWM2DC

Pulse signal inputs to PWM2DC terminal and IC can average it by IC internal 100kΩ and the capacitor connected to ADIM terminal (This means pulse to DC signal transfer circuit.). When the voltage that is higher than 8V(Typ) forces to PWM2DC terminal, buffer output in the IC becomes high impedance, and IC function shifts to direct DC input mode to ADIM. (Refer to the diagram of PIN11 ADIM.)

PIN.16 PGND

This is Power GND pin for output pin N1, N2 at driver part. Please make it independent from GND (Pin 3) pin on inverter PCB. This pin is not connected to GND pin in IC inside.

PIN.17 N2

This is gate drive output pin for Low Side external Nch FET. Normally please connect it to FET gate through about 10Ω resistor. It is for noise reduction. Gate has to be pull-down to source by resistor of 1kΩ to 10kΩ.

PIN.18 N1

This is gate drive output pin for Low Side external Nch FET. Normally please connect it to FET gate through about 10Ω resistor. It is for noise reduction. Gate has to be pull-down to source by resistor of 1kΩ to 10kΩ.

Detection Condition List of the Protection Functions (Typ Condition)

Protect Function	Detection Pin	Detect Condition		Release Condition	Timer Operation	Protection Type
		Detection Condition	SS			
LED OPEN	IS	(ADIM<0.44V) IS < 0.05V (0.44V<ADIM<2.2V) IS < ADIM/8.8 (ADIM>2.2V) IS < 0.25V	SS>2.0V	(ADIM<0.44V) IS > 0.05V (0.44V<ADIM<2.2V) IS > ADIM/8.8 (ADIM>2.2V) IS > 0.25V	2CLK	Latch off
LED SHORT	IS	IS > 1.0V	SS>2.0V	IS < 1.0V	2CLK	Latch off
OVP	VS	VS > 1.25V	SS>2.5V	VS < 1.25V	CP	Latch off
VCC UVLO	VCC	VCC < 8.0V	-	VCC < 7.5V	-	Restart by release
COMPSD	COMPSD	COMPSD > 4.0V	SS>2.0V	COMPSD < 3.8V	2CLK	Latch off

To reset the latch type protection, please set STB logic to 'L' once. Otherwise the detection of VCCUVLO is required. The count number in the list is calculated with double of output frequency.

Behavior List of the Protect Function

Protect Function	Operation of the Protect Function		
	N1,N2 Output	SS pin	FAIL pin
LED OPEN	Stop after latch	Low after latch	High after latch
LED SHORT	Stop after latch	Low after latch	High after latch
OVP	Stop after latch	Low after latch	High after latch
VCC UVLO	Stop immediately	Low Immediately	High Immediately
COMPSD	Stop after latch	Low after latch	High after latch

Application Example

Introduce an application example with BD9412F

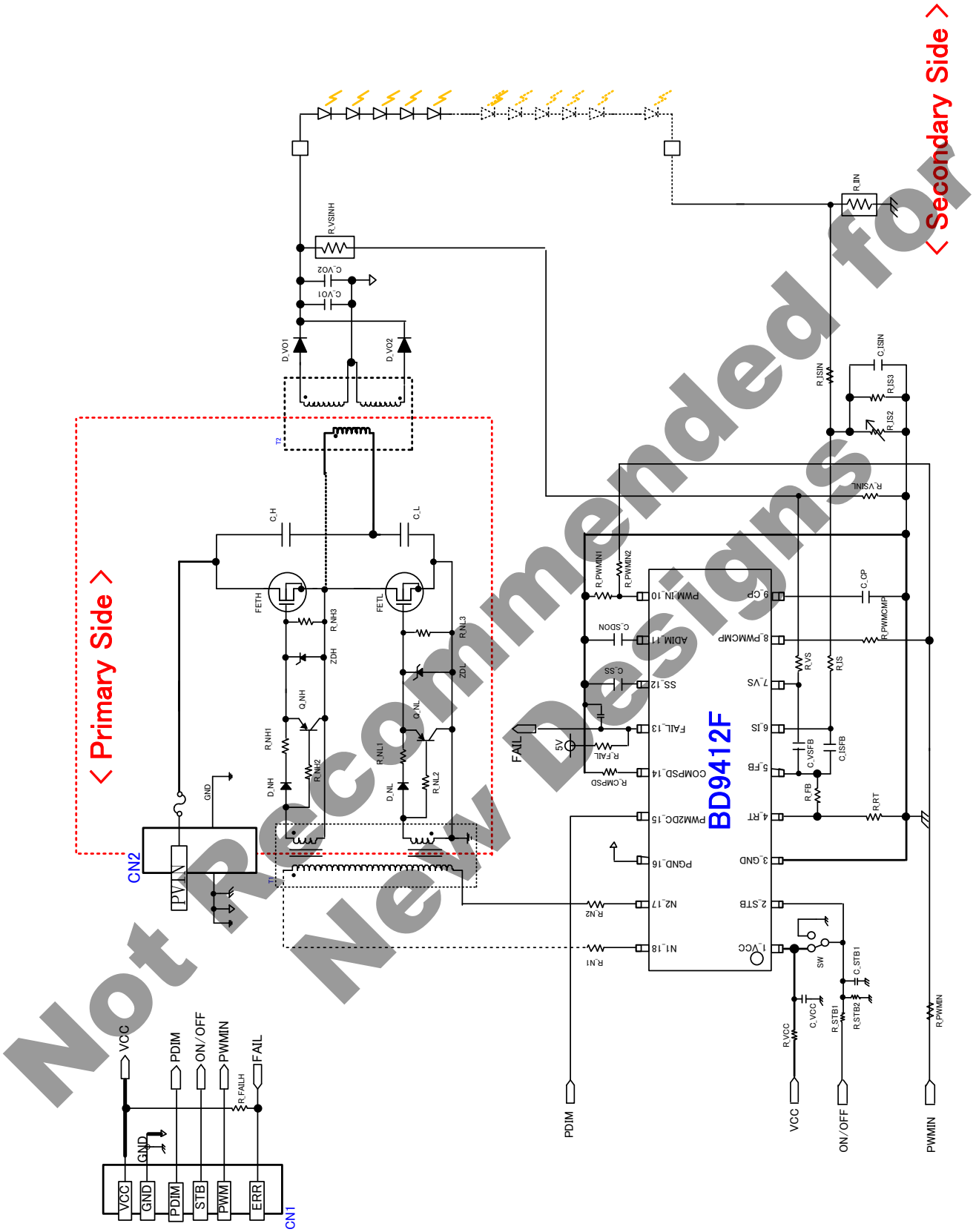


Figure. 23 Application Example

Timing Chart

When it Detects Quick Detection Type Error

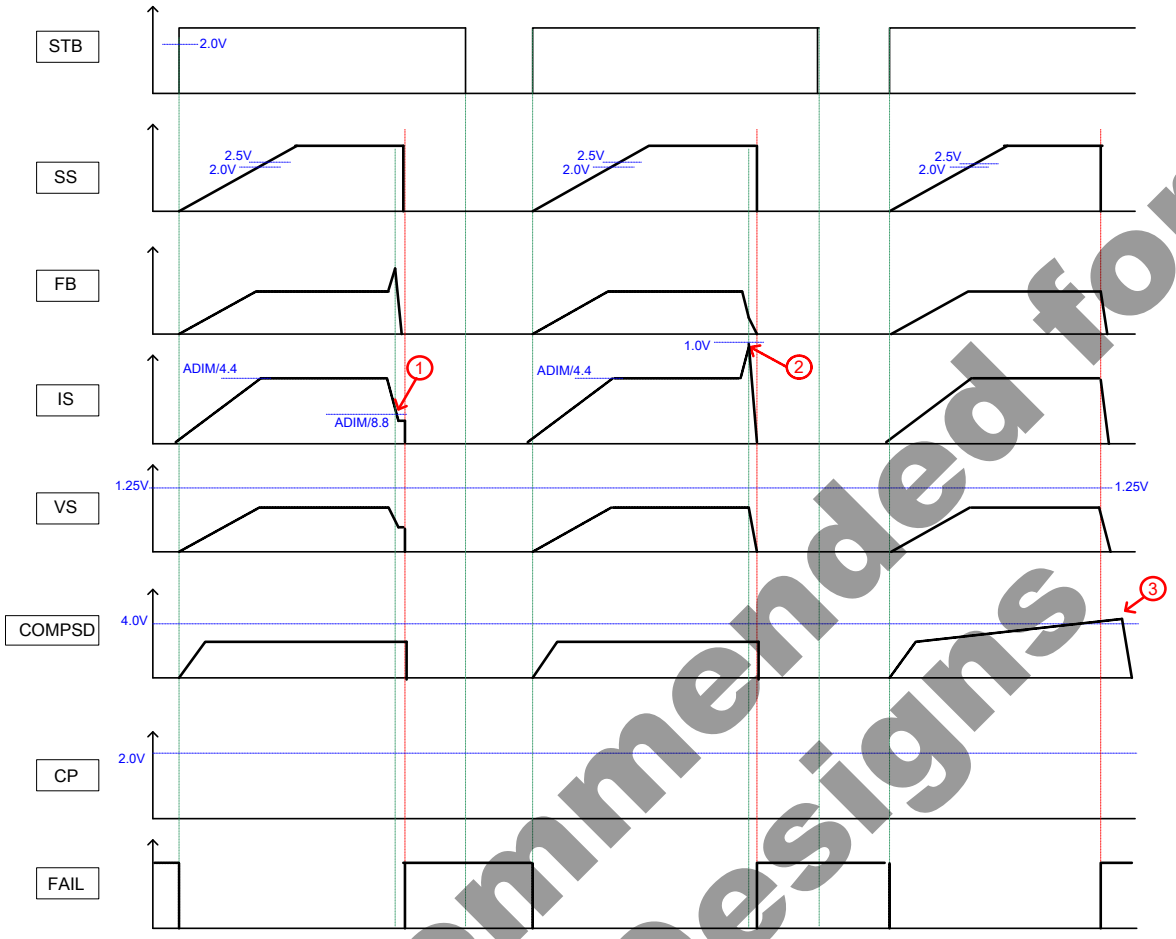


Figure. 24 Timing Chart 1

[The explanation of quick abnormal detection]

Due to the timing of ① to ③ in the above chart, the IC detects malfunction and starts the output-mute latch without CP Charge . For ① to ③, the malfunction is detected according to the conditions in the table shown below.

No.	Content of Abnormal Detection	Condition of Abnormal Detection
①	Abnormal LED current detection	IS<(ADIM/8.8)V
②	Abnormal LED short detection	IS>1.0V
③	COMPSD Over Voltage detection	COMPSD≥ 4.0V

When it Detects Timer Latch Type Error

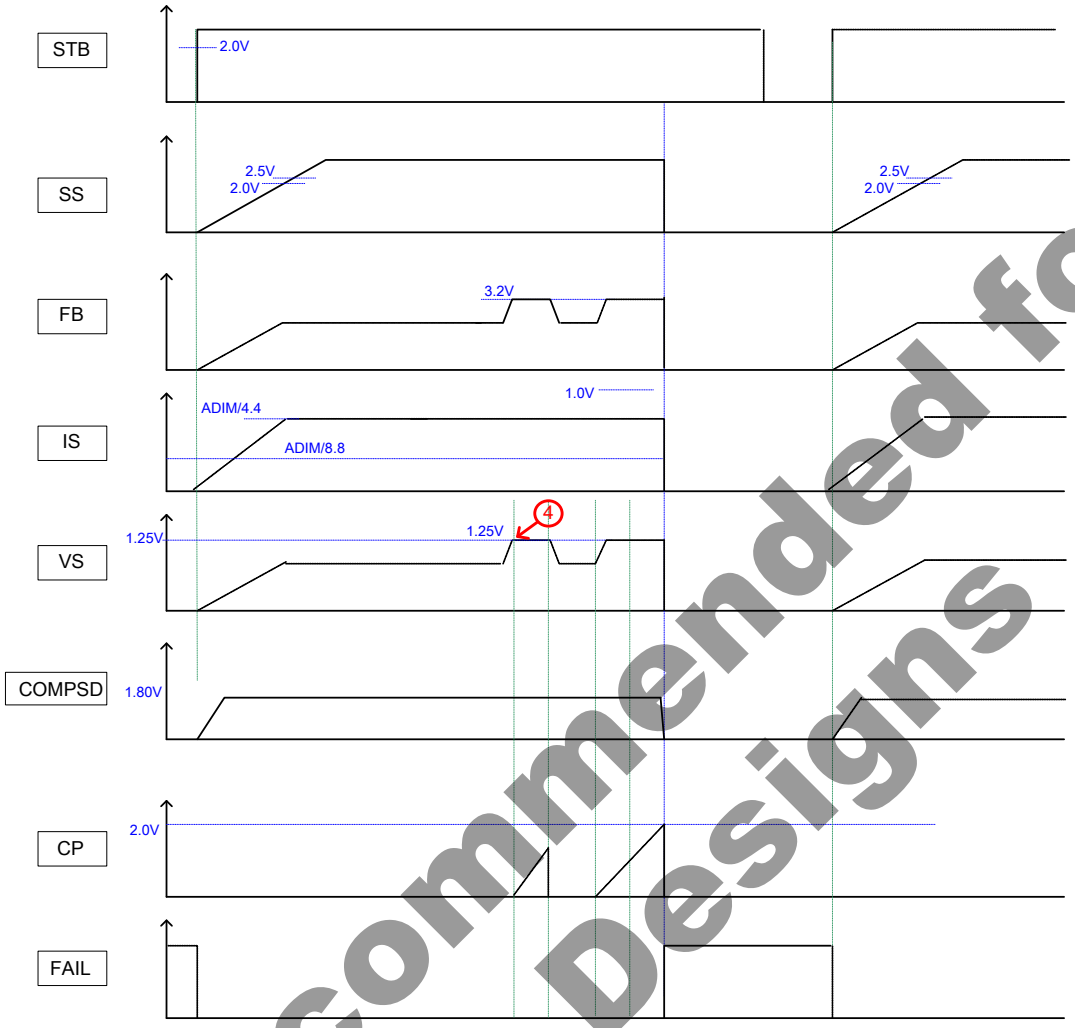


Figure. 25 Timing Chart 2

[The explanation of Time latch type error detection]
Due to the timing of ④ in the above chart, the IC detects abnormal and starts the timer latch charging. For ④, the abnormal is detected according to the conditions in the table shown below.

No.	Content of Abnormal Detection	Condition of Abnormal Detection
④	Abnormal LED voltage detection	VS≥ 1.25V

Output Timing Chart

BD9412F outputs the signal that operates the Push-Pull or Half-Bridge which is made up of Nch FET. The output timing of drive signal is shown in the following chart

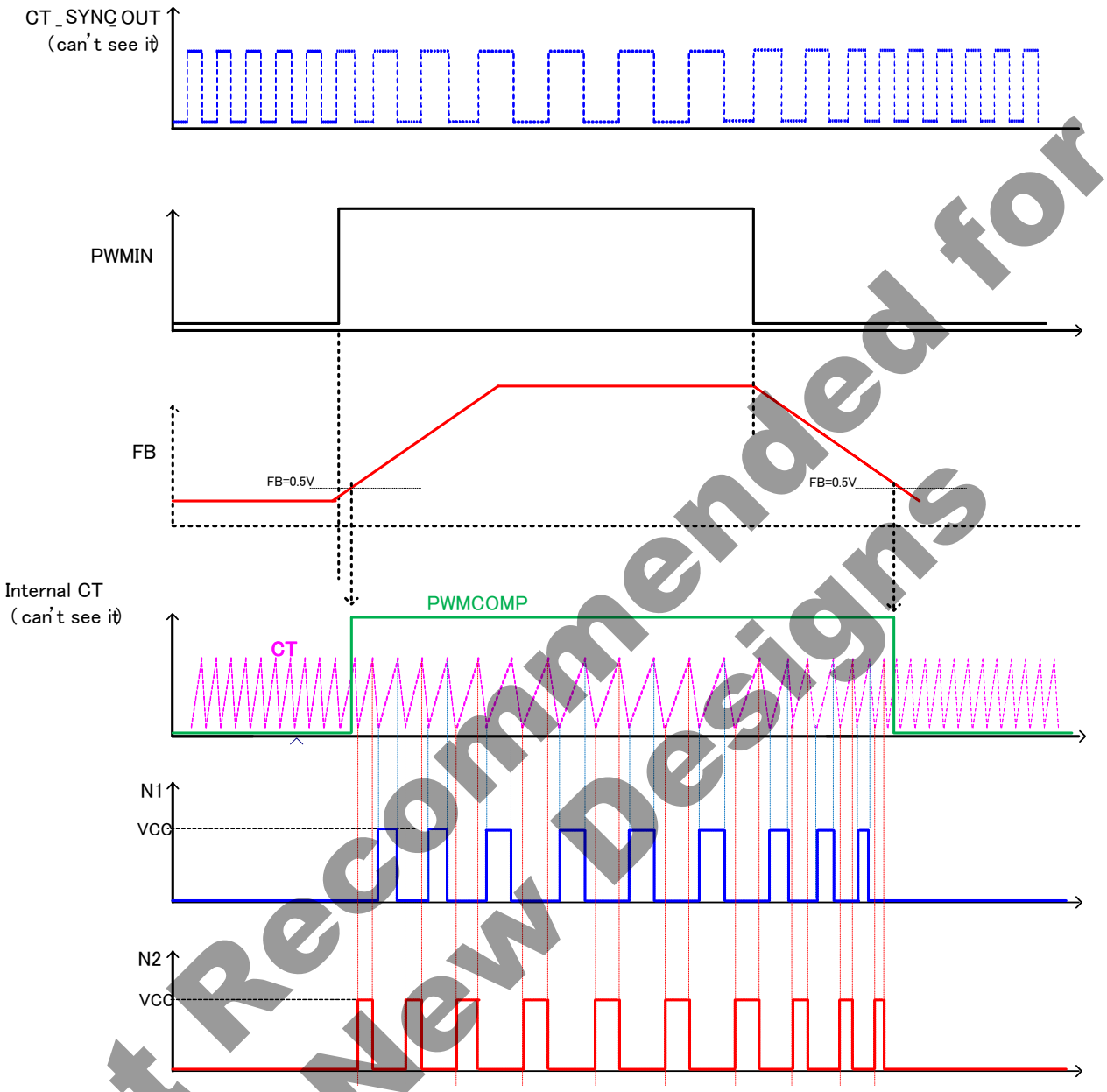


Figure. 26 Output Timing Chart

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes – continued

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

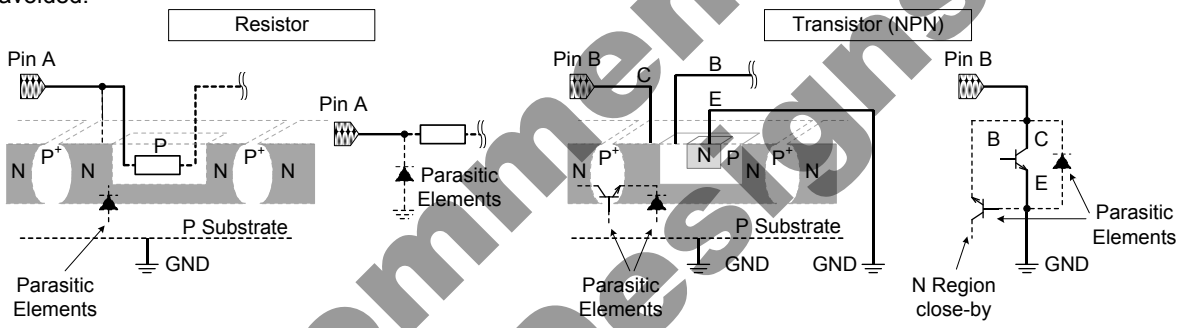


Figure xx. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

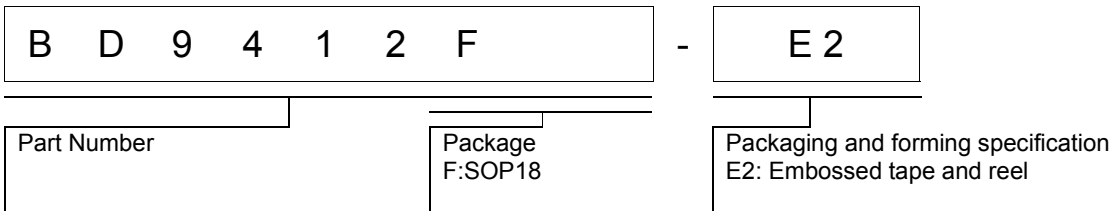
14. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

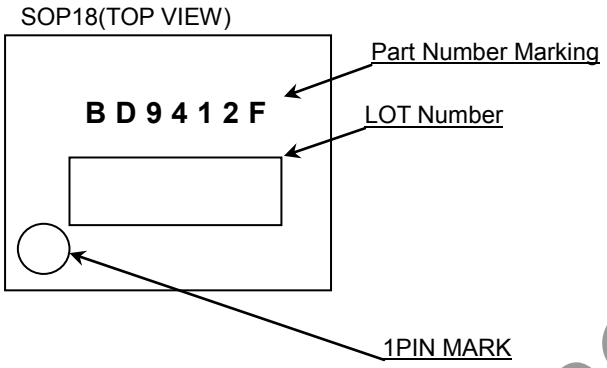
15. Over Current Protection Circuit (OCP)

This IC incorporates an integrated over current protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

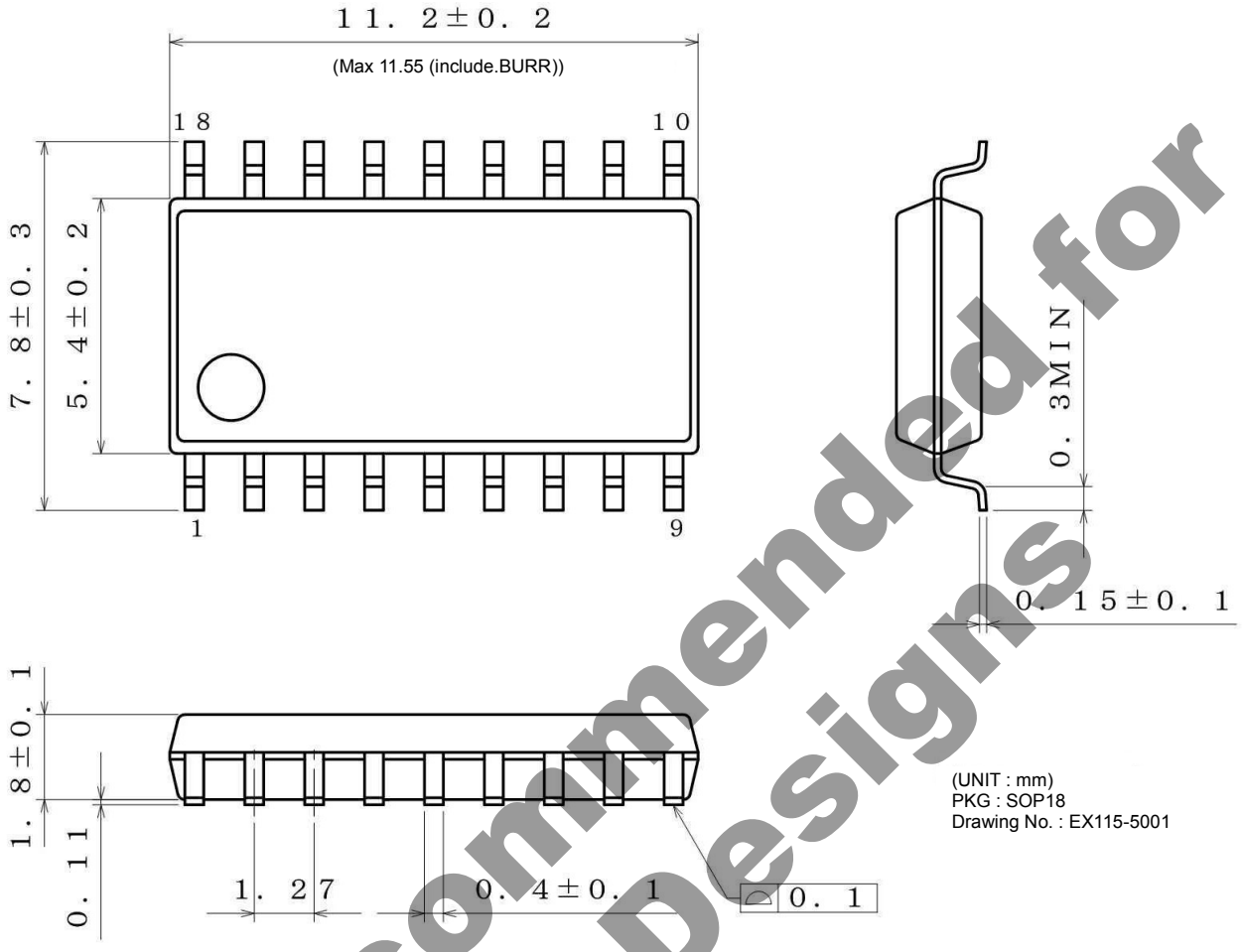


Marking Diagrams



Physical Dimension, Tape and Reel Information

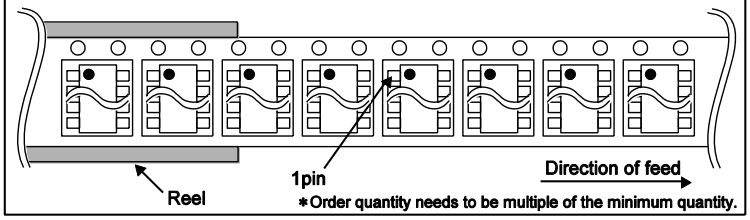
Package Name	SOP18



(UNIT : mm)
PKG : SOP18
Drawing No. : EX115-5001

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Revision No.	Date	Page	Changes
001	26.May.2015	All	New Release
002	12.Aug.2015	p.1	**General Description** LED Short Detection (IS Low Detection) and LED Open Detection (IS High Detection). ↓ LED Short Detection (IS High Detection) and LED Open Detection (IS Low Detection).

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
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2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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