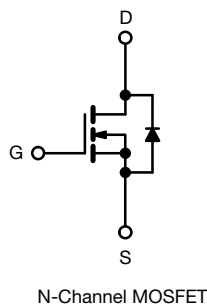
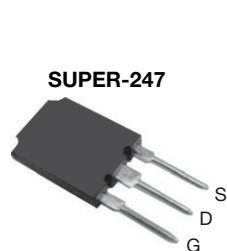


# Power MOSFET



## FEATURES

- Low figure-of-merit  $R_{on} \times Q_g$
- 100 % avalanche tested
- High peak current capability
- dv/dt ruggedness
- Improved  $t_{rr}/Q_{rr}$
- Improved gate charge
- High power dissipation capability
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



## PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	560	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.270
$Q_g$ max. (nC)	76	
$Q_{gs}$ (nC)	21	
$Q_{gd}$ (nC)	34	
Configuration	Single	

## ORDERING INFORMATION

Package	Super-247
Lead (Pb)-free	SiHS20N50C-E3

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	500	V
Gate-source voltage	$V_{GS}$	$\pm 30$	
Continuous drain current ( $T_J = 150\text{ }^\circ\text{C}$ ) <sup>a</sup>	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed drain current <sup>b</sup>	$I_{DM}$	80	
Linear derating factor		1.8	W/ $^\circ\text{C}$
Single pulse avalanche energy <sup>c</sup>	$E_{AS}$	361	mJ
Maximum power dissipation	$P_D$	250	W
Reverse diode dv/dt <sup>d</sup>	dv/dt	5	V/ns
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Soldering recommendations (peak temperature) <sup>d</sup>	For 10 s	300	


### Notes

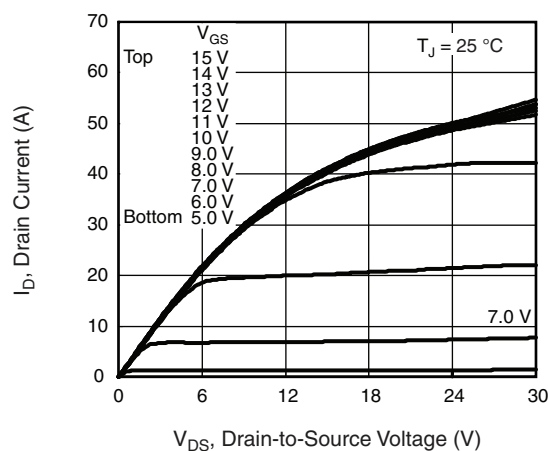
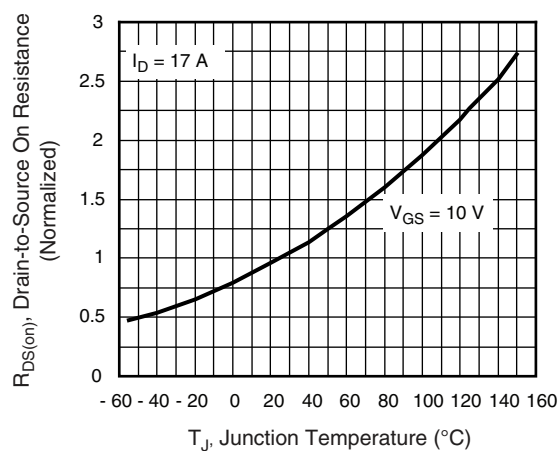
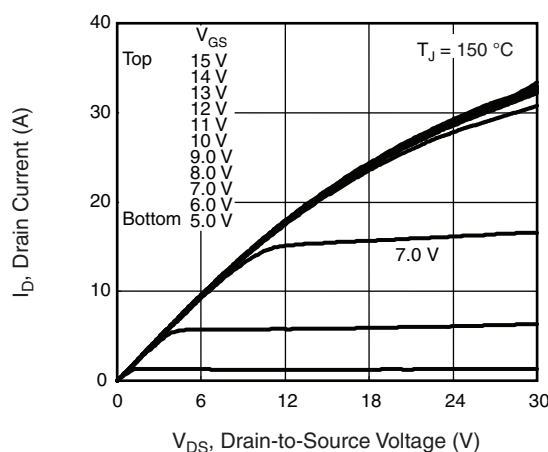
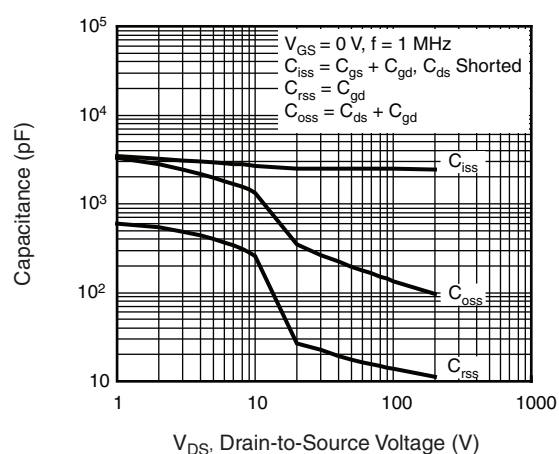
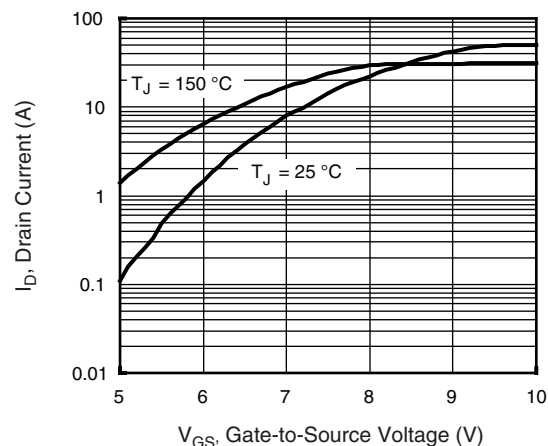
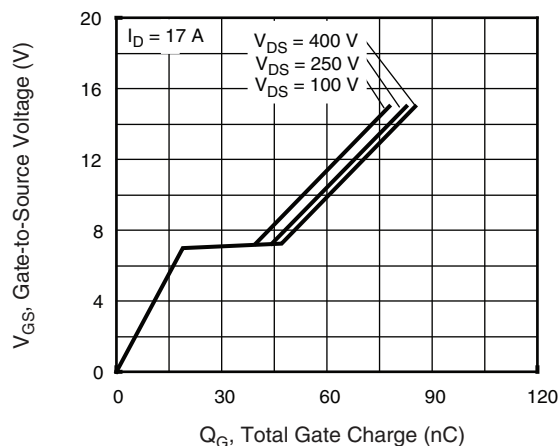
- Limited by maximum junction temperature
- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 2.5\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 17\text{ A}$
- $I_{SD} \leq 18\text{ A}$ ,  $di/dt \leq 380\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case

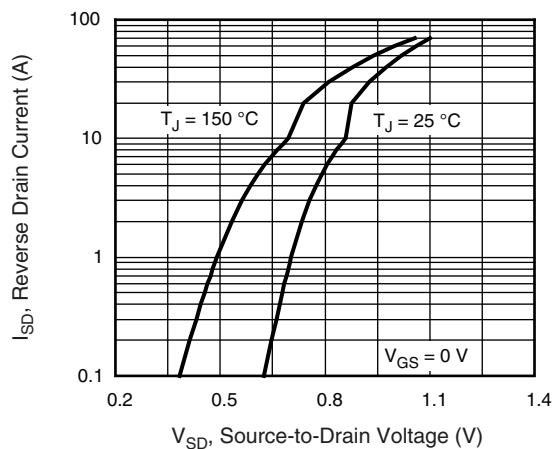
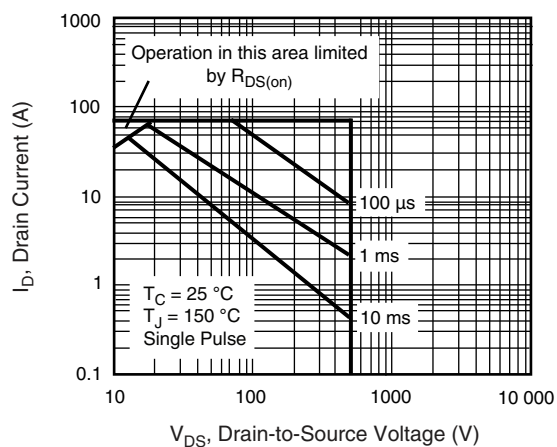
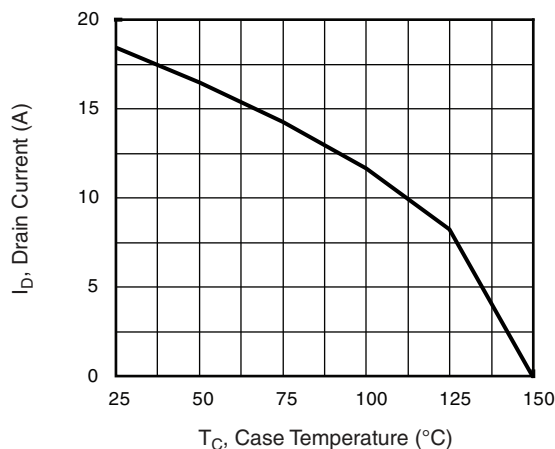
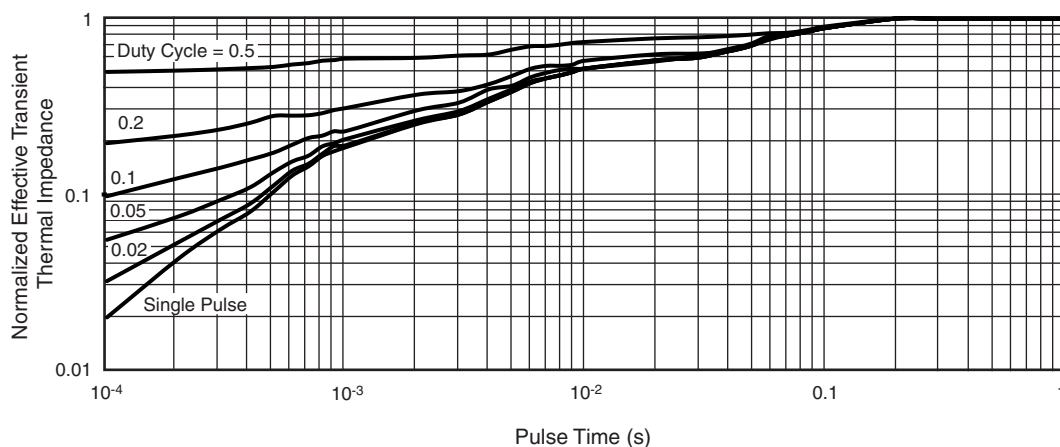
## THERMAL RESISTANCE RATINGS

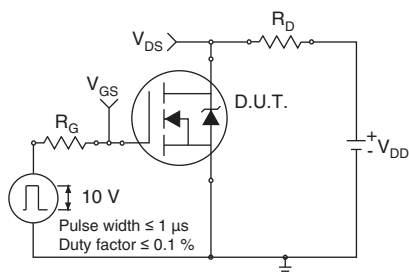
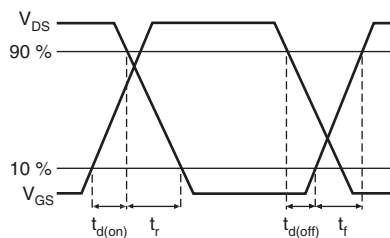
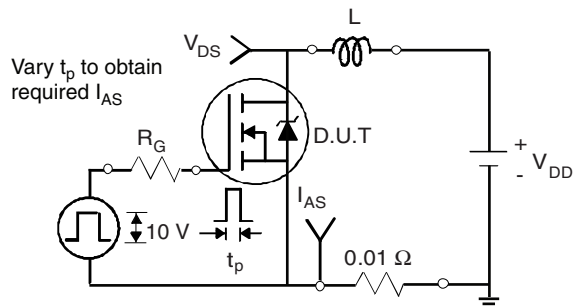
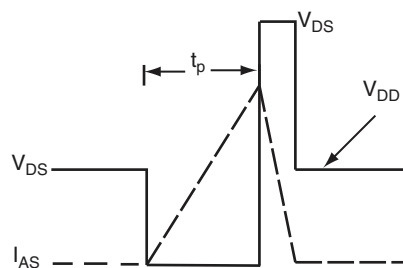
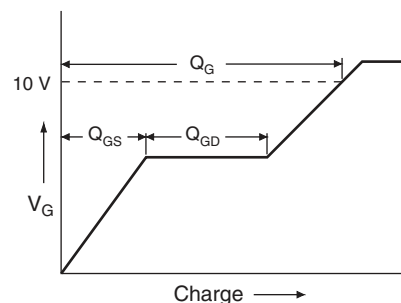
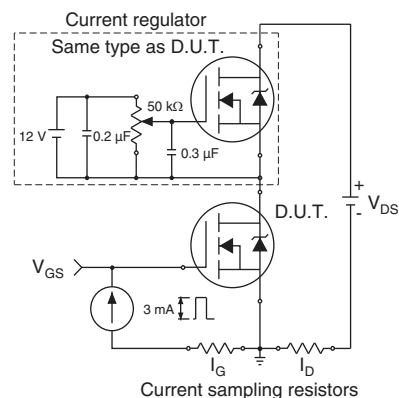
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	40	$^\circ\text{C}/\text{W}$
Maximum junction-to-case (drain)	$R_{thJC}$	-	0.5	



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX. UNIT	
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		500	-	- V	
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.7	- V/°C	
Gate-source threshold voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		3.0	-	5.0 V	
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 30 V		-	-	± 100 nA	
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V		-	-	25 μA	
		V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	250 μA	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 10 A	-	0.225	0.270 Ω	
Forward transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 10 A		-	6.4	- S	
Dynamic							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz		-	2451	2942	pF
Output capacitance	C <sub>oss</sub>			-	300	360	
Reverse transfer capacitance	C <sub>rss</sub>			-	26	32	
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 18 A, V <sub>DS</sub> = 400 V	-	65	76	nC
Gate-source charge	Q <sub>gs</sub>			-	21	-	
Gate-drain charge	Q <sub>gd</sub>			-	29	-	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 18 A, R <sub>g</sub> = 9.1 Ω		-	80	-	ns
Rise time	t <sub>r</sub>			-	27	-	
Turn-off delay time	t <sub>d(off)</sub>			-	32	-	
Fall time	t <sub>f</sub>			-	44	-	
Gate input resistance	R <sub>g</sub>	f = 1 MHz, open drain		-	1.1	-	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	20	A
Pulsed diode forward current	I <sub>SM</sub>			-	-	80	
Diode forward voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 18 A, V <sub>GS</sub> = 0 V		-	-	1.5	V
Reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> , di/dt = 100 A/μs, V <sub>R</sub> = 35 V		-	503	-	ns
Reverse recovery charge	Q <sub>rr</sub>			-	6.7	-	μC
Reverse recovery current	I <sub>RRM</sub>			-	30	-	A

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics,  $T_C = 25^\circ\text{C}$** 

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 2 - Typical Output Characteristics,  $T_C = 150^\circ\text{C}$** 

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

**Fig. 8 - Maximum Safe Operating Area**

**Fig. 9 - Maximum Drain Current vs. Case Temperature**

**Fig. 10 - Normalized Thermal Transient Impedance, Junction-to-Case (Super-247)**


**Fig. 11 - Switching Time Test Circuit**

**Fig. 12 - Switching Time Waveforms**

**Fig. 13 - Unclamped Inductive Test Circuit**

**Fig. 14 - Unclamped Inductive Waveforms**

**Fig. 15 - Basic Gate Charge Waveform**

**Fig. 16 - Gate Charge Test Circuit**


**Note**

a.  $V_{GS} = 5\text{ V}$  for logic level devices

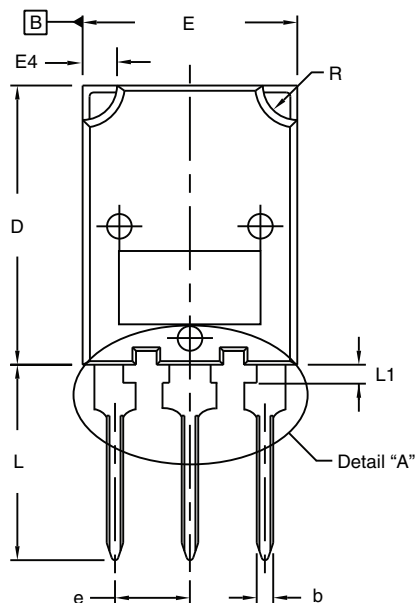
**Fig. 17 - For N-Channel**

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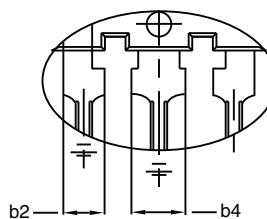
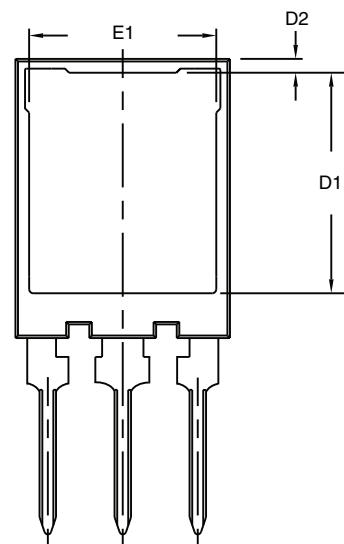
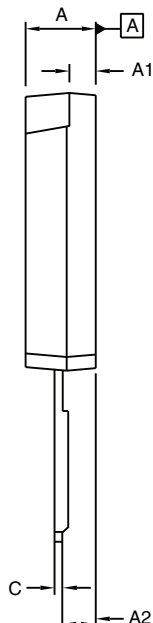
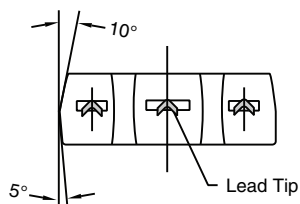


## TO-274AA (High Voltage)

### VERSION 1: FACILITY CODE = Y



⌀ 0.10 (0.25) ⌀ B A ⌀



Detail "A"  
Scale: 2:1

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.70	5.30	0.185	0.209
A1	1.50	2.50	0.059	0.098
A2	2.25	2.65	0.089	0.104
b	1.30	1.60	0.051	0.063
b2	1.80	2.20	0.071	0.087
b4	3.00	3.25	0.118	0.128
c <sup>(1)</sup>	0.38	0.89	0.015	0.035
D	19.80	20.80	0.780	0.819

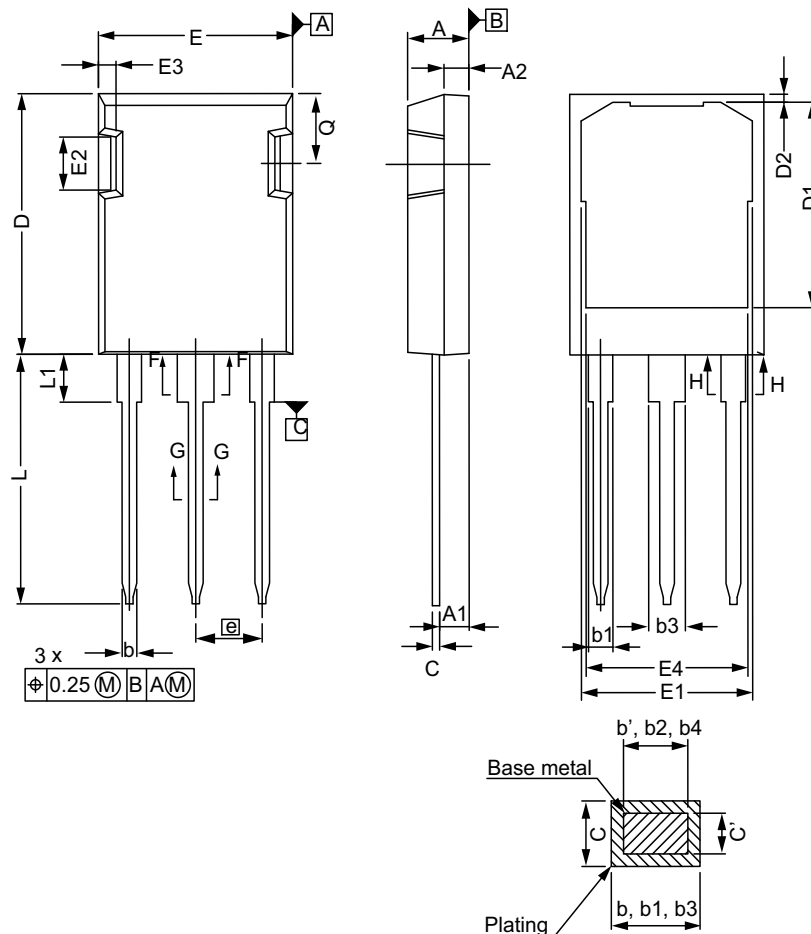
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	15.50	16.10	0.610	0.634
D2	0.70	1.30	0.028	0.051
E	15.10	16.10	0.594	0.634
E1	13.30	13.90	0.524	0.547
e	5.45 BSC		0.215 BSC	
L	13.70	14.70	0.539	0.579
L1	1.00	1.60	0.039	0.063
R	2.00	3.00	0.079	0.118

#### Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outer extremes of the plastic body
- Outline conforms to JEDEC® outline to TO-274AA
- (1) Dimension measured at tip of lead



## VERSION 2: FACILITY CODE = N



SECTION "F-F", "G-G" AND "H-H"  
SCALE: NONE

MILLIMETERS		
DIM.	MIN.	MAX.
A	4.83	5.21
A1	2.29	2.54
A2	1.91	2.16
b'	1.07	1.28
b	1.07	1.33
b1	1.91	2.41
b2	1.91	2.16
b3	2.87	3.38
b4	2.87	3.13
c'	0.55	0.65
c	0.55	0.68
D	20.80	21.10

MILLIMETERS		
DIM.	MIN.	MAX.
D1	16.25	17.65
D2	0.50	0.80
E	15.75	16.13
E1	13.10	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
e	5.44 BSC	
N	3	
L	19.81	20.32
L1	3.70	4.00
Q	5.49	6.00

ECN: E20-0538-Rev. C, 19-Oct-2020  
DWG: 5975

### Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Outline conforms to JEDEC® outline to TO-274AD
- Dimensions are measured in mm, angles are in degree
- Metal surfaces are tin plated, except area of cut





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