QLx4300-S45

Quad Lane Extender

FN6982
Rev 1.00
November 19, 2009

The QLx4300-S45 is a settable quad receive-side equalizer with extended functionality for advanced protocols operating with line rates up to 3.125Gb/s such as InfiniBand (SDR) and 10GBase-CX4. The QLx4300-S45 compensates for the frequency dependent attenuation of copper twin-axial cables, extending the signal reach up to 40m on 24AWG cable.

The small form factor, highly-integrated quad design is ideal for high-density data transmission applications including active copper cable assemblies. The four equalizing filters within the QLx4300-S45 can each be set to one of 32 compensation levels, providing optimal signal fidelity for a given media and length. The compensation level for each filter can be set by either (a) three external control pins or (b) a serial bus interface. When the external control pins are used, 18 of the 32 boost levels are available for each channel. If the serial bus is used, all 32 compensation levels are available.

Operating on a single 1.2V power supply, the QLx4300-S45 enables per channel throughputs of up to 3.125Gb/s while supporting the lower data rates of 2.5Gb/s and 1.5Gb/s. The QLx4300-S45 uses current mode logic (CML) inputs/outputs and is packaged in a 4mmx7mm 46 lead QFN. Individual lane impedance select support is included for module applications.

Features

- Supports data rates up to 3.125Gb/s
- Low power (78mW per channel)
- Low latency (<500ps)
- Four equalizers in a 4mmx7mm QFN package for straight route-through architecture and simplified routing
- Each equalizer boost is independently pin selectable and programmable
- Beacon signal support and line silence preservation
- 1.2V supply voltage
- Individual channel power-down (impedance select)

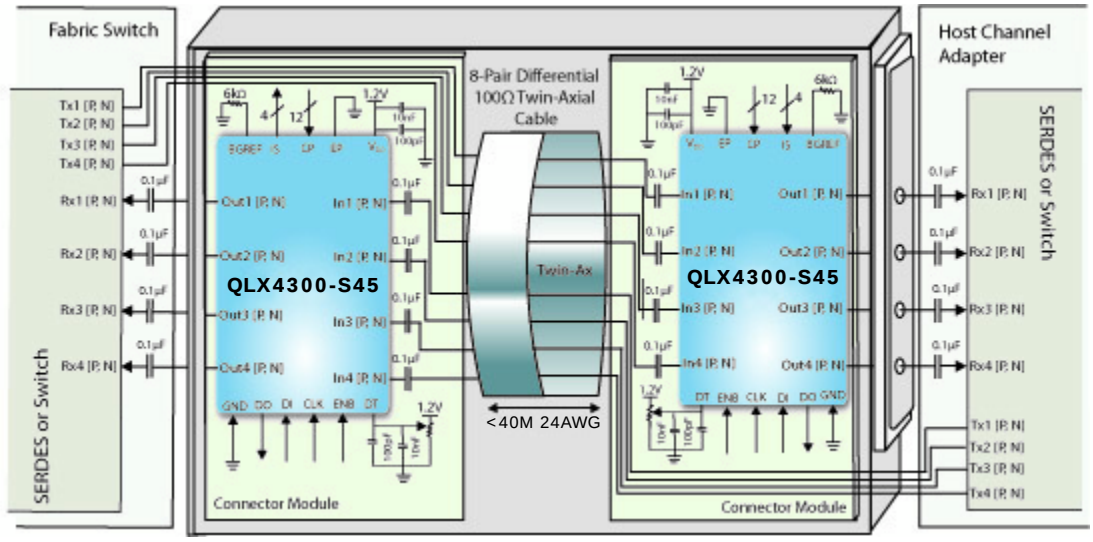
Applications

- InfiniBand (SDR)
- 10GBase-CX4
- PCI Express (Gen 1)
- DisplayPort
- XAUI
- SAS (1.0)
- High-speed active cable assemblies
- High-speed printed circuit board (PCB) traces

Benefits

- Thinner gauge cable
- Extends cable reach greater than 3x
- Improved BER

Typical Application Circuit



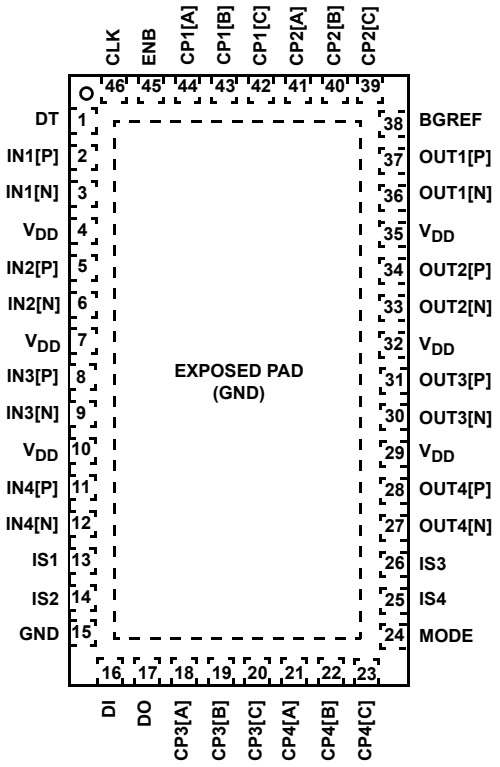
Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
QLX4300SIQT7	QLX4300SIQ	0 to +70	46 Ld QFN 7” Prod. Tape & Reel; Qty 1,000	L46.4x7
QLX4300SIQSR	QLX4300SIQ	0 to +70	46 Ld QFN 7” Sample Reel; Qty 100	L46.4x7

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Configuration

QLx4300-S45
(46 LD 4x7 QFN)
TOP VIEW



Pin Descrptions

PIN NAME	PIN NUMBER	DESCRIPTION
DT	1	Detection Threshold. Reference DC current threshold for input signal power detection. Data output OUT[k] is muted when the power of the equalized version of IN[k] falls below the threshold. Tie to ground to disable electrical idle preservation and always enable the limiting amplifier.
IN1[P,N]	2, 3	Equalizer 1 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
V_{DD}	4, 7, 10, 29, 32, 35	Power supply. 1.2V supply voltage. The use of parallel 100pF and 10nF decoupling capacitors to ground is recommended for each of these pins for broad high-frequency noise suppression.
IN2[P,N]	5, 6	Equalizer 2 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
IN3[P,N]	8, 9	Equalizer 3 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
IN4[P,N]	11, 12	Equalizer 4 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
IS1	13	Impedance Select 1. CMOS logic input. When the voltage on this pin is LOW, the single-ended input impedance of In1P and In1N each go above 200kΩ and powers down the channel. This pin should be connected to the Fundamental Reset signal in PCI Express™. Otherwise, connect to V_{DD} to hold the input impedance at 50Ω.
IS2	14	Impedance Select 2. CMOS logic input. When the voltage on this pin is LOW, the single-ended input impedance of In2P and In2N each go above 200kΩ and powers down the channel. This pin should be connected to the Fundamental Reset signal in PCI Express™. Otherwise, connect to V_{DD} to hold the input impedance at 50Ω.
GND	15	Ground
DI	16	Serial data input, CMOS logic. Input for serial data stream to program internal registers controlling the boost for all four equalizers. Synchronized with clock (CLK) on pin 46. Overrides the boost setting established on CP control pins. Internally pulled down.
DO	17	Serial data output, CMOS logic. Output of the internal registers controlling the boost for all four equalizers. Synchronized with clock on pin 46. Equivalent to serial data input on DI but delayed by 21 clock cycles.
CP3[A,B,C]	18, 19, 20	Control pins for setting equalizer 3. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and C is the LSB. Pins are internally pulled down through a 25kΩ resistor.
CP4[A,B,C]	21, 22, 23	Control pins for setting equalizer 4. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and C is the LSB. Pins are internally pulled down through a 25kΩ resistor.
MODE	24	Boost-level control mode input, CMOS logic. Allows serial programming of internal registers through pins DI, ENB, and Clk when set HIGH. Resets all internal registers to zero and uses boost levels set by CP pins when set LOW. If serial programming is not used, this pin should be grounded.
IS4	25	Impedance Select 4. CMOS logic input. When the voltage on this pin is LOW, the single-ended input impedance of In4P and In4N each go above 200kΩ and powers down the channel. This pin should be connected to the Fundamental Reset signal in PCI Express™. Otherwise, connect to V_{DD} to hold the input impedance at 50Ω.
IS3	26	Impedance Select 3. CMOS logic input. When the voltage on this pin is LOW, the single-ended input impedance of In3P and In3N each go above 200kΩ and powers down the channel. This pin should be connected to the Fundamental Reset signal in PCI Express™. Otherwise, connect to V_{DD} to hold the input impedance at 50Ω.
OUT4[N,P]	27, 28	Equalizer 4 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
OUT3[N,P]	30, 31	Equalizer 3 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.

Pin Descrptions (Continued)

PIN NAME	PIN NUMBER	DESCRIPTION
OUT2[N,P]	33, 34	Equalizer 2 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
OUT1[N,P]	36, 37	Equalizer 1 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 4GHz frequency response is recommended.
BGREF	38	External bandgap reference resistor. Recommended value of 6.04kΩ ±1%.
CP2[C,B,A]	39, 40, 41	Control pins for setting equalizer 2. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and C is the LSB. Pins are internally pulled down through a 25kΩ resistor.
CP1[C,B,A]	42, 43, 44	Control pins for setting equalizer 1. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and C is the LSB. Pins are internally pulled down through a 25kΩ resistor.
ENB	45	Serial data enable (active low), CMOS logic. Internal registers can be programmed with DI and CLK pins only when the ENB pin is ‘LOW’. Internally pulled down.
CLK	46	Serial data clock, CMOS logic. Synchronous clock for serial data on DI and DO pins. Data on DI is latched on the rising clock edge. Clock speed is recommended to be between 10MHz and 20MHz. Internally pulled down.
EXPOSED PAD	-	Exposed ground pad. For proper electrical and thermal performance, this pad should be connected to the PCB ground plane.

Absolute Maximum Ratings

Supply Voltage (V_{DD} to GND) . . . . . -0.3V to 1.3V
Voltage at All Input Pins . . . . . -0.3V to V_{DD} + 0.3V
ESD Rating at All Pins . . . . . 2kV (HBM)

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{Jc} (°C/W)
46 Ld QFN Package (Note 1)	32	2.3

Operating Ambient Temperature Range. . . . . 0°C to +70°C
Storage Ambient Temperature Range . . . . . -55°C to +150°C
Maximum Junction Temperature. . . . . +125°C
Pb-Free Reflow Profile. . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Operating Conditions

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		1.1	1.2	1.3	V
Operating Ambient Temperature	T_A		0	25	70	°C
Bit Rate		NRZ data applied to any channel	1.5		3.125	Gb/s

Control Pin Characteristics

Typical values are at V_{DD} = 1.2V, T_A = +25°C, and V_{IN} = 800mV_{P-P}, unless otherwise noted. V_{DD} = 1.1V to 1.3V, T_A = 0°C to +70°C.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Input ‘LOW’ Logic Level	V_{IL}	DI, Clk, ENB	0	0	350	mV	
Input ‘HIGH’ Logic Level	V_{IH}	DI, Clk, ENB	750		V_{DD}	mV	
Output ‘LOW’ Logic Level	V_{OL}	IS[k], DO	0	0	250	mV	
Output ‘HIGH’ Logic Level	V_{OH}	IS[k], DO	1000		V_{DD}	mV	
‘LOW’ Resistance State		CP[k][A,B,C]	0		1	kΩ	2
‘MID’ Resistance State		CP[k][B,C]	22.5	25	27.5	kΩ	2
‘HIGH’ Resistance State		CP[k][A,B,C]	500		∞	kΩ	2
Input Current		Current draw on digital pin, i.e., CP[k][A,B,C], DI, Clk, ENB		30	100	µA	

NOTE:

2. If four CP pins are tied together, the resistance values in this table should be divided by four.

Electrical Specifications

Typical values are at V_{DD} = 1.2V, T_A = +25°C, and V_{IN} = 800mV_{P-P}, unless otherwise noted. V_{DD} = 1.1V to 1.3V, T_A = 0°C to +70°C.

PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}			260		mA	
Cable Input Amplitude Range	V_{IN}	Measured differentially at data source before encountering channel loss	800	1200	1600	mV_{P-P}	3
DC Differential Input Resistance		Measured on input channel IN[k]	80	100	120	Ω	
DC Single-Ended Input Resistance		Measured on input channel IN[k]P or IN[k]N	40	50	60	Ω	
Input Return Loss (Differential)	$S_{DD}11$	50MHz to 3.75GHz	10			dB	4
Input Return Loss (Common Mode)	$S_{CC}11$	50MHz to 3.75GHz	6			dB	4

Electrical Specifications Typical values are at V_{DD} = 1.2V, T_A = +25°C, and V_{IN} = 800mV_{P-P}, unless otherwise noted. V_{DD} = 1.1V to 1.3V, T_A = 0°C to +70°C. **(Continued)**

PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Input Return Loss (Com. to Diff. Conversion)	$S_{DC}11$	50MHz to 3.75GHz	20			dB	4
Output Amplitude Range	V_{OUT}	Active data transmission mode; Measured differentially at OUT[k]P and OUT[k]N with 50Ω load on both output pins	450	550	650	mV_{P-P}	
		Line Silence mode; Measured differentially at OUT[k]P and OUT[k]N with 50Ω load on both output pins		10	20	mV_{P-P}	
Differential Output Impedance		Measured on OUT[k]	80	105	120	Ω	
Output Return Loss (Differential)	$S_{DD}22$	50MHz to 3.75GHz	10			dB	4
Output Return Loss (Common Mode)	$S_{CC}22$	50MHz to 3.75GHz	5			dB	4
Output Return Loss (Com. to Diff. Conversion)	$S_{DC}22$	50MHz to 3.75GHz	20			dB	4
Output Residual Jitter		3.125Gb/s; Up to 20m 24AWG standard twin-axial cable (approx. -25dB @ 2.5GHz); 800m$V_{P-P} \le V_{IN} \le$ 1600mV_{P-P}		0.15	0.25	UI	3, 5, 6
Output Transition Time	t_r, t_f	20% to 80%	30	60	80	ps	7
Lane-to-Lane Skew					50	ps	
Propagation Delay		From IN[k] to OUT[k]			500	ps	
Data-to-Line Silence Response Time	t_{DS}	Time to transition from active data to line silence (muted output) on 20m 24AWG standard twin-axial cable at 3.125Gb/s			15	ns	8, 11
		Time from last bit of ALIGN(0) for SAS OOB signaling to line silence (<20mV_{P-P} output); Meritec 24AWG 20m; 3.125Gb/s			14	ns	12
Line Silence-to-Data Response Time	t_{SD}	Time to transition from line silence mode (muted output) to active data on 20m 24AWG standard twin-axial cable at 3.125Gb/s			20	ns	8, 11
		Time from first bit of ALIGN(0) for SAS OOB signaling to 450mV_{P-P} output; Meritec 24AWG 20m; 3.125Gb/s			19	ns	12
Timing Difference (SAS)	$\lvert t_{DS} - t_{SD} \rvert$	For SAS OOB signaling support; Meritec 24AWG 20m			5	ns	12

NOTES:

3. After channel loss, differential amplitudes at QLx4300-S45 inputs must meet the input voltage range specified in “Absolute Maximum Ratings” on page 5.
4. Temperature = +25°C, V_{DD} = 1.2V.
5. Output residual jitter is the difference between the total jitter at the lane extender output and the total jitter of the transmitted signal (as measured at the input to the channel). Total jitter (TJ) is DJ_{PP} + 14.1 x RJ_{RMS}.
6. Measured using a PRBS 2^7-1 pattern. Deterministic jitter at the input to the lane extender is due to frequency-dependent, media-induced loss only.
7. Rise and fall times measured using a 1GHz clock with a 20ps edge rate.
8. For active data mode, cable input amplitude is 400mV_{P-P} (differential) or greater. For line silence mode, cable input amplitude is 20mV_{P-P} (differential) or less.
9. Measured differentially across the data source.

NOTES: (Continued)

10. During line silence, transmitter noise in excess of this voltage range may result in differential output amplitudes from the QLx4300-S45 that are greater than $20mV_{P-P}$.
11. The data pattern preceding line silence mode is comprised of the PCIe electrical idle ordered set (EIOS). The data pattern following line silence mode is comprised of the PCIe electrical idle exit sequence (EIES).
12. The data pattern preceding or following line silence mode is comprised of the SAS-2 ALIGN (0) sequence for OOB signaling at 3.125Gb/s, and amplitude of $800mV_{P-P}$.

Serial Bus Timing Characteristics

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
CLK Setup Time	t_{SCK}	From the falling edge of ENB	10			ns
DI Setup Time	t_{SDI}	Prior to the rising edge of CLK	10			ns
DI Hold Time	t_{HDI}	From the rising edge of CLK	6			ns
ENB 'HIGH'	t_{HEN}	From the falling edge of the last data bit's CLK	10			ns
Boost Setting Operational	t_D	From ENB 'HIGH'			10	ns
DO Hold Time	t_{CQ}	From the rising edge of CLK to DO transition	12			ns
Clock Rate	f_{CLK}	Reference clock for serial bus EQ programming			20	MHz

Typical Performance Characteristics

V_{DD} = 1.2V, T_A = +25°C, unless otherwise noted. Performance was characterized using the system testbed shown in Figure 1. Unless otherwise noted, the transmitter generated a non-return-to-zero (NRZ) PRBS-7 sequence at $800mV_{P-P}$ (differential) with 10ps of peak-to-peak deterministic jitter. This transmit signal was launched into twin-axial cable test channels of varying gauges and lengths. The loss characteristics of these test channels are plotted as a function of frequency in Figure 2. The received signal at the output of these test channels was then processed by the QLx4300-S45 before being passed to a receiver. Eye diagram measurements were made with 4000 waveform acquisitions and include random jitter.

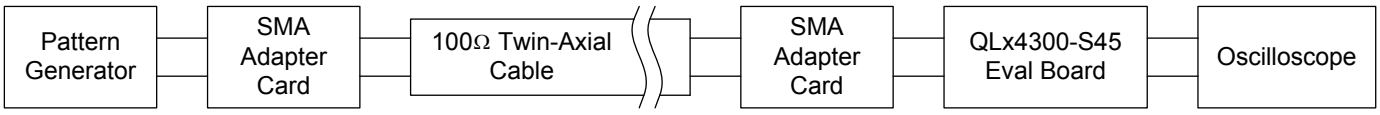


FIGURE 1. DEVICE CHARACTERIZATION TEST SETUP

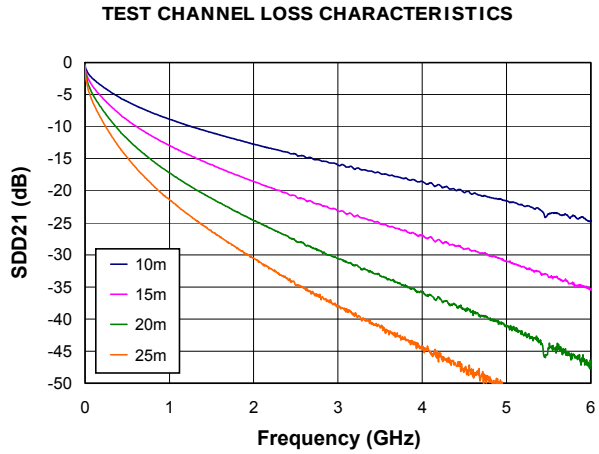


FIGURE 2. 26 AWG TWIN-AXIAL CABLE LOSS AS A FUNCTION OF FREQUENCY FOR VARIOUS TEST CHANNELS

Typical Performance Characteristics (Continued)

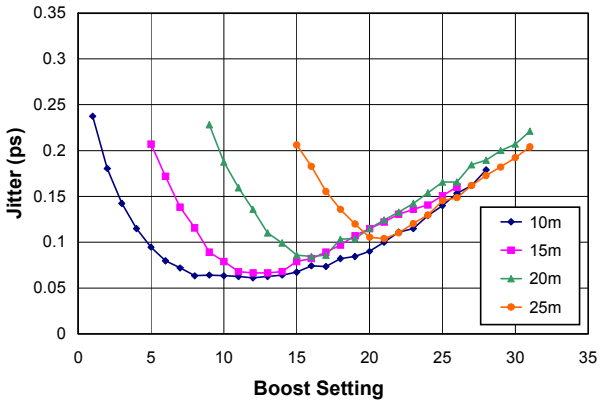


FIGURE 2. JITTER VS BOOST SETTING FOR VARIOUS CABLE LENGTHS, PRBS-7, 0.03PS SYSTEM JITTER INCLUDED

OUTPUT EYE DIAGRAMS

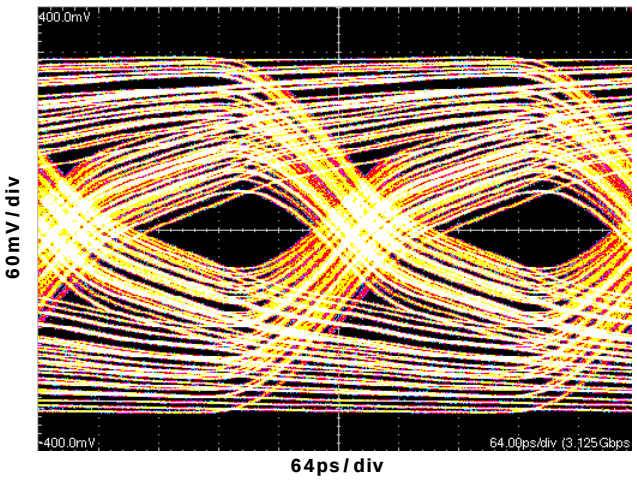


FIGURE 3. RECEIVED SIGNAL AFTER 10m OF 26AWG TWIN-AXIAL CABLE, 3.125Gb/s

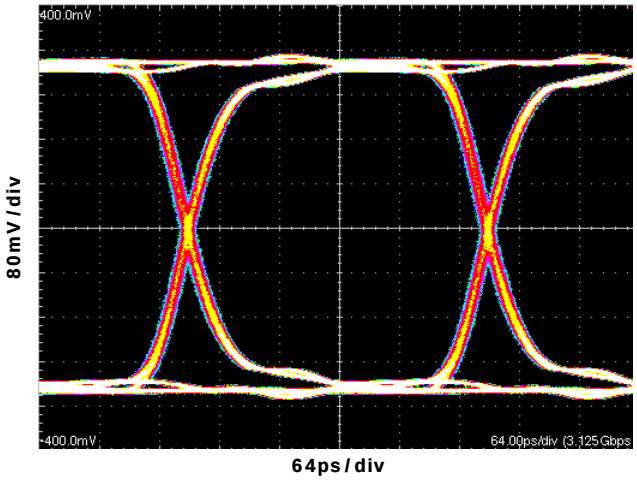


FIGURE 4. QLx4300-S45 OUTPUT AFTER 10m OF 26AWG TWIN-AXIAL CABLE, 3.125Gb/s

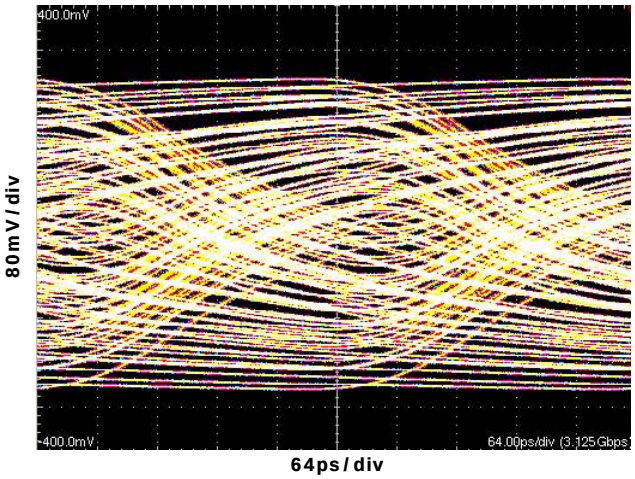


FIGURE 5. RECEIVED SIGNAL AFTER 15m OF 26AWG TWIN-AXIAL CABLE, 3.125Gb/s

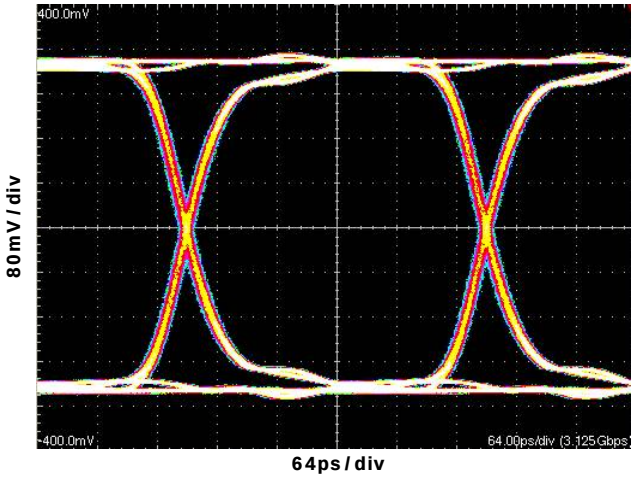


FIGURE 6. QLx4300-S45 OUTPUT AFTER 15m OF 26AWG TWIN-AXIAL CABLE, 3.125Gb/s

Typical Performance Characteristics (Continued)

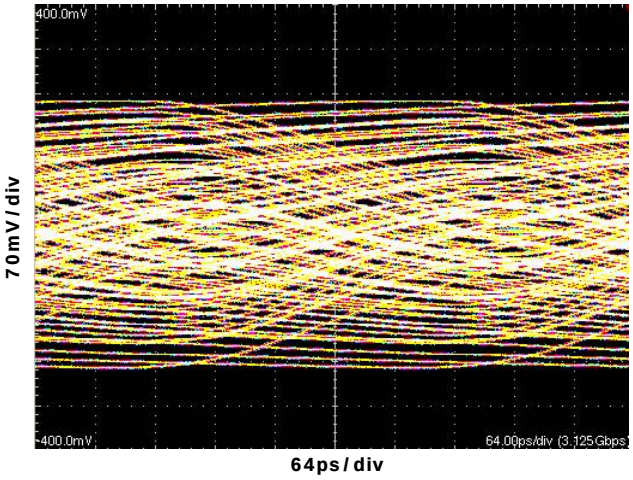


FIGURE 7. RECEIVED SIGNAL AFTER 20m OF 26AWG TWIN-AXIAL CABLE, 3.125Gb/s

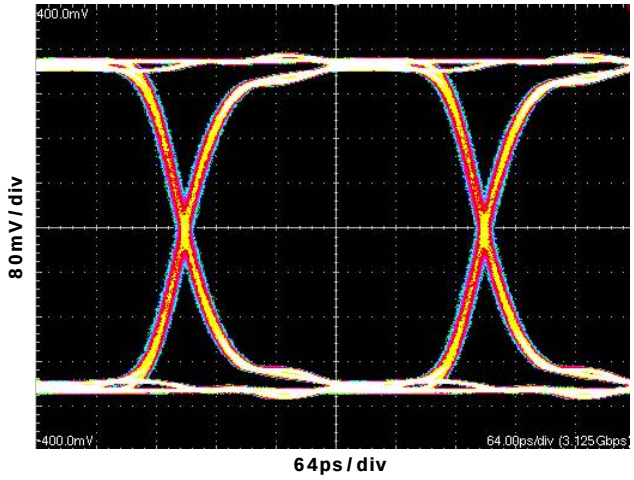


FIGURE 8. QLx4300-S45 OUTPUT AFTER 20m OF 26AWG TWIN-AXIAL CABLE, 3.125Gb/s

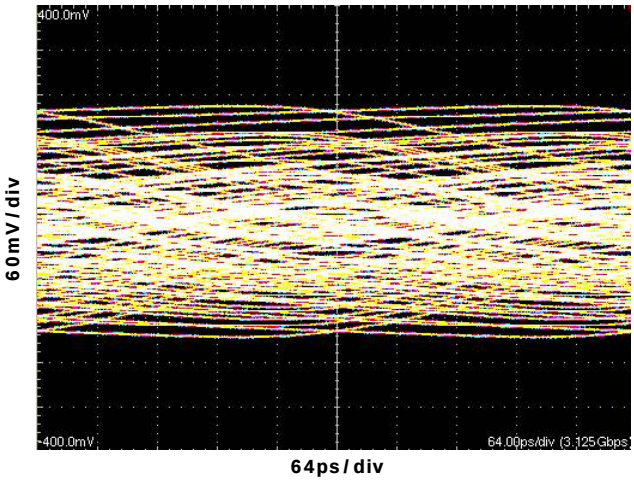


FIGURE 9. RECEIVED SIGNAL AFTER 25m OF 26AWG TWIN-AXIAL CABLE, 3.125Gb/s

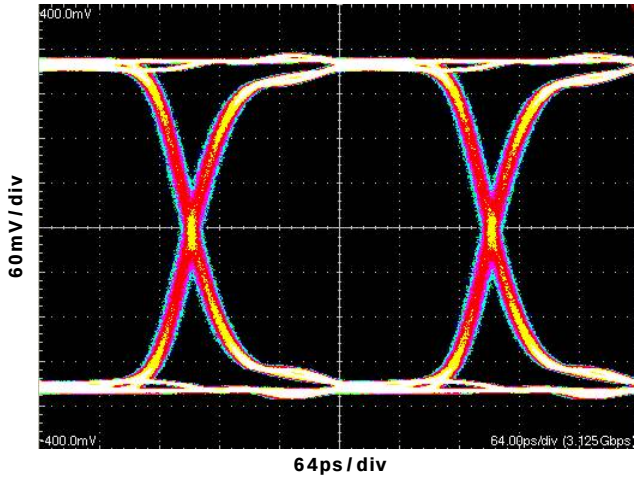


FIGURE 10. QLx4300-S45 OUTPUT AFTER 25m OF 26AWG TWIN-AXIAL CABLE, 3.125Gb/s

RETURN LOSS AND CROSSTALK CHARACTERISTICS

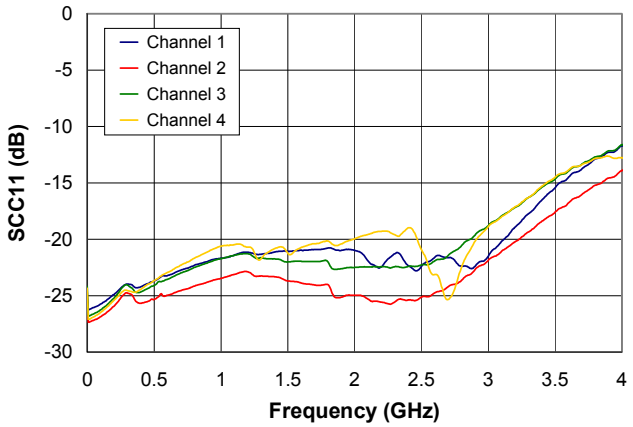


FIGURE 11. INPUT COMMON-MODE RETURN LOSS

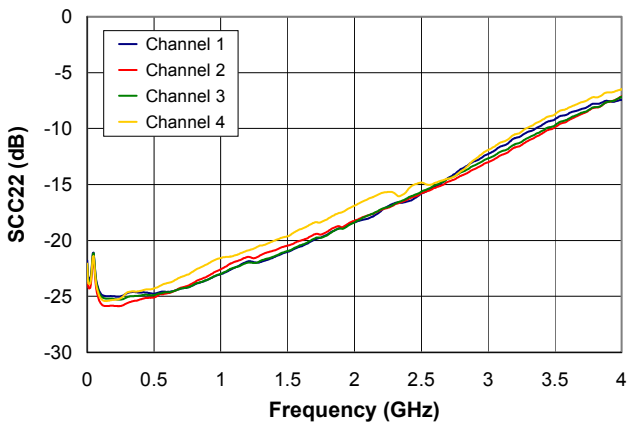


FIGURE 12. OUTPUT COMMON-MODE RETURN LOSS

Typical Performance Characteristics (Continued)

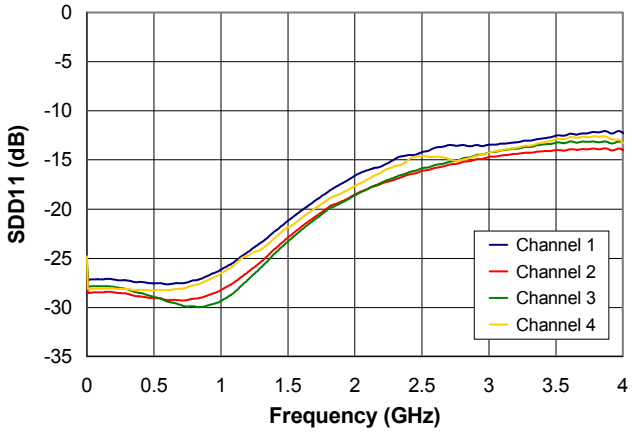


FIGURE 13. INPUT DIFFERENTIAL RETURN LOSS

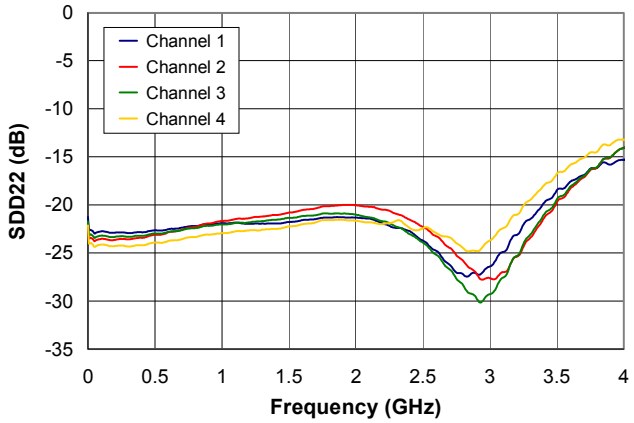


FIGURE 14. OUTPUT DIFFERENTIAL RETURN LOSS

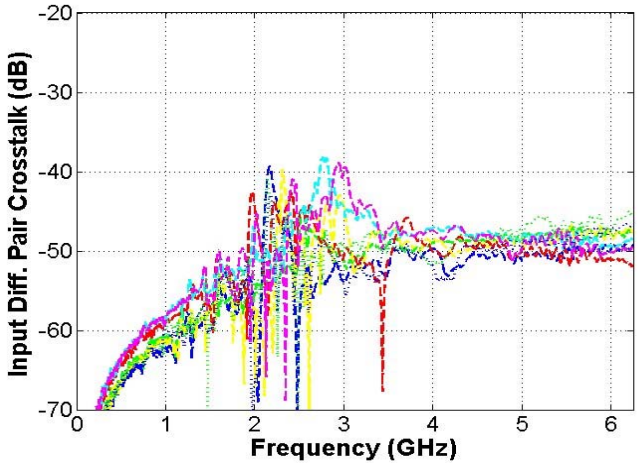


FIGURE 15. DIFFERENTIAL CROSSTALK BETWEEN ADJACENT INPUT CHANNEL

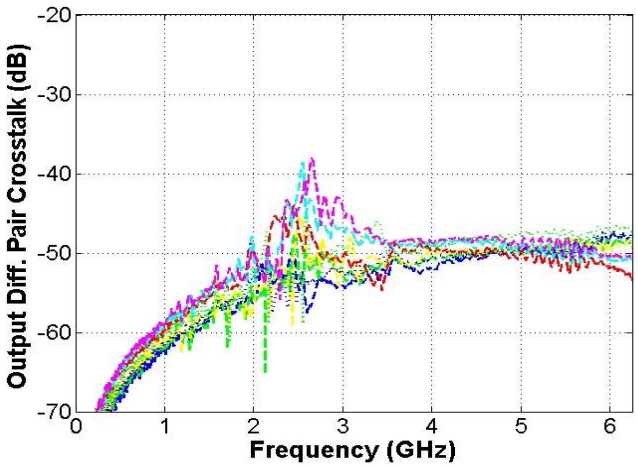


FIGURE 16. DIFFERENTIAL CROSSTALK BETWEEN ADJACENT INPUT CHANNELS

Operation

The QLx4300-S45 is an advanced quad lane-extender for high-speed interconnects. A functional diagram of one of the four channels in the QLx4300-S45 is shown in Figure 17. In addition to a robust equalization filter to compensate for channel loss and restore signal fidelity, the QLx4300-S45 contains unique integrated features to preserve special signaling protocols typically broken by other equalizers. The signal detect function is used to mute the channel output when the equalized signal falls below the level determined by the Detection Threshold (DT) pin voltage. This function is intended to preserve periods of line silence (“quiescent state” in InfiniBand contexts).

As illustrated in Figure 17, the core of each high-speed signal path in the QLx4300-S45 is a sophisticated equalizer followed by a limiting amplifier. The equalizer compensates for skin loss, dielectric loss, and impedance discontinuities in the transmission channel. Each equalizer is followed by a limiting amplification stage that provides a clean output signal with full amplitude swing and fast rise-fall times for reliable signal decoding in a subsequent receiver.

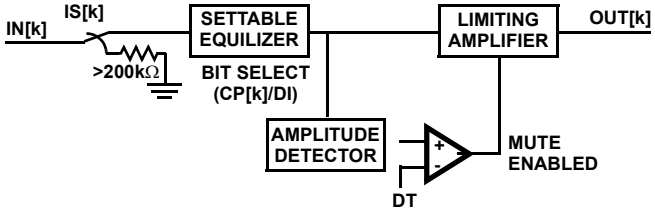


FIGURE 17. FUNCTIONAL DIAGRAM OF A SINGLE CHANNEL WITHIN THE QLx4300-S45

Individually Adjustable Equalization Boost

Each channel in the QLx4300-S45 features an independently settable equalizer for custom signal restoration. Each equalizer can be set to one of 32 levels of compensation when the serial bus is used to program

the boost level and one of 18 compensation levels when the CP[k] pins are used to set the level. The equalizer transfer functions for a subset of these compensation levels are plotted in Figure 18. The flexibility of this adjustable compensation architecture enables signal fidelity to be optimized on a channel-by-channel basis, providing support for a wide variety of channel characteristics and data rates ranging from 2.5Gb/s to 3.125Gb/s. Because the boost level is externally set rather than internally adapted, the QLx4300-S45 provides reliable communication from the very first bit transmitted. There is no time needed for adaptation and control loop convergence. Furthermore, there are no pathological data patterns that will cause the QLx4300-S45 to move to an incorrect boost level.

The “Applications Information” section beginning on page 12 details how to set the boost level by both the CP-pin voltage approach and the serial programming approach.

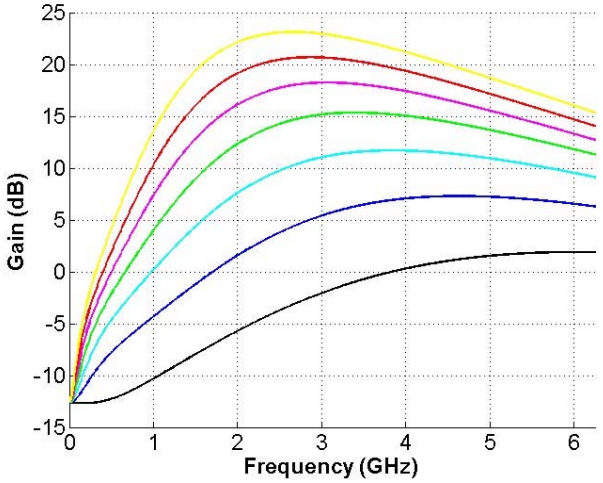


FIGURE 18. EQUALIZER TRANSFER FUNCTIONS FOR SETTINGS 0, 5, 10, 15, 20, 25, AND 31 IN THE QLx4300-S45

CML Input and Output Buffers

The input and output buffers for the high-speed data channels in the QLx4300-S45 are implemented using CML. Equivalent input and output circuits are shown in Figures 19 and 20, respectively.

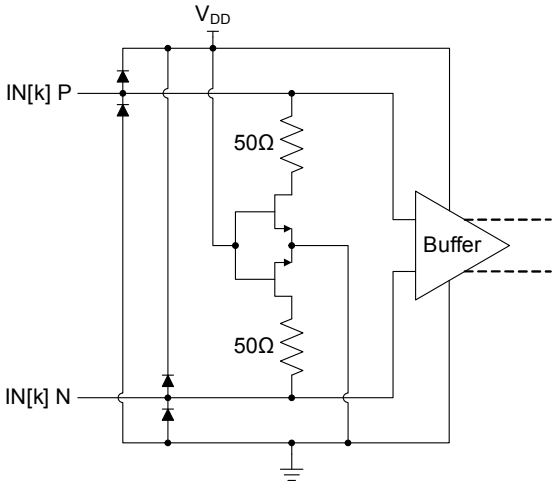


FIGURE 19. CML INPUT EQUIVALENT CIRCUIT FOR THE QLx4300-S45

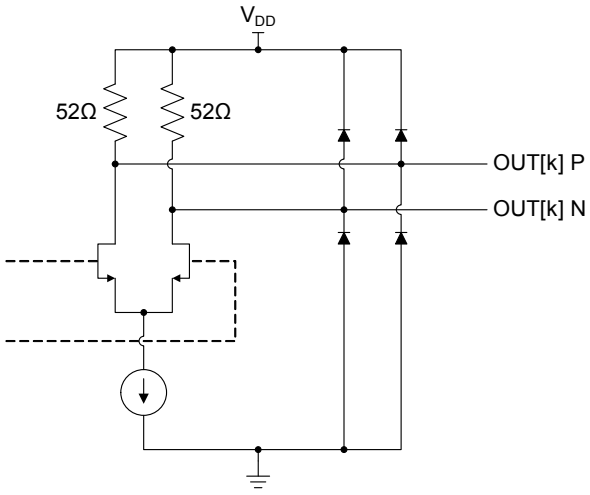


FIGURE 20. CML OUTPUT EQUIVALENT CIRCUIT FOR THE QLx4300-S45

NOTE: The load value of 52Ω is used to internally match SDD_{22} for a characteristic impedance of 50Ω.

Line Silence/Electrical Idle/Quiescent Mode

Line silence is commonly broken by the limiting amplification in other equalizers. This disruption can be detrimental in many systems that rely on line silence as part of the protocol. The QLx4300-S45 contains special lane management capabilities to detect and preserve periods of line silence while still providing the fidelity-enhancing benefits of limiting amplification during active data transmission. Line silence is detected by measuring the amplitude of the equalized signal and comparing that to a threshold set by the current at the DT pin. When the amplitude falls below the threshold, the output driver stages are muted and held at their nominal common mode voltage[1].

1. The output common mode voltage remains constant during both active data transmission and output muting modes.

Channel Power-Down

In addition to controlling the input impedance, the IS[k] pin powers down the equalizer channel when pulled low. This feature allows a system controller individually to power down unused channels and to minimize power consumption. Example: the signal to power down a channel could come from an Intelligent Platform Management controller in ATCA applications for E-Keying. The current draw for a channel is reduced from 50mA to 3.8mA when powered down.

Applications Information

Several aspects of the QLx4300-S45 are capable of being dynamically managed by a system controller to provide maximum flexibility and optimum performance. These functions are controlled by interfacing to the highlighted pins in Figure 21. The specific procedures for controlling these aspects of the QLx4300-S45 are the focus of this section.

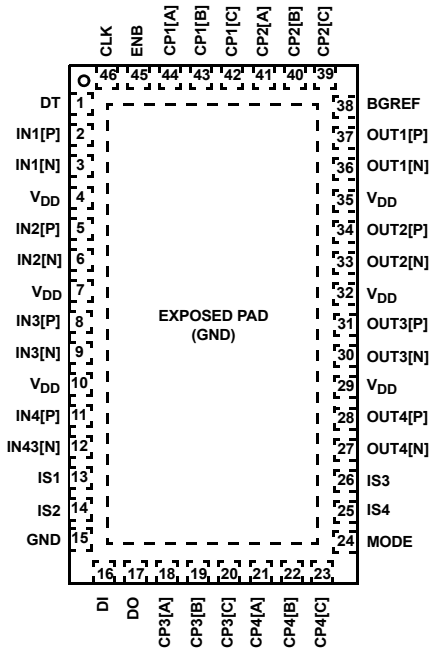


FIGURE 21. PIN DIAGRAM HIGHLIGHTING PINS USED FOR DYNAMIC CONTROL OF THE QLx4300-S45

TABLE 1. DESCRIPTIONS OF PINS THAT CAN BE USED TO SET EQUALIZATION BOOST LEVEL

PIN NAME	PIN NUMBER	DESCRIPTION
DI	16	Serial data input, CMOS logic. Input for serial data stream to program internal registers controlling the boost for all four equalizers. Synchronized with clock (CLK) on pin 46. Overrides the boost setting established on CP control pins. Internally pulled down.
DO	17	Serial data output, CMOS logic. Output of the internal registers controlling the boost for all four equalizers. Synchronized with clock on pin 46. Equivalent to serial data input on DI but delayed by 21 clock cycles.
CP3[A,B,C]	18, 19, 20	Control pins for setting equalizer 3. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and C is the LSB. Pins are internally pulled down through a 25kΩ resistor.
CP4[A,B,C]	21, 22, 23	Control pins for setting equalizer 4. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and C is the LSB. Pins are internally pulled down through a 25kΩ resistor.
MODE	24	Boost-level control mode input, CMOS logic. Allows serial programming of internal registers through pins DI, ENB, and Clk when set “HIGH”. Resets all internal registers to zero and uses boost levels set by CP pins when set LOW. If serial programming is not used, this pin should be grounded.
CP2[C,B,A]	39, 40, 41	Control pins for setting equalizer 2. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and C is the LSB. Pins are internally pulled down through a 25kΩ resistor.
CP1[C,B,A]	42, 43, 44	Control pins for setting equalizer 1. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and C is the LSB. Pins are internally pulled down through a 25kΩ resistor.
ENB	45	Serial data enable (active low), CMOS logic. Internal registers can be programmed with DI and CLK pins only when the ENB pin is ‘LOW’. Internally pulled down.
CLK	46	Serial data clock, CMOS logic. Synchronous clock for serial data on DI and DO pins. Data on DI is latched on the rising clock edge. Clock speed is recommended to be between 10MHz and 20MHz. Internally pulled down.

Equalization Boost Level

Channel equalization for the QLx4300-S45 can be individually set to either (a) one of 18 levels through the DC voltages on external control pins or (b) one of 32 levels via a set of registers programmed by a low speed serial bus. The pins used to control the boost level are highlighted in Figure 21. Descriptions of these pins are listed in Table 1. Please refer to “Pin Descrptions” on page 3 for descriptions of all other pins on the QLx4300-S45.

The boost setting for equalizer channel k can be read as a three digit ternary number across CP[k][A,B,C]. The ternary value is established by the value of the resistor between VDD and the CP[k][A,B,C] pin.

As a second option, the equalizer boost setting can be taken from a set of registers programmed through a serial bus interface (pins 16, 17, 45, and 46). Using this interface, a set of registers is programmed to store the boost level. A total of 21 registers are used. Registers 2 through 21 are parsed into four 5-bit words. Each 5-bit word determines which of 32 boost levels to use for the corresponding equalizer. Register 1 instructs the QLx4300-S45 to use registers 2 through 21 to set the boost level rather than the control pins CP[k][A,B,C].

Both options have their relative advantages. The control pin option minimizes the need for external controllers as the boost level can be set in the board design resulting in a compact layout. The register option is more flexible for cases in which the optimum boost level will not be known and can be changed by a host bus adapter with a small number of pins. It is noted that the serial bus interface can also be daisy-chained among multiple QLx4300-S45 devices to afford a compact programmable solution even when a large number of data lines need to be equalized.

Upon power-up, the default value of all the registers (and register 1 in particular) is zero, and thus, the CP pins are used to set the boost level. This permits an alternate interpretation on setting the boost level. Specifically, the CP pins define the default boost level until the registers are (if ever) programmed via the serial bus.

TABLE 2. MAPPING BETWEEN CP-SETTING RESISTOR AND PROGRAMMED BOOST LEVELS

RESISTANCE BETWEEN CP PIN AND V_{DD}			SERIAL BOOST LEVEL
CP[A]	CP[B]	CP[C]	
Open	Open	Open	0
Open	Open	25kΩ	2
Open	Open	0Ω	4
Open	25kΩ	Open	6
Open	25kΩ	25kΩ	8
Open	25kΩ	0Ω	10
Open	0Ω	Open	12
Open	0Ω	25kΩ	14
Open	0Ω	0Ω	15
0Ω	Open	Open	16
0Ω	Open	25kΩ	17
0Ω	Open	0Ω	19
0Ω	25kΩ	Open	21
0Ω	25kΩ	25kΩ	23
0Ω	25kΩ	0Ω	24
0Ω	0Ω	Open	26
0Ω	0Ω	25kΩ	28
0Ω	0Ω	0Ω	31

Control Pin Boost Setting

When register 1 of the QLx4300-S45 is zero (the default state on power-up), the voltages at the CP pins are used to determine the boost level of each channel. For each of the four channels, k, the [A], [B], and [C] control pins (CP[k]) are associated with a 3-bit non binary word. While [A] can take one of two values, ‘LOW’ or ‘HIGH’, [B] and [C] can take one of three different values: ‘LOW’, ‘MIDDLE’, or ‘HIGH’. This is achieved by changing the value of a resistor connected between V_{DD} and the CP pin, which is internally pulled low with a 25kΩ resistor. Thus, a ‘HIGH’ state is achieved by using a 0Ω resistor, ‘MIDDLE’ is achieved with a 25kΩ resistor, and ‘LOW’ is achieved with an open resistance. Table 2 defines the mapping from the 3-bit CP word to the 18 out of 32 possible levels available via the serial interface.

If all four channels are to use the same boost level, then a minimum number of board resistors can be realized by tying together like CP[k][A,B,C] pins across all channels k. For instance, all four CP[k][A] pins can be tied to the same resistor running to V_{DD}. Consequently, only three resistors are needed to control the boost of all four channels. If the CP Pins are tied together and the 25kΩ is used, the value changes to a 6.25kΩ resistor because the 25kΩ is divided by 4.

Optimal Cable Boost Settings

The settable equalizing filter within the QLx4300-S45 enables the device to optimally compensate for frequency-dependent attenuation across a wide variety of channels, data rates, and encoding schemes. For the reference channels plotted in Figure 2, Table 3 shows the optimal boost setting when transmitting a PRBS-7 signal. The optimal boost setting is defined as the equalizing filter setting that minimizes the output residual jitter of the QLx4300-S45. The settings in Table 4 represent the optimal settings for the QLx4300-S45 across an ambient temperature range of 0°C to +70°C. The optimal setting at room temperature (+20°C to +40°C) is generally one to two settings lower than the values listed in Table 3.

TABLE 3. OPTIMAL CABLE BOOST SETTINGS

CABLE	APPROX. LOSS @ 1.5625GHz (dB)	QLx4300-S45 BOOST
Cable A	17	12
Cable B	23	16
Cable C	28	23

NOTE: Optimal boost settings should be determined on an application-by-application basis to account for variations in channel type, loss characteristics, and encoding schemes. The settings in this table are presented as guidelines to be used as a starting point for application-specific optimization.

Register Description

The QLx4300-S45's internal registers are listed in Table 4. Register 1 determines whether the CP pins or register values 2 through 21 are used to set the boost level. When this register is set, the QLx4300-S45 uses registers 2-6, 7-11, 12-16, and 17-21 to set the boost level of equalizers 1, 2, 3, and 4. When register 1 is not set, the CP pins are used to determine the boost level for each equalizer channel. The use of five registers for each equalizer channel allows all 32 boost levels as candidate boost levels.

TABLE 4. DESCRIPTION OF INTERNAL SERIAL REGISTERS

REGISTER	EQUALIZER CHANNEL	DESCRIPTION
1	1-4	CP control override – Use registers 2 through 21 (rather than CP pins) to establish the boost levels when this bit is set.
2	1	Equalizer setting bit 0 (LSB).
3		Equalizer setting bit 1.
4		Equalizer setting bit 2.
5		Equalizer setting bit 3.
6		Equalizer setting bit 4 (MSB).
7	2	Equalizer setting bit 0 (LSB).
8		Equalizer setting bit 1.
9		Equalizer setting bit 2.
10		Equalizer setting bit 3.
11		Equalizer setting bit 4 (MSB).
12	3	Equalizer setting bit 0 (LSB).
13		Equalizer setting bit 1.
14		Equalizer setting bit 2.
15		Equalizer setting bit 3.
16		Equalizer setting bit 4 (MSB).
17	4	Equalizer setting bit 0 (LSB).
18		Equalizer setting bit 1.
19		Equalizer setting bit 2.
20		Equalizer setting bit 3.
21		Equalizer setting bit 4 (MSB).

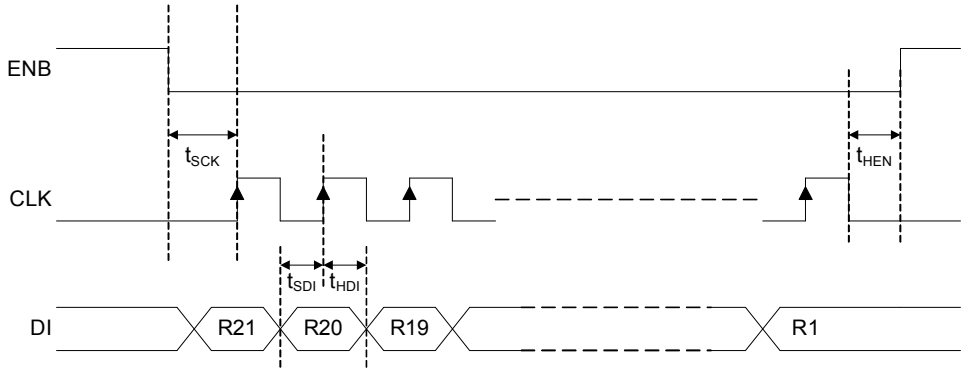


FIGURE 22. TIMING DIAGRAM FOR PROGRAMMING THE INTERNAL REGISTERS OF THE QLx4300-S45

Serial Bus Programming

Pins 16 (DI), 45 (ENB), and 46 (CLK) are used to program the registers inside the QLx4300-S45. Figure 22 shows an exemplary timing diagram for the signals on these pins. The serial bus can be used to program a single QLx4300-S45 according to the following steps:

1. The ENB pin is pulled 'LOW'.
   - While this pin is 'LOW', the data input on DI are read into registers but not yet latched.
   - A setup time of t_{SCK} is needed between ENB going 'LOW' and the first rising clock edge.
2. At least 21 values are read from DI on the rising edge of the CLK signal.
   - If more than 21 values are passed in, then only the last 21 values are kept in a FIFO fashion.
   - The data on DI should start by sending the value destined for register 21 and finish by sending the value destined for register 1.
   - A range of clock frequencies can be used. A typical rate is 10MHz. The clock should not exceed 20MHz.
   - Setup (t_{SDI}) and hold (t_{HDI}) times are needed around the rising clock edge.
3. The ENB pin is pulled 'HIGH' and the contents of the registers are latched and take effect.
   - After clocking in the last data bit, an additional t_{HEN} should elapse before pulling the ENB signal 'HIGH'.
   - After completing these steps, the new values will affect within t_D.

Programming Multiple QLx4300-S45 Devices

The serial bus interface provides a simple means of setting the equalizer boost levels with a minimal amount of board circuitry. Many of the serial interface signals can be shared among the QLx4300-S45 devices on a board and two options are presented in this section. The first uses common clock and serial data signals along with separate ENB signals to select which QLx4300-S45 accepts the programmed changes. The second method uses a common ENB signal as the serial data is carried-over from one QLx4300-S45 to the next.

Separate ENB Signals

Multiple QLx4300-S45 devices can be programmed from a common serial data stream as shown in Figure 23. Here, each QLx4300-S45 is provided its own ENB signal, and only one of these ENB signals is pulled 'LOW', and hence accepting the register data one at a time. In this situation, the programming of each equalizer follows the steps outlined in Figure 22.

DI/DO Carryover

The DO pin (pin 17) can be used to daisy-chain the serial bus among multiple QLx4300-S45 chips. The DO pin outputs the overflow data from the DI pin. Specifically, as data is pipelined into a QLx4300-S45, it proceeds according to the following flow. First, a bit goes into shadow register 1. Then, with each clock cycle, it shifts over into subsequent higher numbered registers. After shifting into register 21, it is output on the DO pin on the same clock cycle. Thus, the DO signal is equal to the DI signal, but delayed by 20 clock cycles. The timing diagram for the DO pin is shown in Figure 24 where the first 20 bits output from the DO are indefinite and subsequent bits are the data fed into the DI pin. The delay between the rising clock edge and the data transition is t_{CQ}.

A diagram for programming multiple QLx4300-S45s is shown in Figure 25. It is noted that the board layout should ensure that the additional clock delay experienced between subsequent QLx4300-S45s should be no more than the minimum value of t_{CQ}, i.e. 12ns.

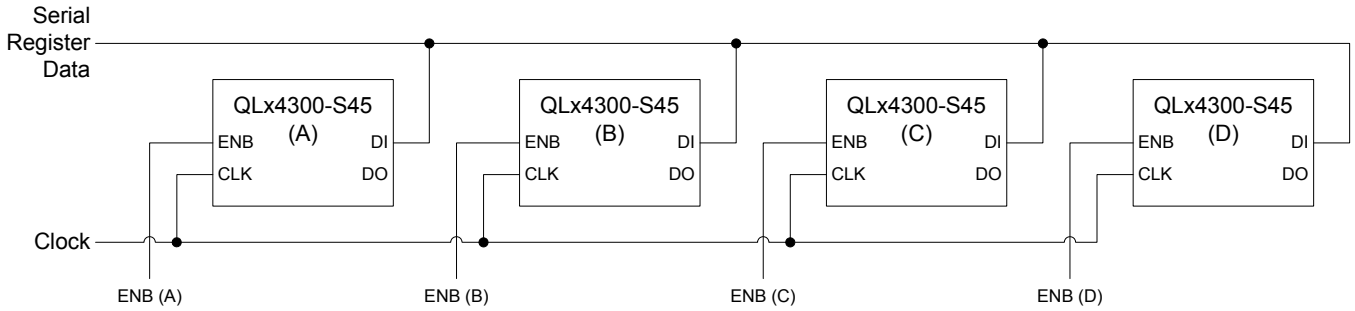


FIGURE 23. SERIAL BUS PROGRAMMING MULTIPLE QLx4300-S45 DEVICES USING SEPARATE ENB SIGNALS

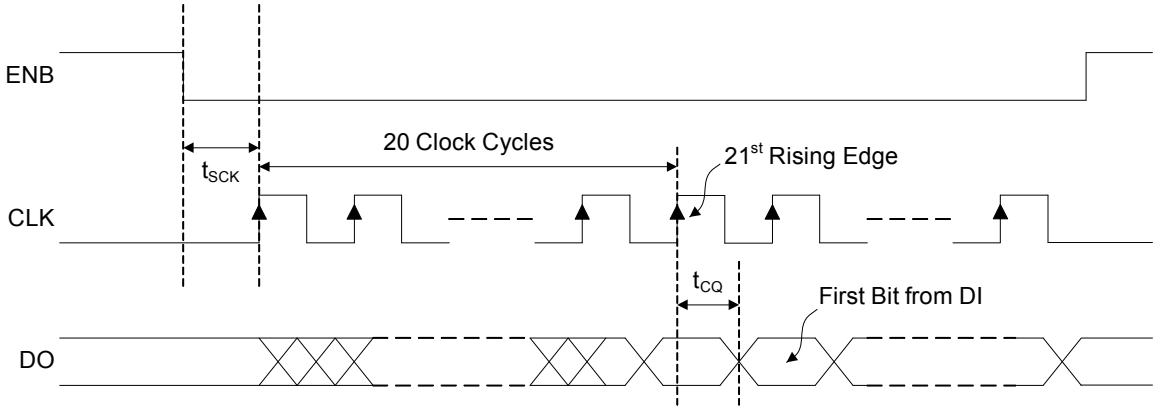


FIGURE 24. TIMING DIAGRAM FOR DI/DO CARRYOVER

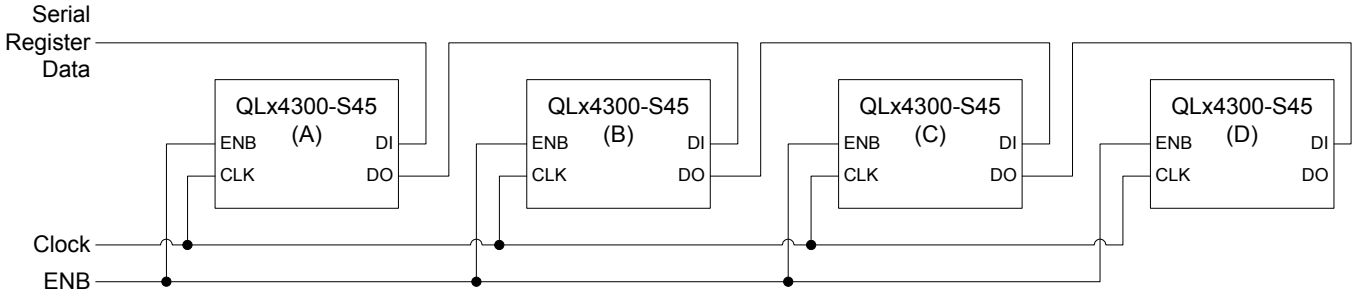


FIGURE 25. SERIAL BUS PROGRAMMING MULTIPLE QLx4300-S45 DEVICES USING DI/DO CARRYOVER

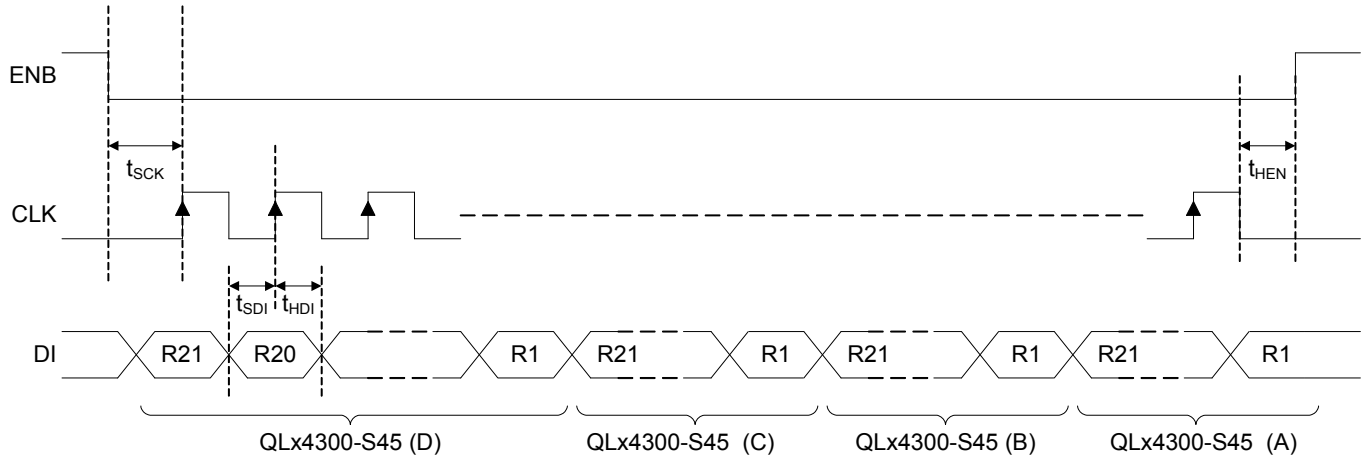


FIGURE 26. TIMING DIAGRAM FOR PROGRAMMING MULTIPLE QLx4300-S45 DEVICES USING DI/DO CARRYOVER

Detection Thereshold (DT) Pin Functionality

The QLx4300-S45 is capable of maintaining periods of line silence on any of its four channels by monitoring each channel for loss of signal (LOS) conditions and subsequently muting the outputs of a respective channel when such a condition is detected. A reference current applied to the detection threshold (DT) pin is used to set the LOS threshold of the internal signal detection circuitry. Current control on the DT pin is done via one or two external resistors. Nominally, both a pull-up and pull-down resistor are tied to the DT pin (Figure 27A), but if adequate control of the supply voltage is maintained to within ±3% of 1.2V, then a simple pull down resistor is adequate (as in Figure 27B). Resistors used should be at least 1/16W, with ±1% precision.

The internal bias point of the DT pin, nominally 1.05V, is used in conjunction with the voltage divider (R1 and R2) shown in Figure 27A to set the reference current on the DT pin.

Case 1: Channels with less than or equal to 17dB loss at 1.5625GHz:

For signals transmitted on channels having less than or equal to 25dB of loss at 2.5GHz, the optimal DT reference current is 0µA. This optimal reference current may be achieved by either leaving the DT pin floating, or tying the DT pin to ground (GND) with a 10MΩ resistor.

Case 2: Channels with greater 17dB loss at 1.5625GHz:

For channels exhibiting more than 25dB of total loss (this includes cable or FR-4 loss) the DT pin should be configured for a reference sink current (coming out of the DT pin) of approximately 2µA. A typical configuration for a 2µA sink current is given in Figure 27C. If the configuration in Figure 27B is utilized, a 525kΩ resistor is used.

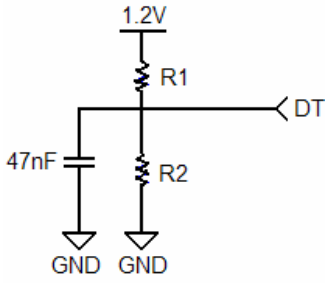


FIGURE 27A.

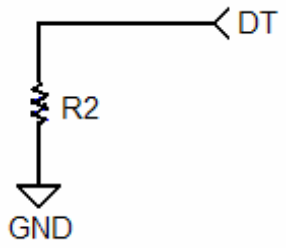


FIGURE 27B.

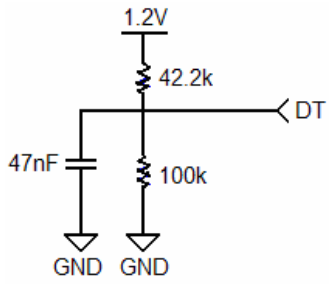


FIGURE 27C.

FIGURE 27.

Typical Application Reference Designs

Figures 28 and 29 show reference design schematics for a QLx4300-S45 evaluation board with an SMA connector interface. Figure 28 shows the schematic for the case when the equalizer boost level is set via the CP pins. Figure 29 shows the schematic for the case when the level is set via the serial bus interface.

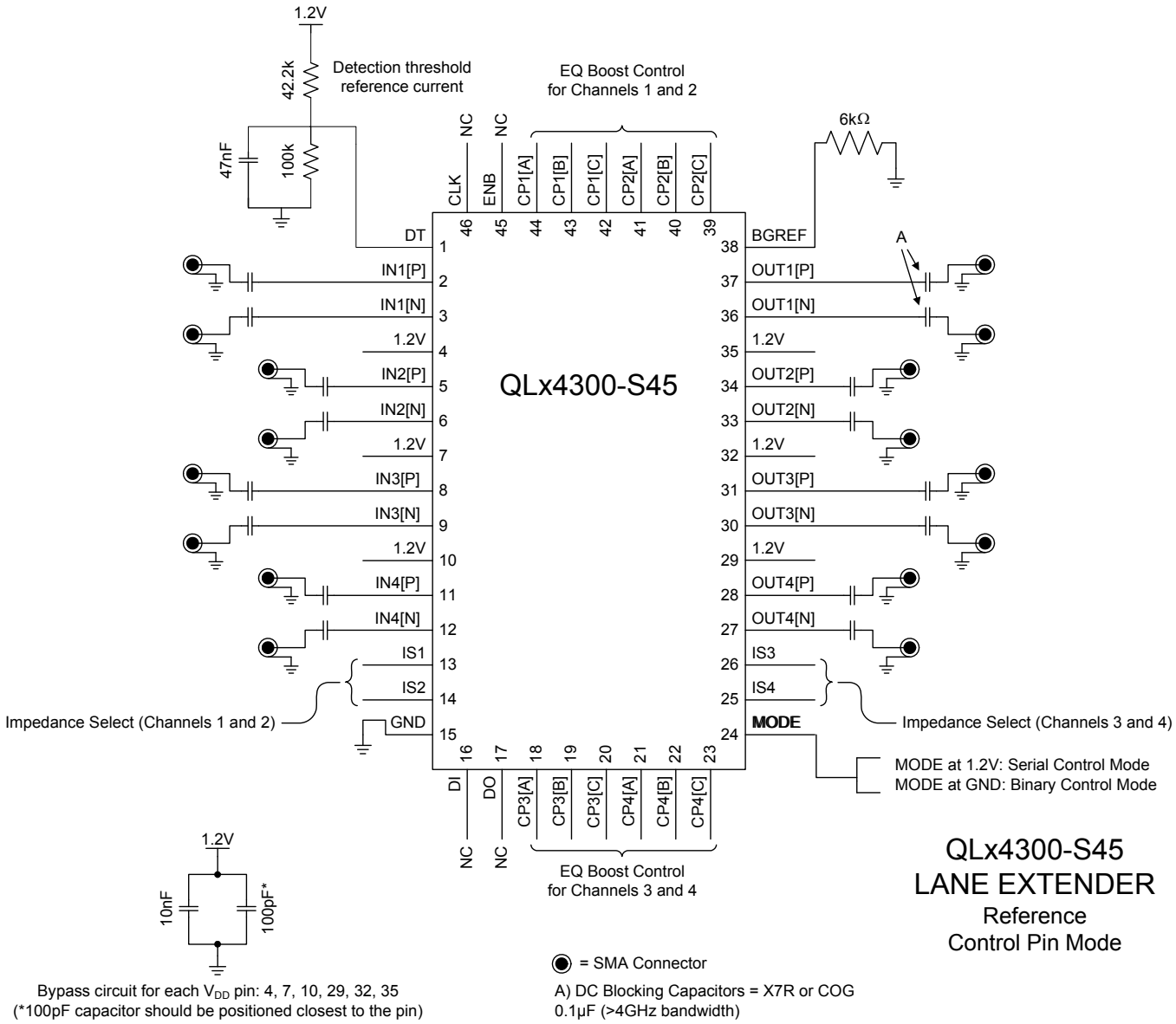


FIGURE 28. APPLICATION CIRCUIT FOR THE QLx4300-S45 EVALUATION BOARD USING THE CONTROL PINS FOR SETTING THE EQUALIZER COMPENSATION LEVEL

Typical Application Reference Designs (Continued)

Figures 28 and 29 show reference design schematics for a QLx4300-S45 evaluation board with an SMA connector interface. Figure 28 shows the schematic for the case when the equalizer boost level is set via the CP pins. Figure 29 shows the schematic for the case when the level is set via the serial bus interface.

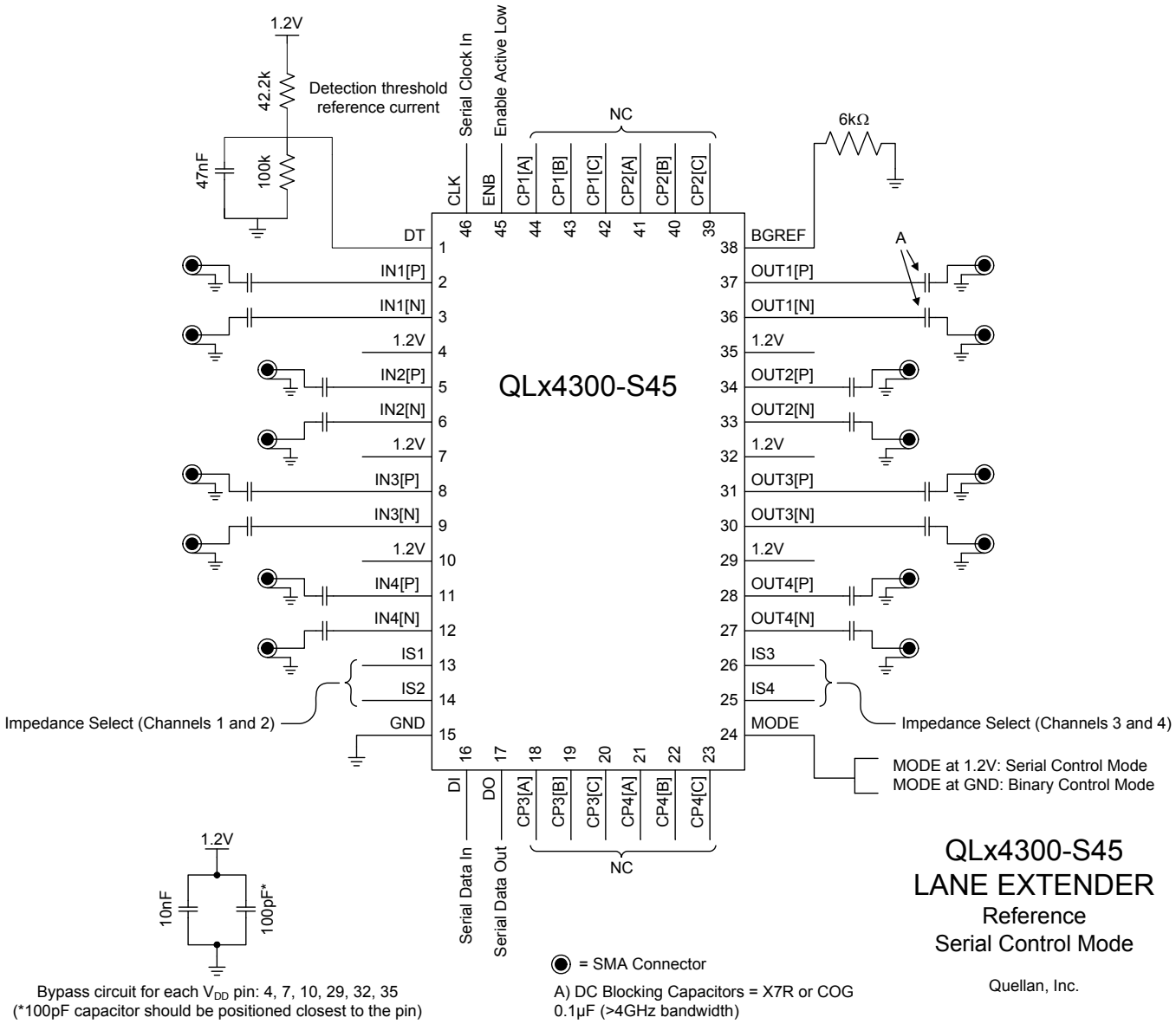


FIGURE 29. APPLICATION CIRCUIT FOR THE QLx4300-S45 EVALUATION BOARD USING THE SERIAL BUS INTERFACE FOR SETTING THE EQUALIZER COMPENSATION LEVEL

About Q:ACTIVE®

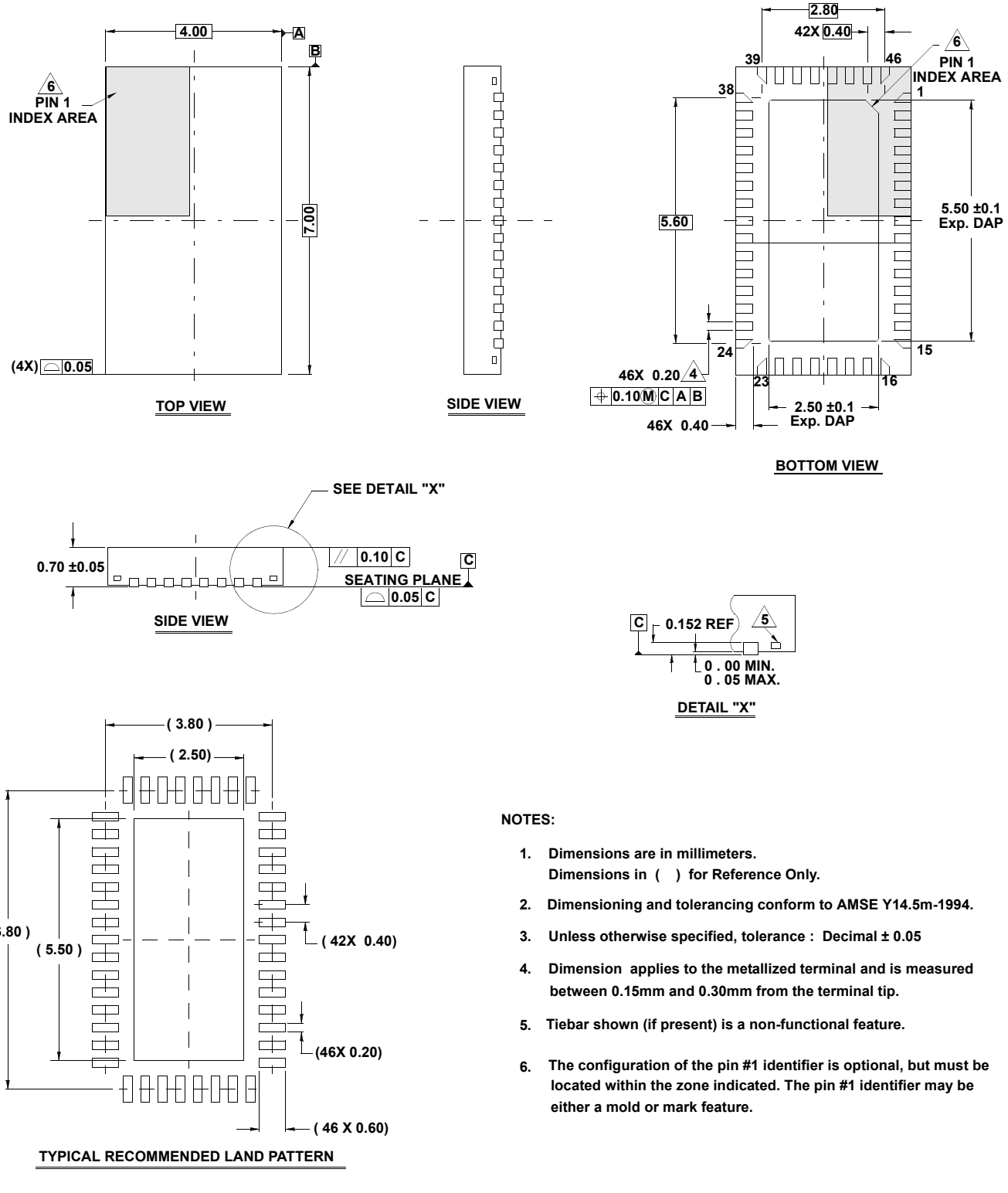
Intersil has long realized that to enable the complex server clusters of next generation datacenters, it is critical to manage the signal integrity issues of electrical interconnects. To address this, Intersil has developed its groundbreaking Q:ACTIVE® product line. By integrating its analog ICs inside cabling interconnects, Intersil is able to achieve unsurpassed improvements in reach, power consumption, latency, and cable gauge size as well as increased airflow in tomorrow's datacenters. This new technology transforms passive cabling into intelligent "roadways" that yield lower operating expenses and capital expenditures for the expanding datacenter.

Intersil Lane Extenders allow greater reach over existing cabling while reducing the need for thicker cables. This significantly reduces cable weight and clutter, increases airflow, and reduces power consumption.

Package Outline Drawing

L46.4x7

46 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE (TQFN)
Rev 0, 9/09



NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.