HMC1027BG

14.2 GBPS, 13X13 ASYNCHRONOUS CROSSPOINT SWITCH WITH EQUALIZATION AND DE-EMPHASIS

Features

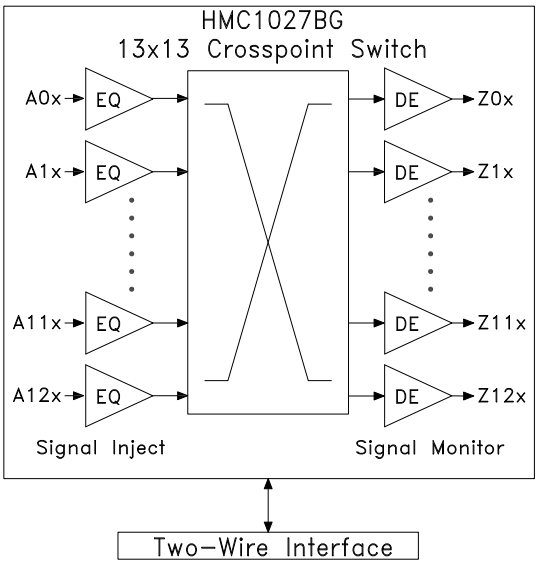
- Supports Data Rates from DC to 14.2 Gbps
- Protocol and Data Rate Agnostic
- Fully Non-Blocking, with Multicast and Broadcast
- Excellent Crosstalk Immunity (>35 dB)
- Data Invert on Both Input and Output Channels
- Output Squelch Mode
- Low Latency (<380 ps)
- Up to 20 dB Programmable Input Equalization
- Equalization Bypass Mode for Short Links
- Programmable Output Amplitude Control: 400 mVppd to 800 mVppd
- Programmable Output De-emphasis Control: 0 to 12 dB
- 13th Channel Available for Signal Inject and Monitor
- Low-Power Operation
  - 69 mW/Channel in Equalization Bypass Mode
  - 92 mW/Channel in Equalization Enable Mode
- Single 2.5 V Supply Operation with Ability for I/O to Operate at 1.8 V
- Independent Input and Output Power Down Options of Unused Channels
- 14x14 mm, 1 mm ball pitch, 169 pin BGA
- Digital Control via Two-wire interface

Typical Applications

The HMC1027BG is ideal for:

- Supports SONET OC192, 10GbE and FEC rates 8/16G FC, 10G QDR, and 14G FDR IB, 6/12G SAS/SATA
- Signal Conditioning and Distribution for Backplanes and Linecards
- Optical Transport Switch and Protect
- Redundancy Switching
- Video Broadcasting
- FPGA Interfacing
- Broadband Test and Measurement Equipment

Functional Diagram



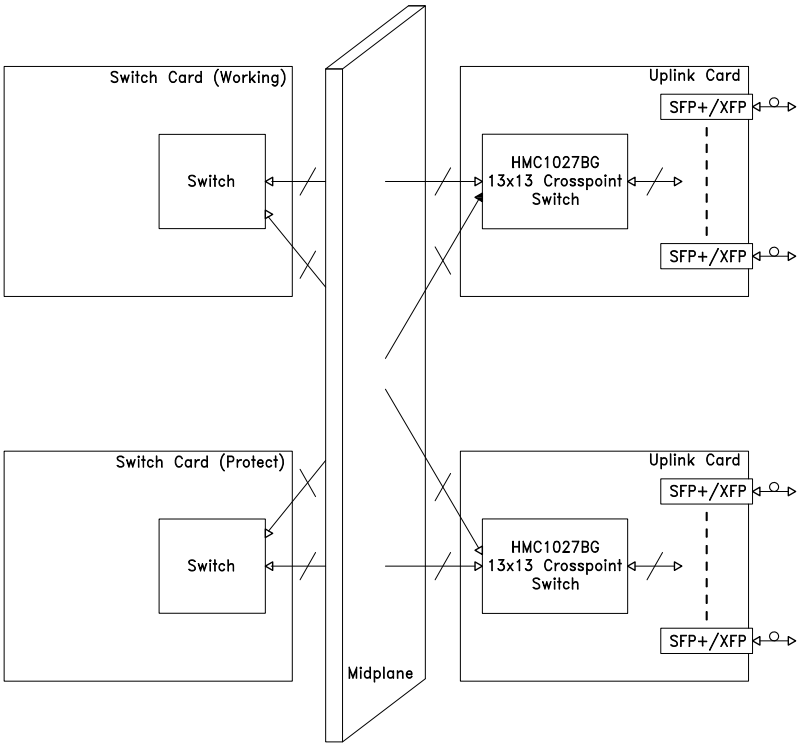
14.2 GBPS 13X13 ASYNCHRONOUS CROSSPOINT SWITCH WITH EQUALIZATION AND DE-EMPHASIS

General Description

The HMC1027BG is an extremely low-power, high-performance, fully programmable asynchronous 13x13 crosspoint switch operating with data rates up to 14.2 Gbps. The HMC1027BG consists of a programmable input equalizer, a 13x13 switch, and a de-emphasis based programmable output driver. The 13x13 switch is fully non-blocking and it allows any input to be routed to any output, any combination of outputs, or broadcast to all outputs. The HMC1027BG performs both receive equalization (EQ) and transmit de-emphasis (DE) on all input and output channels to compensate signal impairments due to inter-symbol interference (ISI) caused by a wide variety of transmission media and channel lengths. The input equalizer can be bypassed for short links to further reduce the overall power dissipation. The 13th channel is identical to the other 12 channels and it can be either used as the 13th channel or signal inject and monitor for debugging purposes during the prototyping stage.

All high-speed differential inputs and outputs of the HMC1027BG are Current Mode Logic (CML) and terminated on-chip with 50 ohms to the positive supply, 1.8 V or 2.5 V, and may be DC or AC coupled. The inputs and outputs of the HMC1027BG can be operated either differentially or single ended. The low-power, high-performance and feature-rich HMC1027BG is packaged in a 169 pin and 1 mm ball pitch, 14x14 mm BGA package. The device uses a 2.5 V core supply but the I/O can be operated at 1.8 V supply to reduce the power dissipation to less than 92 mW per channel. The HMC1027BG operates over a case temperature range of -40 °C up to 85 °C.

Typical Application: 10G Optical Transport Switch and Protect



Electrical Specifications, T_A = +25 °C,

Vcc = +2.5 V, V2WI = +3.3 V, VCCI = +1.8 V, VCCO = +1.8 V, 14.2 Gbps, unless otherwise indicated

Parameter	Conditions / Notes	Min	Typ	Max	Units
Data Rate		DC		14.2	Gbps
Supply Voltage VCC		2.375	2.5	2.625	V
Supply Voltage VCCI		1.71	1.8 / 2.5	2.625	V
Supply Voltage VCCO	VCCO ≥ VCC - 0.7 V	1.71	1.8 / 2.5	2.625	V
Supply Voltage V2WI		3.135	3.3	3.465	V
Operating Temperature		-40		+85	°C
Signal Inputs					
CML Input Voltage Swing	Differential	50		2000	mVppd
CML Input Voltage Swing	Single-ended	50		1000	mVpp
CML Common-mode Input voltage	AC coupled	1.71	VCCI	2.625	V
CML Input Termination Resistance	Single-ended	50	55	60	Ω
CML Input Termination Resistance	Differential	100	110	120	Ω
CML Input Return Loss	≤7 GHz		10		dB
Input Equalization	11.3 Gbps 12.5 Gbps 14.2 Gbps			20 16 15	dB
Equalization Resolution			0.24	0.33	dB/LSB
CML Signal Ouputs					
Output Voltage Swing, Programmable	Differential	400		800	mVppd
Output Voltage High	Single-ended, de-emphasis off	VCCO - 50	VCCO	VCCO + 50	mV
Output Voltage Low, Programmable	Single-ended, de-emphasis off	VCCO - 400		VCCO - 200	mV
Output Termination Resistance	Single-ended	45	50	55	Ω
Output Termination Resistance	Differential	90	100	110	Ω
De-emphasis Voltage Ratio, Programmable	14.2 Gbps	0		12	dB
De-emphasis Resolution			0.5	1.5	dB/LSB
AC Characteristics					
Propagation Delay		270	325	380	ps
Input Skew			±10		ps
Output Skew			±10		ps
Rise Time			22	30	ps
Fall Time			23	30	ps
Random Jitter [1]	11.3 Gbps 3 dB loss 12.5 Gbps 3 dB loss 14.2 Gbps 3 dB loss		190 200 200		fs
Data Dependant Jitter [1] [2]	11.3 Gbps 3 dB loss 12.5 Gbps 3 dB loss 14.2 Gbps 3 dB loss		0.09 0.10 0.13		UI
Two-wire I/O					
Input High voltage		1.75			V
Input Low Voltage				0.75	V
Output High Voltage		V2WI - 5%	V2WI		V
Ouput Low Voltage				0.372	V

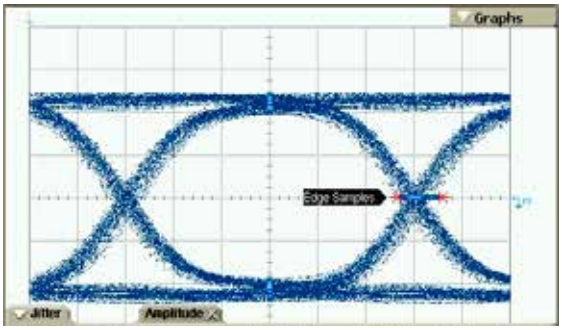
Electrical Specifications (continued), T_A = +25 °C

Vcc = +2.5 V, V2WI = +3.3 V, VCCI = +1.8 V, VCCO = +1.8 V, 14.2 Gbps, unless otherwise indicated

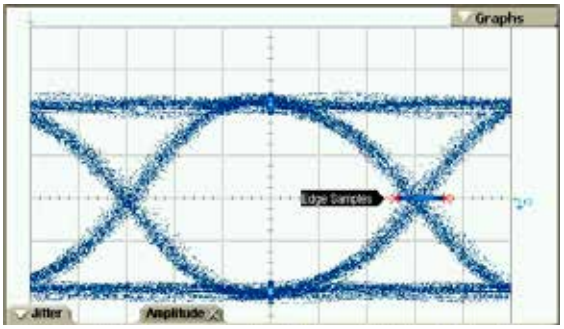
Parameter	Conditions / Notes	Min	Typ	Max	Units
Power					
Power Dissipation	All 13 channels ON, AC-coupled, 400 mVppd, no DE, EQ enable mode		1.2	1.35	W
Power Dissipation	All 13 channels ON, AC-coupled, 400 mVppd, no DE, EQ bypass mode		0.89	0.99	W
Power Per Channel	AC-coupled, 400 mVppd, no DE, EQ enable mode		92	104	mW
	AC-coupled, 400 mVppd, no DE, EQ bypass mode		69	77	mW
Current Consumption VCC	AC-coupled, 400 mVppd, no DE, EQ enable mode		397	423	mA
	AC-coupled, 400 mVppd, no DE, EQ bypass mode		273	286	mA
Current Consumption VCCO	AC-coupled, 400 mVppd, no DE		117	130	mA
Current Consumption VCCI			80 - 90		mA
Power Supply Rejection Ratio	50 mV at 400 kHz		-45	-42	dB

[1] Measured with PRBS15 [2] DDJ will vary with load conditions.

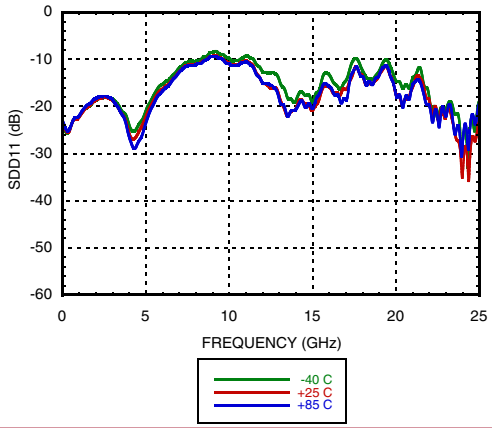
11.3 Gbps Eye Diagram



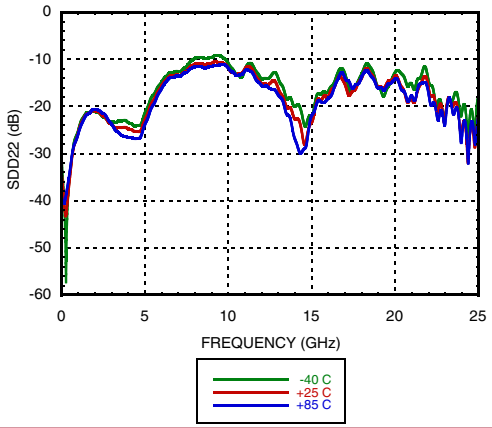
14.2 Gbps Eye Diagram



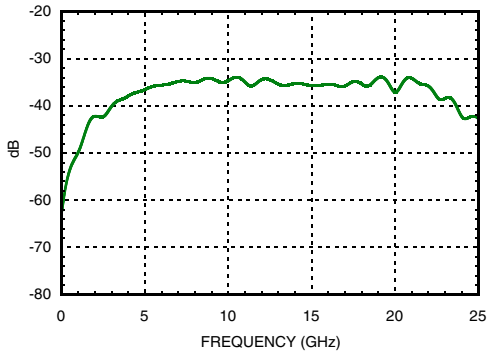
Input Return Loss



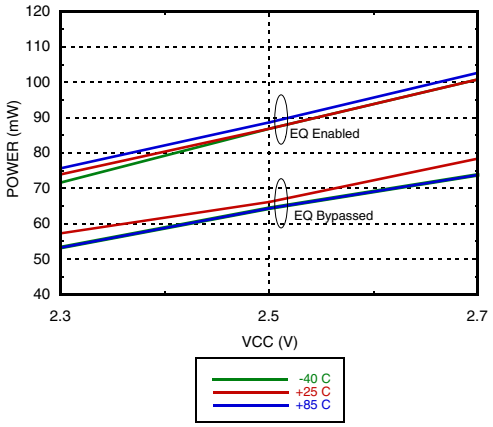
Output Return Loss



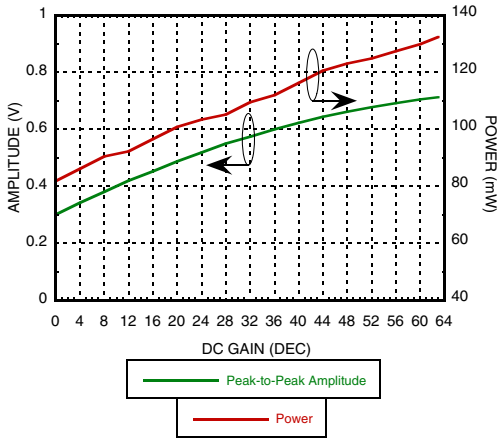
Channel-to-Channel Isolation



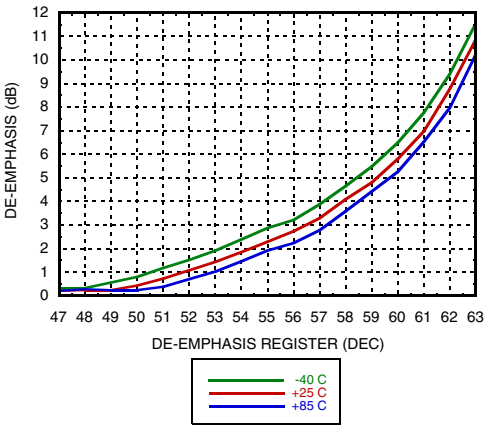
Power [1][2]



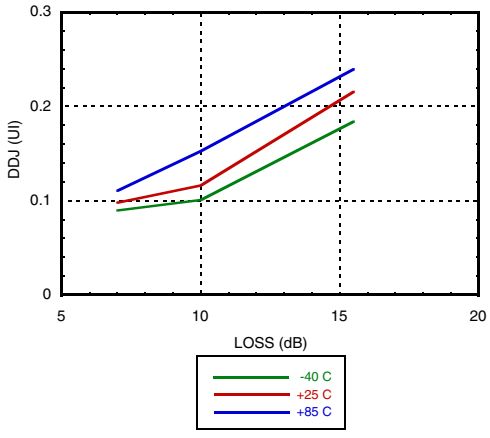
Output Vppd De-emphasis DC Gain 0 dB Peaking



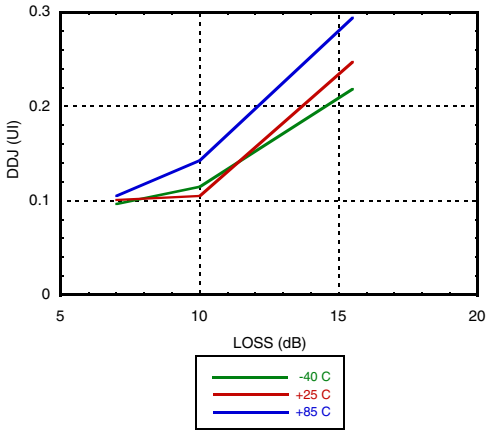
De-emphasis Peaking @ 14.2 Gbps [1][2]



Receiver DDJ @14.2 Gbps with Crosstalk Off



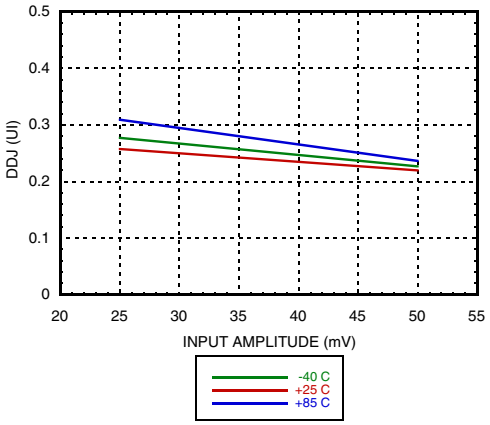
Receiver DDJ @14.2 Gbps with Crosstalk On



[1] VCCO = 1.8 V [2] Amplitude = 300 mVppd

14.2 GBPS 13X13 ASYNCHRONOUS CROSSPOINT SWITCH WITH EQUALIZATION AND DE-EMPHASIS

Differential Input Sensitivity



Absolute Maximum Ratings

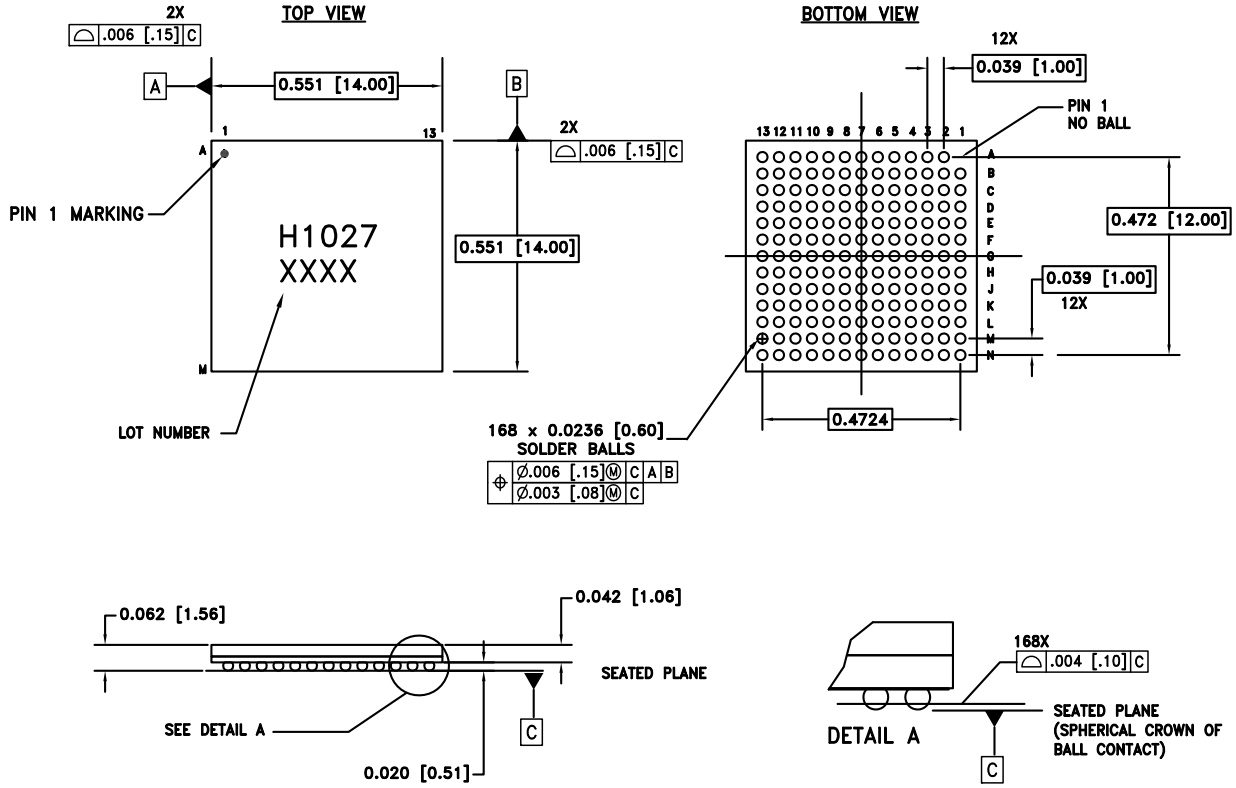
Power Supply Voltage VCC	-0.5 V to +3.75 V
Power Supply Voltage VCCI	- 0.5 V to +3.75 V VCC -1.0 V to VCC +1.0 V
Power Supply Voltage VCCO	- 0.5 V to +3.75 V VCC -1.0 V to VCC +1.0 V
Power Supply Voltage V2WI	-0.5 V to +3.75 V
Control Input Signals	-0.5 V to +3.75 V
CML Input Signals	VCCI -1.5 V to VCCI +0.5 V
Control Output Signals	-0.5 V to +3.75 V
CML Output Signals	VCCO -1.5 V to VCCO +0.5 V
Continuous Pdiss (T = 85 °C) (Derate 17 mW/°C above 85 °C)	2.6 W
Thermal Resistance ($R_{th\ j\text{-}p}$) worst case junction to package paddle	15 °C/W
Junction Temperature	125 °C
Storage Temperature	-65 °C to +150 °C
Operating Temperature	-40 °C to +85 °C
ESD Sensitivity (HBM)	Class 1C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

14.2 GBPS 13X13 ASYNCHRONOUS CROSSPOINT SWITCH WITH EQUALIZATION AND DE-EMPHASIS

Outline Drawing



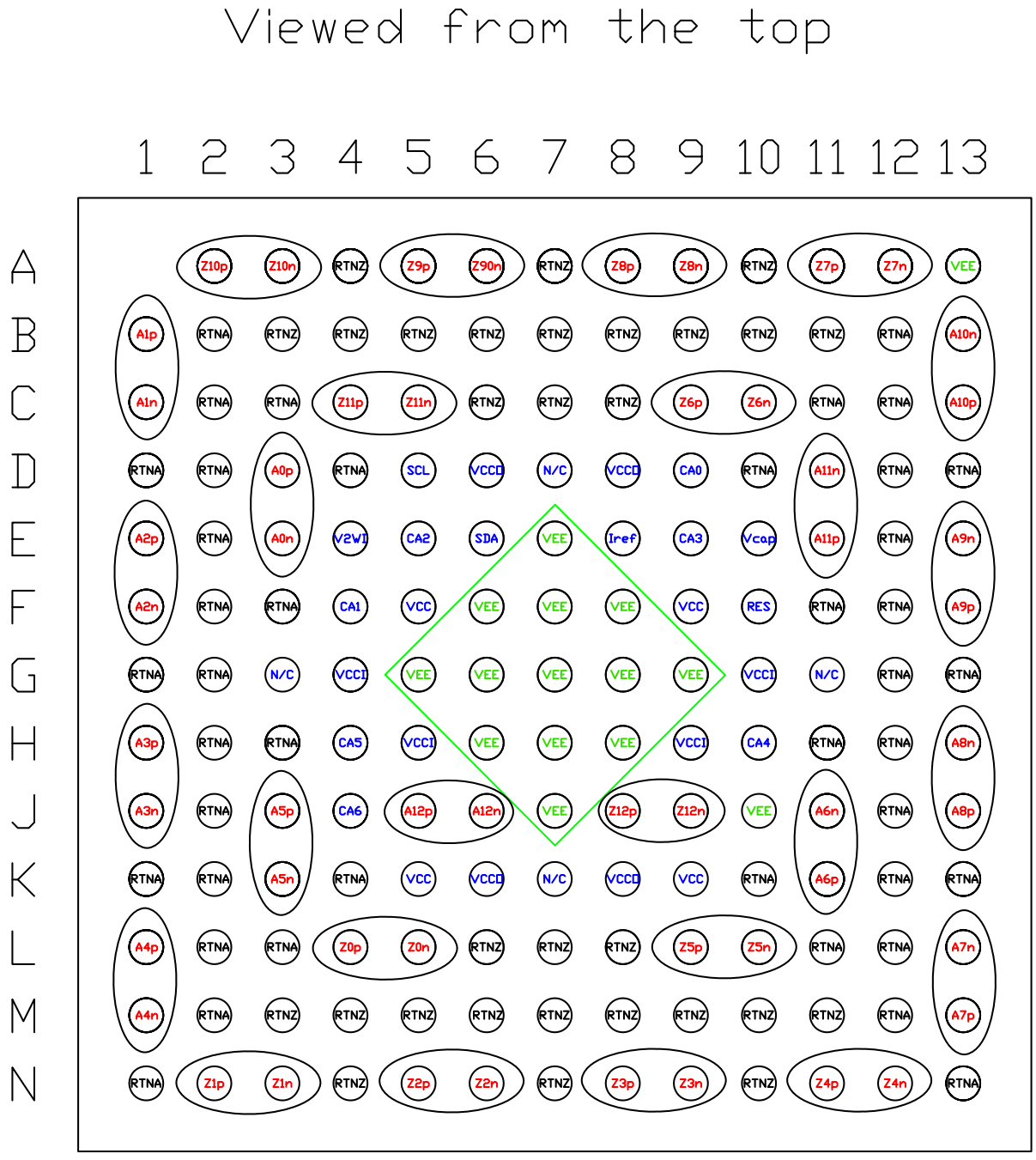
NOTES:
1. PACKAGE BASE: GLASS REINFORCED LAMINATE
2. SOLDER BALL: 0.0295 (0.75 mm) DIAMETER ON 0.050 (1.27 mm) SPACING.
3. SOLDER BALL MAKEUP: SAC305.
4. CHARACTERS TO BE LASER MARKED WITH 0.11 (2.5 mm) HIGH.
5. BURRS SHALL NOT EXCEED PACKAGE OD BY 0.006 (0.15 mm) MAX.
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTIE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.
8.MAXIMUM REFLOW TEMPERATURE IS 245 °C.

Package Information

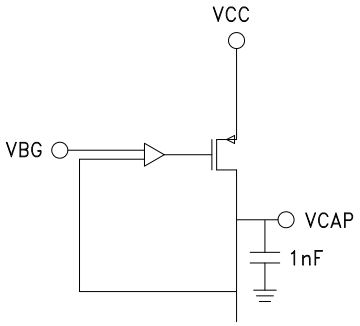
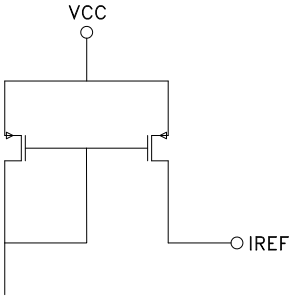
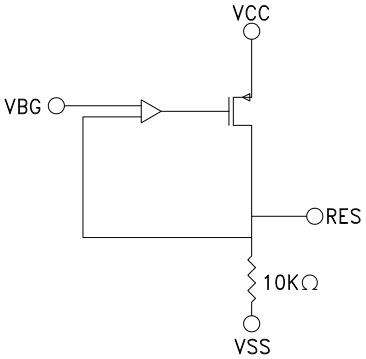
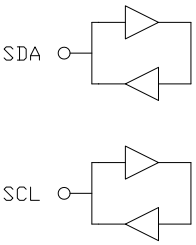
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC1027BG	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL3 [1]	H1027 XXXX

[1] Max peak reflow temperature of 245 °C
[2] 4-Digit lot number XXXX

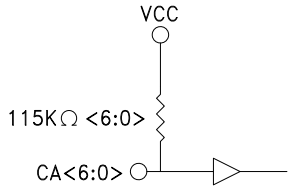
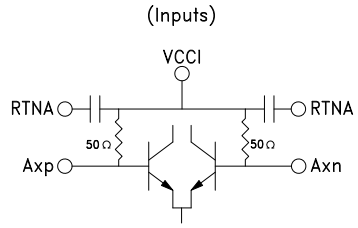
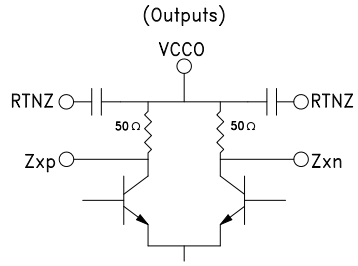
Pin Descriptions



Pin Descriptions

Pin Number	Function	Pin Type	Description	Interface Schematic
F5, F9, K5, K9	VCC	Power	Positive 2.5 V supply	
A13, E7, F6, F7, F8, G5, G6, G7, G8, G9, H6, H7, H8, J7, J10	VEE	Power	Ground supply	
E10	VCAP	Output	Positive 1.8 V supply regulator 1 nF external capacitor required	
E8	IREF	Output	Analog bias	
F10	RES	Output	Analog external bias resistor	
E6, D5	SDA, SCL	Input/Output	Two wire digital data and clock	

Pin Descriptions (continued)

Pin Number	Function	Pin Type	Description	Interface Schematic
J4, H4, H10, E9, E5, F4, D9	CA[6:0]	Input	Chip address	
B2, B12, C2, C3, C11, C12, D1, D2, D4, D10, D12, D13, E2, E12, F2, F3, F11, F12, G1, G2, G12, G13, H2, H3, H11, H12, J2, J12, K1, K2, K4, K10, K12, K13, L2, L3, L11, L12, M2, M12, N1, N13	RTNA	Input	Analog Input Returns Tie to GND or VCCI	
G4, G10, H5, H9	VCCI	Power	Receiver input termination supply (2.5 V/1.8 V)	
D3, E3 B1,C1 E1, F1 H1, J1 L1, M1 J3, K3 K11, J11 M13, L13 J13, H13 F13, E13 C13, B13 E11, D11 J5, J6	A0p, A0n A1p, A1n A2p, A2n A3p, A3n A4p, A4n A5p, A5n A6p, A6n A7p, A7n A8p, A8n A9p, A9n A10p, A10n A11p, A11n A12p, A12n	Input	Differential data inputs, referenced to VCCI positive supply	
A4, A7, A10, B3-B11, C6-C8, L6-L8, M3-M11, N4, N7, N10	RTNZ	Output	Analog Output Returns Tie to GND or VCCO	
D6, D8, K6, K8	VCCO	Power	Transmitter termination supply (2.5 V/1.8 V)	
L4, L5 N2, N3 N5, N6 N8, N9 N11, N12 L9, L10 C9, C10 A11, A12 A8, A9 A5, A6 A2, A3 C4, C5 J8, J9	Z0p, Z0n Z1p, Z1n Z2p, Z2n Z3p, Z3n Z4p, Z4n Z5p, Z5n Z6p, Z6n Z7p, Z7n Z8p, Z8n Z9p, Z9n Z10p, Z10n Z11p, Z11n Z12p, Z12n	Output	Differential data outputs, referenced to VCCO positive supply	
E4	V2WI	Power	+3.3 V pad power (two wire)	
A1	Empty		Position ball	
D7, G3, G11, K7	N/C		These pins are not connected internally	

Theory of Operation

The HMC1027BG consists of the following functional blocks:

1. Receiver Equalizer
2. Selectable Input Invert
3. Crosspoint Switch
4. Selectable Output Invert
5. Transmitter De-emphasis

Power Sequence and Initial Setup

Observe recommended power sequencing for correct operation of the HMC1027BG. Initialization and setup is accomplished via programming through the two-wire interface (TWI). The proper power-up sequence is VCC, VCCI, VCCO, and finally V2WI, while the power-down sequence is just the reverse. The register map and corresponding descriptions are found in Table 11. The switch is configurable and there are specific items that need to be programmed in order to get started.

Once power is stable, a soft reset must be performed. This is done by writing the following registers and values:

- Set register 0x04 to 0xD6
- Set register 0x06 to 0x80
- Set register 0x06 to 0x00
- Set register 0x04 to 0x00

The Input Receiver Enable Registers (0x10 and 0x11), Input Equalizer Enable Registers (0x08 and 0x09), Output De-emphasis Enable Registers (0x0A and 0x0B), and Output Driver enable Registers (0x12 and 0x13) are used to select the user-defined channels for operation. Registers (0x19) and (0x1A) should be set to 0x40 and 0x3F, respectively.

The 13x13 Crospoint Switch matrix is configured for active I/O channels by programming Switch Channel Registers (0x20 through 0x2B and 0x2F). See Tables 7 and 8. The final step for initial setup of the HMC1027BG is to program the Input Equalizer and Output De-emphasis Registers to compensate for lossy channel impairments.

Table 1. Reg 0x08-0x09 Equalization Enable Registers

Name	Reg	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit 2	Bit 1	Bit 0
EQ_EN_B	0x08	R/W	0xFF	Ch12	RSV	RSV	RSV	Ch11	Ch10	Ch9	Ch8
EQ_EN_A	0x09	R/W	0xFF	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0

1 = enabled

0 = disabled and powered off

Table 2. Reg 0x0A-0x0B De-emphasis Enable Registers

Name	Reg	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit 2	Bit 1	Bit 0
De_Emph_B	0x0A	R/W	0xFF	Ch12	RSV	RSV	RSV	Ch11	Ch10	Ch9	Ch8
De_Emph_A	0x0B	R/W	0xFF	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0

1 = enabled

0 = disabled and powered off

Table 3. Reg 0x10-0x11 Input Receiver Enable Registers

Name	Reg	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit 2	Bit 1	Bit 0
Input_EN_B	0x10	R/W	0x00	Ch12	RSV	RSV	RSV	Ch11	Ch10	Ch9	Ch8
Input_EN_A	0x11	R/W	0x00	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0

1 = enabled

0 = disabled

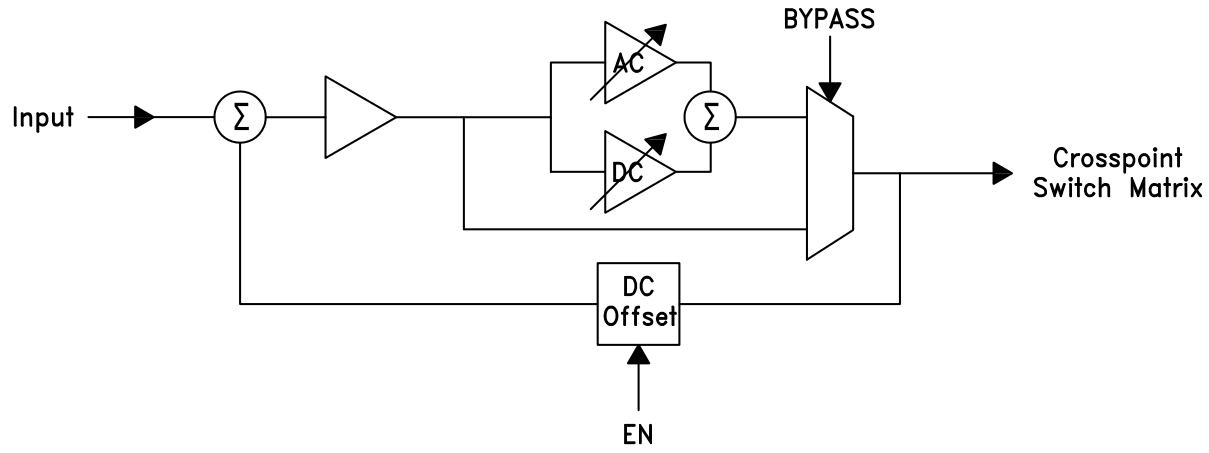
Table 4. Reg 0x12-0x13 Output Driver Enable Registers

Name	Reg	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit 2	Bit 1	Bit 0
Output_EN_B	0x12	R/W	0x00	Ch12	RSV	RSV	RSV	Ch11	Ch10	Ch9	Ch8
Output_EN_A	0x13	R/W	0x00	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0

1 = enabled

0 = disabled

Receiver Equalizer

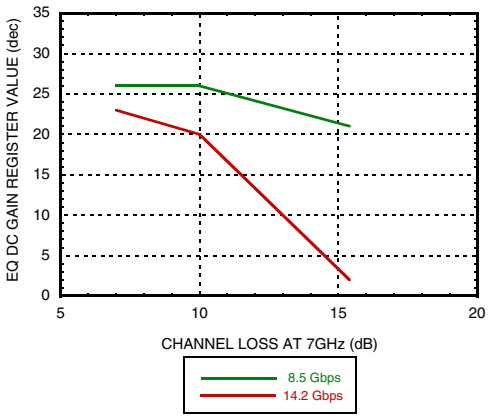


Each input channel has its own fully programmable Equalizer and each independent Equalizer is controlled by two registers. For example, channel 0 is controlled by registers 0x80 and 0x81. The first register (0x80) controls whether the EQ is bypassed or enabled via bits <7:6>. Bypass mode can be used in combination with a clean input signal to the RX and will save on power dissipation. Bits <5:0> control the amount of DC gain (see Table 5 for details). The second register (0x81) controls the DC offset enable with bit 6 and the AC gain is controlled with bits <5:0> (see Table 5 for details). Essentially, the RX can be programmed to overcome up to 20 dB of loss seen at its input.

Table 5. Channel Equalization Control Registers

Name	Reg Addr(s)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit 2	Bit 1	Bit 0
Equalizer DC Gain	0x80, 0x84, 0x88, 0x8C, 0x90, 0x94, 0x98, 0x9C, 0xA0, 0xA4, 0xA8, 0xAC, 0xBC	01 = EQ Bypass 10 = EQ Enable		DC Gain Setting (refer to Graph 1) 111111: Maximum 000000: Minimum					
Equalizer AC Gain	0x81, 0x85, 0x89, 0x8D, 0x91, 0x95, 0x99, 0x9D, 0xA1, 0xA5, 0xA9, 0xAD, 0xBD	Not Used	DC Offset 0 = Disable 1 = Enable	AC Gain Setting (set to 0x1E and then optimize eye from this point) 111111: Maximum 000000: Minimum					

Graph 1. EQ DC Gain Register Value vs. Channel Loss [1]



[1] Settings need to be optimized for actual channel and data rate.

Selectable Input Invert

The selectable input invert allows the user to independently invert any input signal using the Input Polarity Registers 0x0C and 0x0D. The bit corresponding to the input to be inverted needs to be set to a 1.

Table 6. Reg 0x0C-0x0D Input Polarity Registers

Name	Reg	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit 2	Bit 1	Bit 0
Input_Pol_B	0x0C	R/W	0x00	Ch12	RSV	RSV	RSV	Ch11	Ch10	Ch9	Ch8
Input_Pol_A	0x0D	R/W	0x00	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0

1 = inverted

0 = not inverted

The switch is asynchronous, non-blocking , low power and capable of supporting data rates up to 14.2 Gbps. The switch has 13 differential inputs that are independently programmable to be routed to any single, any combination or broadcast to all of the 13 differential outputs. The switch must be setup to use the desired input and output channel(s). In order to route an input to an output, the Input_Sel register must be set to the correct value as shown in Tables 7 and 8. There is one Input_Sel register that corresponds to each output. The value programmed into this register corresponds to the input to be routed to that specific output (see Tables 7 and 8). For example, in order to connect Input Channel 1 to Output Channel 1, set Register 0x21 to 0x2. In order to connect Input Channel 1 to Output Channels 2, 4, and 8, set registers 0x22, 0x24, and 0x28 to a 0x2. In order to broadcast Input Channel 5 to all Output Channels, write a 0x6 to every one of the Switch Channel Registers. Finally, to squelch any channel, write a 0x40 to the Switch Channel Register to be squelched.

Table 7. Reg 0x20-0x2F Switch Channel Registers

Name	Reg	Type	Default	Bit	Description
Input_Sel0	0x20	R/W	0x00	[3:0]	Input Select for Output 0
Input_Sel1	0x21	R/W	0x00	[3:0]	Input Select for Output 1
Input_Sel2	0x22	R/W	0x00	[3:0]	Input Select for Output 2
Input_Sel3	0x23	R/W	0x00	[3:0]	Input Select for Output 3
Input_Sel4	0x24	R/W	0x00	[3:0]	Input Select for Output 4
Input_Sel5	0x25	R/W	0x00	[3:0]	Input Select for Output 5
Input_Sel6	0x26	R/W	0x00	[3:0]	Input Select for Output 6
Input_Sel7	0x27	R/W	0x00	[3:0]	Input Select for Output 7
Input_Sel8	0x28	R/W	0x00	[3:0]	Input Select for Output 8
Input_Sel9	0x29	R/W	0x00	[3:0]	Input Select for Output 9
Input_Sel10	0x2A	R/W	0x00	[3:0]	Input Select for Output 10
Input_Sel11	0x2B	R/W	0x00	[3:0]	Input Select for Output 11
Input_Sel12	0x2F	R/W	0x00	[3:0]	Input Select for Output 12

Table 8. Channel Selection Table

Bit Value	Description
0x0	No input channel selected
0x1	Select Input Channel 0
0x2	Select Input Channel 1
0x3	Select Input Channel 2
0x4	Select Input Channel 3
0x5	Select Input Channel 4
0x6	Select Input Channel 5
0x7	Select Input Channel 6
0x8	Select Input Channel 7
0x9	Select Input Channel 8
0xA	Select Input Channel 9
0xB	Select Input Channel 10
0xC	Select Input Channel 11
0xD	Select Input Channel 12
0x40	Squelch

Selectable Output Invert

The selectable output invert allows the user to independently invert any output signal using the Output Polarity Registers 0x0E and 0x0F. The bit corresponding to the input to be inverted needs to be set to a 1.

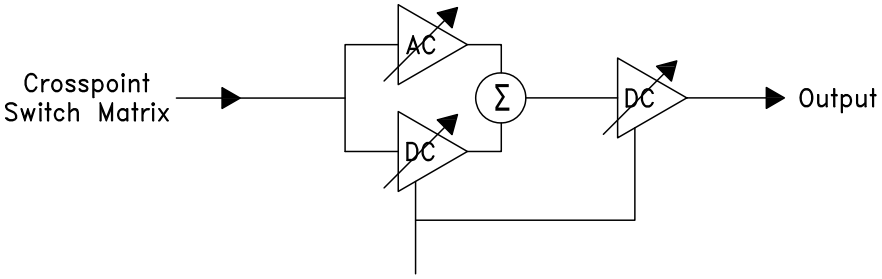
Table 9. Reg 0x0E-0x0F Output Polarity Registers

Name	Reg	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit 2	Bit 1	Bit 0
Output_Pol_B	0x0E	R/W	0x00	Ch12	RSV	RSV	RSV	Ch11	Ch10	Ch9	Ch8
Output_Pol_A	0x0F	R/W	0x00	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0

1 = inverted

0 = not inverted

Transmit De-emphasis



Each output channel has its own fully programmable De-emphasis and each independent De-emphasis is controlled by three registers. For example, Channel 0 is controlled by registers 0xC0, 0xC1 and 0xC2. The first register (0xC0) controls the PreDriver DC gain of the transmitter. The second register (0xC1) controls the PreDriver AC gain of the transmitter. Register three (0xC2) controls the DC gain of the output driver. The programmable output De-emphasis is capable of up to 12 dB of control.

Table 10. Channel De-emphasis Control Registers

Name	Reg Addr(s)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit 2	Bit 1	Bit 0
PRE_DV_DC	0xC0,0xC4,0xC8,0xCC, 0xD0,0xD4,0xD8,0xDC, 0xE0,0xE4,0xE8,0xEC, 0xFC	Not Used	Not Used	Pre-Driver DC Gain					
PRE_DV_DE	0xC1,0xC5,0xC9,0xCD, 0xD1,0xD5,0xD9,0xDD, 0xE1,0xE5,0xE9,0xED, 0xFD	Not Used	Not Used	Pre-Driver AC Gain					
OUT_DV_DC	0xC2,0xC6,0xCA,0xCE, 0xD2,0xD6,0xDA,0xDE, 0xE2,0xE6,0xEA,0xEE, 0xFE	Not Used	Not Used	Output Driver DC Gain					

14.2 GBPS 13X13 ASYNCHRONOUS CROSSPOINT SWITCH WITH EQUALIZATION AND DE-EMPHASIS

Typical Operation

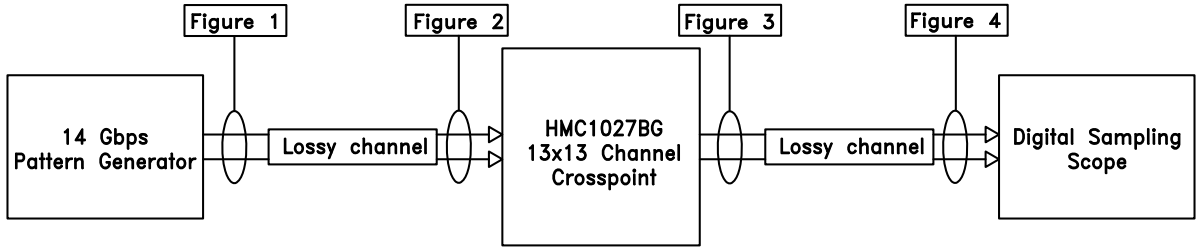


Figure 1

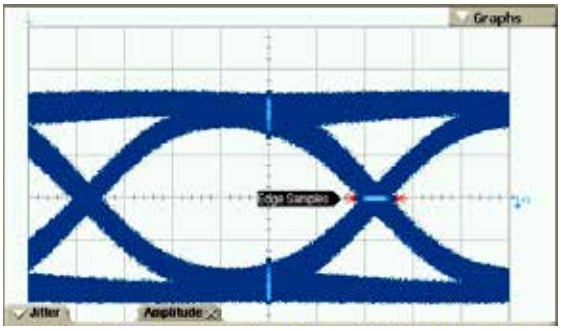


Figure 2

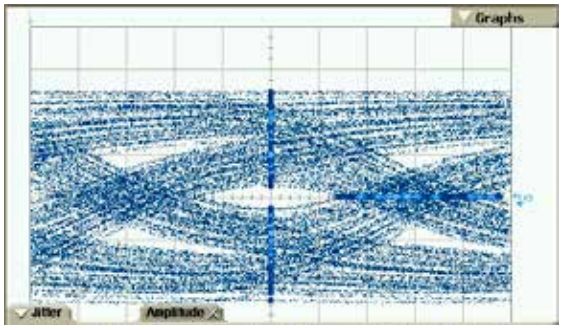


Figure 3

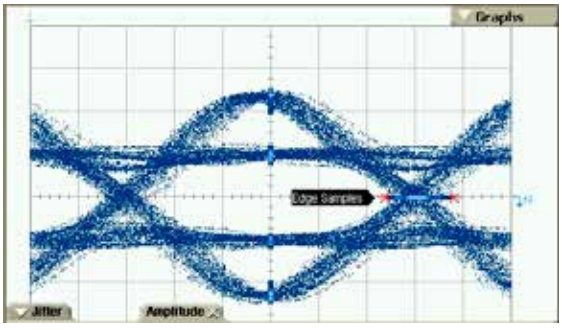
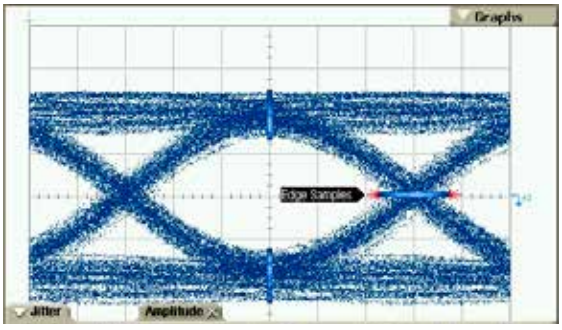


Figure 4



Two-Wire Serial Port

To access all its internal registers, the HMC1027BG uses a two-wire interface, which consists of a Serial Data Line (SDA) and a Serial Clock Line (SCL). Both SDA and SCL are implemented with open-drain I/O pins and are connected to a positive supply voltage via pull-up resistors. The value of these external resistors must be between 2 KΩ and 19 KΩ.

Typically, a microcontroller, a microprocessor or a digital signal processor acts as a master, controls the bus and has the responsibility to generate the clock signal and device addresses.

The HMC1027BG functions as a slave device and can transmit and receive data at a maximum rate of 800 Kbps. The device address on the HMC1027BG is set by connecting each chip address pin CA[6:0] to either VCC (logic 1) or GND (logic 0).

Protocol

The following are some definitions and conditions occurring in a two-wire data transfer.

START condition: is always generated by the master and is defined as a High to Low transition on the SDA line while SCL is High. The bus becomes busy after a START condition.

STOP condition: is always generated by the master and is defined as a Low to High transition on the SDA line while SCL is High. The bus becomes free after the STOP condition occurs.

Byte format: every byte transmitted on SDA must be 8 bits long and is transferred with the Most Significant Bit (MSB) first. Each byte must be followed by an Acknowledge (ACK) bit.

Data Valid condition: for data to be considered valid, the SDA line must be stable during the entire high period of its respective clock pulse.

Acknowledge: for each byte sent or received on the bus the master generates an extra clock cycle that is used for acknowledgement, for a total of 9 bits. The transmitter releases the SDA line, which is pulled High by the external resistor, and the receiver must pull down the SDA line and drive it Low while SCL is High in this entire clock cycle (data valid) to indicate acknowledgment. SDA is left High during this clock cycle to indicate a Not-acknowledge situation, usually because the device addressed is unable to receive or transmit the data requested.

Figure 5 shows a representation of a complete communication cycle on the two wire interface.

The master generates a Start condition to indicate the beginning of a new data transfer.

The master then starts generating clock pulses on SCL and transmits the first byte on SDA. This first byte always consists of a 7-bit slave address followed by 1 bit that indicates the Read/Write direction (R/$\overline{W}$). The device on the bus with a matching address generates an acknowledge.

The master continues generating more clock pulses on SCL and, depending on the value of the R/$\overline{W}$ bit, it sends (Write operation, R/$\overline{W}$ bit set to 0) or receives (Read operation, R/$\overline{W}$ bit set to 1) data on SDA. In each case the receiver must acknowledge the data sent by the transmitter. This sequence of 8-bit data followed by a 1-bit acknowledge may be repeated multiple times.

When all data communication is over for the current transfer cycle the master indicates the end of data transfer by generating a Stop condition.

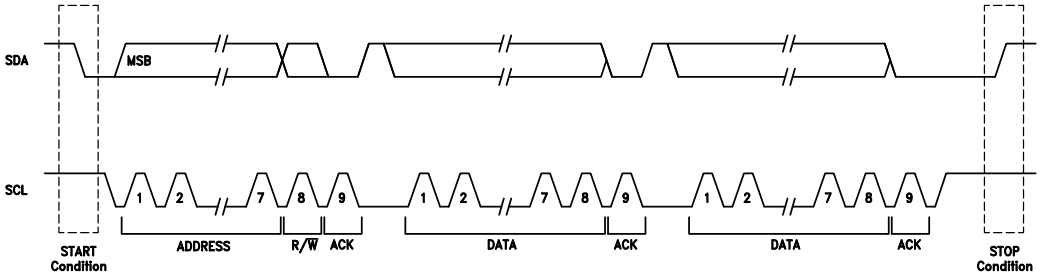


Figure 5. Complete data transfer.

Data Transfer Formats

1. **Write Cycle** (master transmitter sends data to slave receiver. See Figure 6): the transfer direction is from Master to Slave and does not change. The master generates a Start condition followed by a 7-bit slave address followed by the R//$\overline{W}$ bit set to 0. The slave with a matching address replies with an acknowledge. The master then transmits the first byte to the slave device, this first byte is an address of the internal registers of the slave. The slave device replies with an acknowledge bit. The master then transmits the next byte, which is now a data byte to be stored in the internal slave register previously addressed. This is followed by an acknowledge bit from the slave. This process can continue for multiple bytes and the slave device increments its internal register address count as it receives subsequent bytes from the master. When all data transfer is over, the master generates a Stop condition to end the cycle.

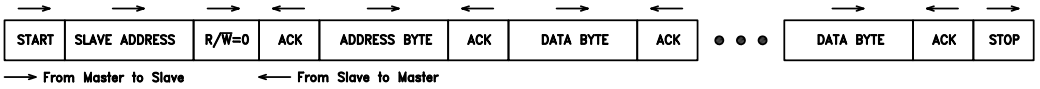


Figure 6. Master transmitter writes to slave receiver.

2. **Write/Read Cycle** (master writes to slave and then reads from slave. See Figure 7): after addressing the slave with the R/$\overline{W}$ set to 0, the master sends the first byte indicating the internal register address of the slave device where the first data byte is to be read. The master then generates a new Start condition, also known as a Repeated Start dondition and addresses the slave device again, this time followed by the R/$\overline{W}$ bit set to 1. The slave replies with an acknowledge bit, followed by the first data byte. Now the master must in turn reply with an ACK if more data bytes are to be read from the slave or with a NACK followed by a Stop condition to indicate the end of the Write/Read cycle.

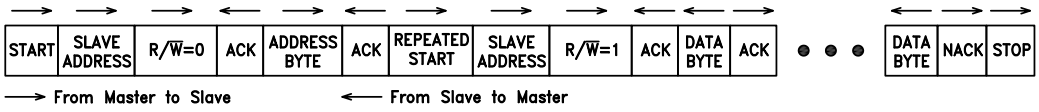


Figure 7. Master reads from slave.

Table 11. 13x13 Crosspoint Switch Register Map Summary

Address	Register Name	Type	Default Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit 2	Bit 1	Bit 0
0x00	Chip_ID[3:0]	RO	0xC3	0xC3964000 is the Chip ID for HMC1027BG							
0x01			0x96								
0x02			0x40								
0x03			0x00								
0x04	Unlock	R/W	0x00	Unlock Register							
0x05	Rsvd_05		0x00	RESERVED							
0x06	SW_RST	R/W	0x00	Software Reset							
0x07	Rsvd_07		0xFF	RESERVED							
0x08	EQ_EN_B	R/W	0xFF	Ch12	RESERVED			Ch11	Ch10	Ch9	Ch8
0x09	EQ_EN_A			Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0
0x0A	De_Emph_B	R/W	0xFF	Ch12	RESERVED			Ch11	Ch10	Ch9	Ch8
0x0B	De_Emph_A			Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0
0x0C	Input_Pol_B	R/W	0x00	Ch12	RESERVED			Ch11	Ch10	Ch9	Ch8
0x0D	Input_Pol_A			Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0
0x0E	Output_Pol_B	R/W	0x00	Ch12	RESERVED			Ch11	Ch10	Ch9	Ch8
0x0F	Output_Pol_A			Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0
0x10	Input_EN_B	R/W	0x00	Ch12	RESERVED			Ch11	Ch10	Ch9	Ch8
0x11	Input_EN_A			Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0
0x12	Output_EN_B	R/W	0x00	Ch12	RESERVED			Ch11	Ch10	Ch9	Ch8
0x13	Output_EN_A			Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0
0x14 - 0x17	Rsvd_14 - Rsvd_17		0x3F	RESERVED							
0x18	Rsvd_18	R/W	0x78	RESERVED							
0x19	Rsvd_19		0x80	RESERVED, Set to 0x40							
0x1A	Rsvd_1A		0x00	RESERVED, Set to 0x3F							
0x1B - 0x1F	Rsvd_1B - Rsvd_1F		0x00	RESERVED							
0x20	Input_Sel0	R/W	0x00	Input Select for Channel 0							
0x21	Input_Sel1			Input Select for Channel 1							
0x22	Input_Sel2			Input Select for Channel 2							
0x23	Input_Sel3			Input Select for Channel 3							
0x24	Input_Sel4			Input Select for Channel 4							
0x25	Input_Sel5			Input Select for Channel 5							
0x26	Input_Sel6			Input Select for Channel 6							
0x27	Input_Sel7			Input Select for Channel 7							
0x28	Input_Sel8			Input Select for Channel 8							
0x29	Input_Sel9			Input Select for Channel 9							
0x2A	Input_Sel10			Input Select for Channel 10							
0x2B	Input_Sel11			Input Select for Channel 11							
0x2C - 0x2E	Rsvd_2C - Rsvd_2E		0x00	RESERVED							
0x2F	Input_Sel12	R/W	0x00	Input Select for Channel 12							
0x30 - 0x7F	Rsvd_30 - Rsvd_7F		0x00	RESERVED							
0x80	EQ0_Byp_DC	R/W	0x9D	Ch0 EQ Bypass/EN		Ch0 EQ DC Gain					
0x81	EQ0_Offs_AC		0x1B	RSV	Ch0 EQ Offset	Ch0 EQ AC Gain					
0x82 - 0x83	Rsvd_82 - Rsvd_83		0x00	RESERVED							

Table 11. 13x13 Crosspoint Switch Register Map Summary (continued)

Address	Register Name	Type	Default Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit 2	Bit 1	Bit 0
0x84	EQ1_Byp_DC	R/W	0x9D	Ch1 EQ Bypass/EN		Ch1 EQ DC Gain					
0x85	EQ1_Offs_AC		0x1B	RSV	Ch1 EQ Offset	Ch1 EQ AC Gain					
0x86 - 0x87	Rsvd_86 - Rsvd_87		0x00	RESERVED							
0x88	EQ2_Byp_DC	R/W	0x9D	Ch2 EQ Bypass/EN		Ch2 EQ DC Gain					
0x89	EQ2_Offs_AC		0x1B	RSV	Ch2 EQ Offset	Ch2 EQ AC Gain					
0x8A - 0x8B	Rsvd_8A - Rsvd_8B		0x00	RESERVED							
0x8C	EQ3_Byp_DC	R/W	0x9D	Ch3 EQ Bypass/EN		Ch3 EQ DC Gain					
0x8D	EQ3_Offs_AC		0x1B	RSV	Ch3 EQ Offset	Ch3 EQ AC Gain					
0x8E - 0x8F	Rsvd_8E - Rsvd_8F		0x00	RESERVED							
0x90	EQ4_Byp_DC	R/W	0x9D	Ch4 EQ Bypass/EN		Ch4 EQ DC Gain					
0x91	EQ4_Offs_AC		0x1B	RSV	Ch4 EQ Offset	Ch4 EQ AC Gain					
0x92 - 0x93	Rsvd_92 - Rsvd_93		0x00	RESERVED							
0x94	EQ5_Byp_DC	R/W	0x9D	Ch5 EQ Bypass/EN		Ch5 EQ DC Gain					
0x95	EQ5_Offs_AC		0x1B	RSV	Ch5 EQ Offset	Ch5 EQ AC Gain					
0x96 - 0x97	Rsvd_96 - Rsvd_97		0x00	RESERVED							
0x98	EQ6_Byp_DC	R/W	0x9D	Ch6 EQ Bypass/EN		Ch6 EQ DC Gain					
0x99	EQ6_Offs_AC		0x1B	RSV	Ch6 EQ Offset	Ch6 EQ AC Gain					
0x9A - 0x9B	Rsvd_9A - Rsvd_9B		0x00	RESERVED							
0x9C	EQ7_Byp_DC	R/W	0x9D	Ch7 EQ Bypass/EN		Ch7 EQ DC Gain					
0x9D	EQ7_Offs_AC		0x1B	RSV	Ch7 EQ Offset	Ch7 EQ AC Gain					
0x9E - 0x9F	Rsvd_9E - Rsvd_9F		0x00	RESERVED							
0xA0	EQ8_Byp_DC	R/W	0x9D	Ch8 EQ Bypass/EN		Ch8 EQ DC Gain					
0xA1	EQ8_Offs_AC		0x1B	RSV	Ch8 EQ Offset	Ch8 EQ AC Gain					
0xA2 - 0xA3	Rsvd_A2 - Rsvd_A3		0x00	RESERVED							
0xA4	EQ9_Byp_DC	R/W	0x9D	Ch9 EQ Bypass/EN		Ch9 EQ DC Gain					
0xA5	EQ9_Offs_AC		0x1B	RSV	Ch9 EQ Offset	Ch9 EQ AC Gain					
0xA6 - 0xA7	Rsvd_A6 - Rsvd_A7		0x00	RESERVED							
0xA8	EQ10_Byp_DC	R/W	0x9D	Ch10 EQ Bypass/EN		Ch10 EQ DC Gain					
0xA9	EQ10_Offs_AC		0x1B	RSV	Ch10 EQ Offset	Ch10 EQ AC Gain					
0xAA - 0xAB	Rsvd_AA - Rsvd_AB		0x00	RESERVED							
0xAC	EQ11_Byp_DC	R/W	0x9D	Ch11 EQ Bypass/EN		Ch11 EQ DC Gain					
0xAD	EQ11_Offs_AC		0x1B	RSV	Ch11 EQ Offset	Ch11 EQ AC Gain					
0xAE - 0xBB	Rsvd_AE - Rsvd_BB		0x00	RESERVED							
0xBC	EQ12_Byp_DC	R/W	0x9D	Ch12 EQ Bypass/EN		Ch12 EQ DC Gain					
0xBD	EQ12_Offs_AC		0x1B	RSV	Ch12 EQ Offset	Ch12 EQ AC Gain					

Table 11. 13x13 Crosspoint Switch Register Map Summary (continued)

Address	Register Name	Type	Default Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit 2	Bit 1	Bit 0
0xBE - 0xBF	Rsvd_BE - Rsvd_BF		0x00	RESERVED							
0xC0	CH0_PRE_DV_DC	R/W	0x18	RESERVED		Ch0 Pre-Driver DC Gain					
0xC1	CH0_PRE_DV_DE		0x00			Ch0 Pre-Driver AC Gain					
0xC2	CH0_OUT_DV_DC		0x28			Ch0 Output Driver DC Gain					
0xC3	Rsvd_C3		0x00	RESERVED, Set to 0x35							
0xC4	CH1_PRE_DV_DC	R/W	0x18	RESERVED		Ch1 Pre-Driver DC Gain					
0xC5	CH1_PRE_DV_DE		0x00			Ch1 Pre-Driver AC Gain					
0xC6	CH1_OUT_DV_DC		0x28			Ch1 Output Driver DC Gain					
0xC7	Rsvd_C7		0x00	RESERVED, Set to 0x35							
0xC8	CH2_PRE_DV_DC	R/W	0x18	RESERVED		Ch2 Pre-Driver DC Gain					
0xC9	CH2_PRE_DV_DE		0x00			Ch2 Pre-Driver AC Gain					
0xCA	CH2_OUT_DV_DC		0x28			Ch2 Output Driver DC Gain					
0xCB	Rsvd_CB		0x00	RESERVED, Set to 0x35							
0xCC	CH3_PRE_DV_DC	R/W	0x18	RESERVED		Ch3 Pre-Driver DC Gain					
0xCD	CH3_PRE_DV_DE		0x00			Ch3 Pre-Driver AC Gain					
0xCE	CH3_OUT_DV_DC		0x28			Ch3 Output Driver DC Gain					
0xCF	Rsvd_CF		0x00	RESERVED, Set to 0x35							
0xD0	CH4_PRE_DV_DC	R/W	0x18	RESERVED		Ch4 Pre-Driver DC Gain					
0xD1	CH4_PRE_DV_DE		0x00			Ch4 Pre-Driver AC Gain					
0xD2	CH4_OUT_DV_DC		0x28			Ch4 Output Driver DC Gain					
0xD3	Rsvd_D3		0x00	RESERVED, Set to 0x35							
0xD4	CH5_PRE_DV_DC	R/W	0x18	RESERVED		Ch5 Pre-Driver DC Gain					
0xD5	CH5_PRE_DV_DE		0x00			Ch5 Pre-Driver AC Gain					
0xD6	CH5_OUT_DV_DC		0x28			Ch5 Output Driver DC Gain					
0xD7	Rsvd_D7		0x00	RESERVED, Set to 0x35							
0xD8	CH6_PRE_DV_DC	R/W	0x18	RESERVED		Ch6 Pre-Driver DC Gain					
0xD9	CH6_PRE_DV_DE		0x00			Ch6 Pre-Driver AC Gain					
0xDA	CH6_OUT_DV_DC		0x28			Ch6 Output Driver DC Gain					
0xDB	Rsvd_DB		0x00	RESERVED, Set to 0x35							
0xDC	CH7_PRE_DV_DC	R/W	0x18	RESERVED		Ch7 Pre-Driver DC Gain					
0xDD	CH7_PRE_DV_DE		0x00			Ch7 Pre-Driver AC Gain					
0xDE	CH7_OUT_DV_DC		0x28			Ch7 Output Driver DC Gain					
0xDF	Rsvd_DF		0x00	RESERVED, Set to 0x35							
0xE0	CH8_PRE_DV_DC	R/W	0x18	RESERVED		Ch8 Pre-Driver DC Gain					
0xE1	CH8_PRE_DV_DE		0x00			Ch8 Pre-Driver AC Gain					
0xE2	CH8_OUT_DV_DC		0x28			Ch8 Output Driver DC Gain					
0xE3	Rsvd_E3		0x00	RESERVED, Set to 0x35							
0xE4	CH9_PRE_DV_DC	R/W	0x18	RESERVED		Ch9 Pre-Driver DC Gain					
0xE5	CH9_PRE_DV_DE		0x00			Ch9 Pre-Driver AC Gain					
0xE6	CH9_OUT_DV_DC		0x28			Ch9 Output Driver DC Gain					
0xE7	Rsvd_E7		0x00	RESERVED, Set to 0x35							
0xE8	CH10_PRE_DV_DC	R/W	0x18	RESERVED		Ch10 Pre-Driver DC Gain					
0xE9	CH10_PRE_DV_DE		0x00			Ch10 Pre-Driver AC Gain					
0xEA	CH10_OUT_DV_DC		0x28			Ch10 Output Driver DC Gain					

Table 11. 13x13 Crosspoint Switch Register Map Summary (continued)

Address	Register Name	Type	Default Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit 2	Bit 1	Bit 0
0xEB	Rsvd_EB		0x00	RESERVED, Set to 0x35							
0xEC	CH11_PRE_DV_DC	R/W	0x18	RESERVED		Ch11 Pre-Driver DC Gain					
0xED	CH11_PRE_DV_DE		0x00			Ch11 Pre-Driver AC Gain					
0xEE	CH11_OUT_DV_DC		0x28			Ch11 Output Driver DC Gain					
0xEF - 0xFB	Rsvd_EF - Rsvd_FB	0x00		RESERVED, Set to 0x35							
0xFC	CH12_PRE_DV_DC	R/W	0x18	RESERVED		Ch12 Pre-Driver DC Gain					
0xFD	CH12_PRE_DV_DE		0x00			Ch12 Pre-Driver AC Gain					
0xFE	CH12_OUT_DV_DC		0x28			Ch12 Output Driver DC Gain					
0xFF	Rsvd_FF		0x00	RESERVED, Set to 0x35							

Evaluation Board

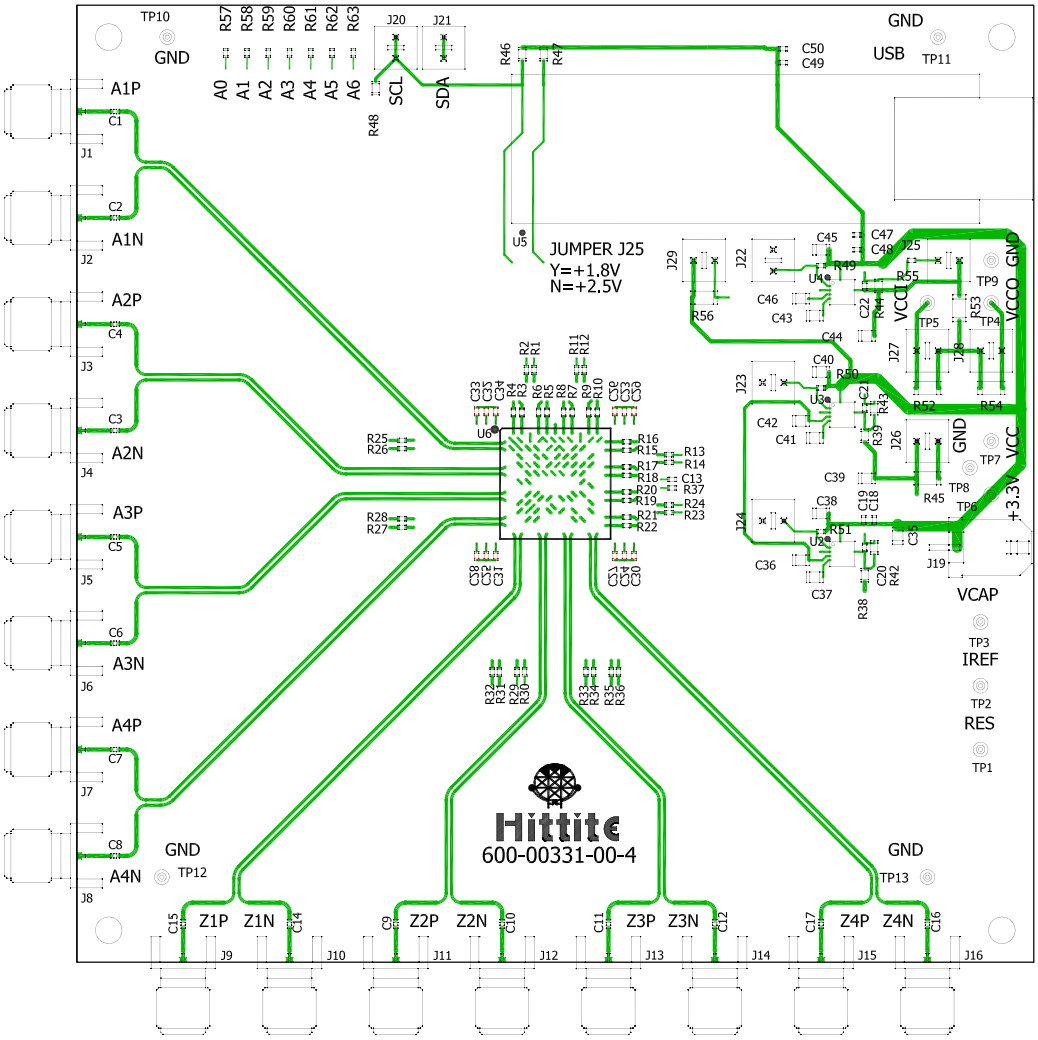


Table 12. Evaluation Order Information

Item	Contents	Part Number
Evaluation Kit	HMC1027BG Evaluation PCB 6' USB A Male to USB B Female Cable Power Supply Cable CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software	EKIT01-HMC1027BG