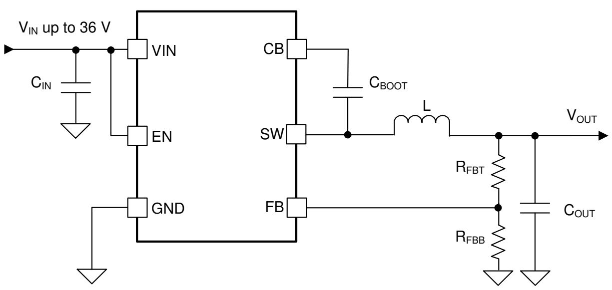
LV3842 4-V to 36-V, 600-mA, Synchronous Step-Down Converter

1 Features

- New product available:
  - LMR54406 4-V to 45-V, 0.6-A, 1.1-MHz synchronous buck converter
- For faster time to market:
  - TPSM365R6 3-V to 65-V, 0.6-A, 200-kHz to 2.2-MHz power module
- Configured for rugged industrial applications
  - 4-V to 36-V input voltage range supporting 40-V absolute maximum rating
  - 600-mA continuous output current
  - 70-ns minimum switching-on time
  - 98% maximum duty cycle
  - PFM and Forced PWM (FPWM) options
  - 1.1-MHz switching frequency
  - Support start-up with pre-biased output
  - Short-circuit protection with hiccup mode
  - ±0.5% tolerance voltage reference at 25°C junction temperature
  - Precision enable
  - Overtemperature protection
- Small solution size and ease of use
  - Integrated synchronous rectification
  - Internal compensation for ease of use
  - SOT-23-6 package

2 Applications

- Electricity meter
- Smart meter data collector, concentrator
- Power Line Communication (PLC) module
- General purpose wide V_{IN} power supplies



Typical Application Schematic

3 Description

The LV3842 is an easy to use synchronous step-down DC-DC converter capable of driving up to 600-mA load current. With a wide input range of 4 V to 36 V, the device is designed for a wide range of industrial applications for power conditioning from an unregulated source.

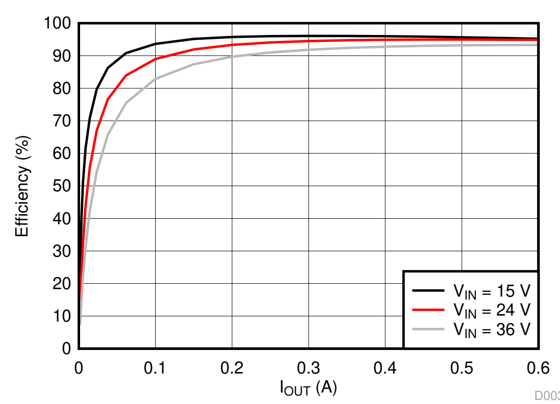
The LV3842 employs 1.1-MHz switching frequency for small solution size. The LV3842 also has FPWM (forced PWM) version to achieve constant frequency and small output voltage ripple over the full load range. Soft-start and compensation circuits are employed internally which allows the device to be used with minimum external components.

The device has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, and thermal shutdown in case of excessive power dissipation. The LV3842 is available in SOT-23-6 package.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LV3842	DBV (SOT-23, 6)	2.90 mm × 2.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Efficiency vs Output Current V_{OUT} = 12 V, 1.1 MHz, FPWM

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2019) to Revision C (August 2023) — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document 1
- Changed document status from Advance Information to Production Data....1
- First public release....1

5 Device Comparison Table

PART NUMBER	Frequency	PFM or FPWM	Output
LV3842XF	1.1 MHz	FPWM	Adjustable
LV3842X	1.1 MHz	PFM	Adjustable

6 Pin Configuration and Functions

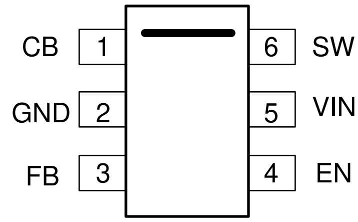


Figure 6-1. DBV Package 6-Pin SOT-23-6 Top View

Table 6-1. Pin Functions

PIN		TYPE [(1)]	DESCRIPTION
NO.	NAME		
1	CB	P	Bootstrap capacitor connection for high-side FET driver. Connect a high quality 100 nF capacitor from this pin to the SW pin.
2	GND	G	Power ground terminal, connected to the source of low-side FET internally. Connect to system ground, ground side of C_{IN} and C_{OUT}. Path to C_{IN} must be as short as possible.
3	FB	A	Feedback input to the convertor. Connect a resistor divider to set the output voltage. Never short this terminal to ground during operation.
4	EN	A	Precision enable input to the convertor. Do not float. High = on, Low = off. Can be tied to VIN. Precision enable input allows adjustable UVLO by external resistor divider.
5	VIN	P	Supply input terminal to internal bias LDO and high-side FET. Connect to input supply and input bypass capacitors C_{IN}. Input bypass capacitors must be directly connected to this pin and GND.
6	SW	P	Switching output of the convertor. Internally connected to source of the high-side FET and drain of the low-side FET. Connect to power inductor.

(1) A = Analog, P = Power, G = Ground.

7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of -40 °C to 125 °C (unless otherwise noted) [(1)]

PARAMETER		MIN	MAX	UNIT
Input Voltages	VIN to GND	–0.3	40	V
	EN to GND	–0.3	V_{IN} + 0.3	
	FB to GND	–0.3	5.5	
Output Voltages	SW to GND	–0.3	V_{IN} + 0.3	V
	SW to GND less than 10 ns transient	–3.5	40	
	CB to SW	–0.3	5.5	
T_J	Junction temperature [(2)]	–40	150	°C
T_{stg}	Storage temperature	–65	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Operating at junction temperatures greater than 125°C, although possible, degrades the lifetime of the device.

7.2 ESD Ratings

PARAMETER	DEFINITION		VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	± 2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	± 750	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of -40 °C to 125 °C (unless otherwise noted) [(1)]

PARAMETER		MIN	MAX	UNIT
Input Voltages	VIN to GND	4	36	V
	EN	0	V_{IN}	
	FB	0	4.5	
Output Voltage	V_{OUT}	1.0	95% of V_{IN}	V
Output Current	I_{OUT}	0	600	mA
Temperature	Operating junction temperature range, T_J	–40	+125	°C

(1) *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but do not verify specific performance limits. For verified specifications, see *Electrical Characteristics*.

7.4 Thermal Information

THERMAL METRIC [(1)] [(2)]		DBV (6 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	173	°C/W
$R_{\theta JC\_T}$	Junction-to-case (TOP) thermal resistance	116	°C/W
$R_{\theta JC\_B}$	Junction-to-case (BOTTOM) thermal resistance	31	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	20	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	30	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953

(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application

7.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25 °C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 4 V to 36 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
V_{IN}	Operation input voltage		4		36	V
V_{IN_UVLO}	Undervoltage lockout thresholds	Rising threshold	3.55	3.75	4.00	V
		Falling threshold	3.25	3.45	3.65	
		Hysteresis		0.3		
I_Q	Operating quiescent current (non-switching)	PFM version, V_{EN} = 3.3 V, V_{FB} = 1.1V		80	120	µA
I_{SHDN}	Shutdown current			3	10	µA
ENABLE (EN PIN)						
V_{EN_H}	Enable rising threshold voltage		1.1	1.23	1.36	V
V_{EN_L}	Enable falling threshold voltage		0.95	1.1	1.22	V
V_{EN_HYS}	Enable hysteresis voltage			0.13		V
I_{EN}	Leakage current at EN pin	V_{EN} = 3.3 V		10	200	nA
VOLTAGE REFERENCE (FB PIN)						
V_{REF}	Reference voltage	T_J = 25 °C	0.995	1.00	1.005	V
		T_J = –40°C to 125°C	0.98	1.00	1.02	V
I_{FB}	Leakage current at FB pin	V_{FB} = 1.2 V		0.2	50	nA
CURRENT LIMITS AND HICCUP						
I_{HS_LIMIT}	Peak inductor current limit			1.1		A
I_{LS_LIMIT}	Valley inductor current limit			0.8		A
I_{LS_ZC}	Zero cross current (PFM version)			20		mA
I_{LS_NEG}	Negative current limit (FPWM version)			–0.5		A
V_{HICCUP}	Hiccup threshold of FB pin	% of reference voltage		40%		
INTEGRATED MOSFETS						
$R_{DS\_ON\_HS}$	High-side MOSFET ON-resistance	T_J = 25°C		550		mΩ
$R_{DS\_ON\_LS}$	Low-side MOSFET ON-resistance	T_J = 25°C		285		mΩ
THERMAL SHUTDOWN [1]						
T_{SHDN}	Thermal shutdown threshold			170		°C
T_{HYS}	Hysteresis			12		°C

(1) Specified by design.

7.6 Timing Requirements

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25 °C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 4 V to 36 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT START						
t_{SS}	Internal soft-start time	The time of internal reference to increase from 10% to 90% of V_{REF}, V_{IN} = 12 V		1.8		ms
HICCUP Protection						
T_{HICCUP}	Hiccup time	V_{IN} = 12 V		135		ms

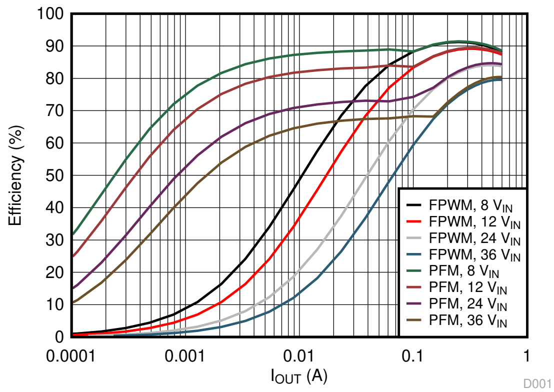
7.7 Switching Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25 °C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 4 V to 36 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING NODE (SW PIN)						
t_{ON_MIN}	Minimum turn-on time	I_{OUT} = 600 mA		70		ns
t_{OFF_MIN}	Minimum turn-off time	I_{OUT} = 600 mA		100		ns
t_{ON_MAX}	Maximum turn-on time			7.5		µs
OSCILLATOR						
f_{SW}	Oscillator frequency		0.935	1.1	1.265	MHz

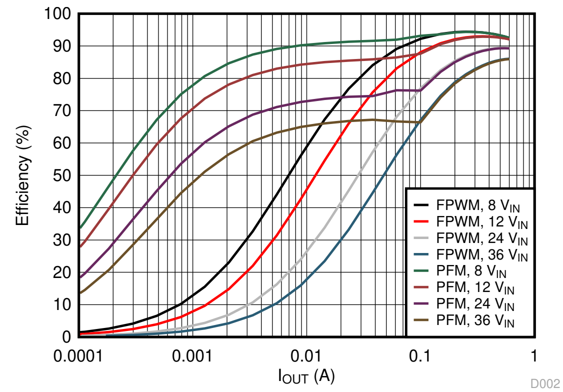
7.8 Typical Characteristics

V_{IN} = 12 V, f_{SW} = 1.1 MHz, T_A = 25°C, unless otherwise specified.



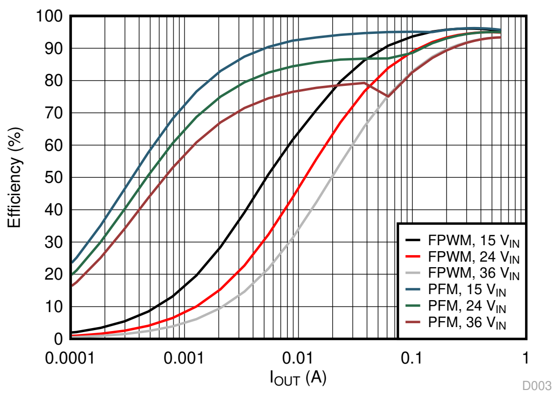
V_{OUT} = 3.3 V

Figure 7-1. Efficiency vs Load Current



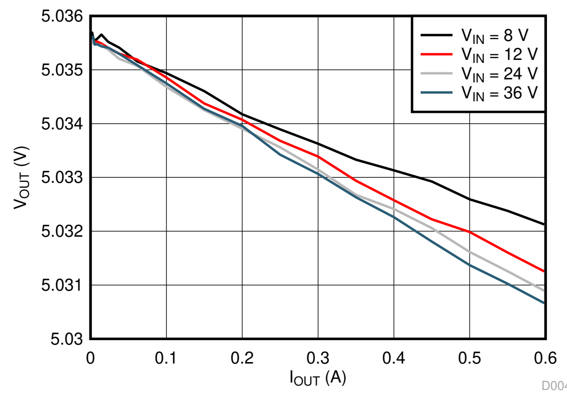
V_{OUT} = 5 V

Figure 7-2. Efficiency vs Load Current



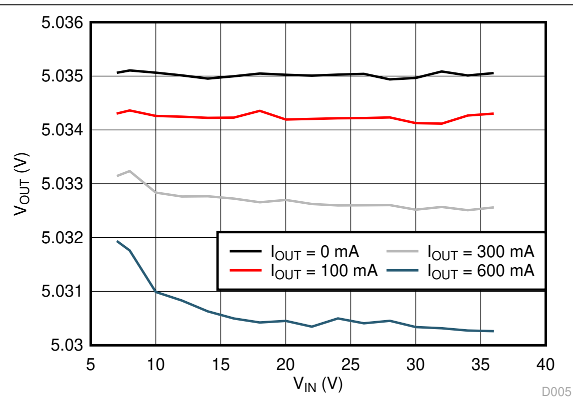
V_{OUT} = 12 V

Figure 7-3. Efficiency vs Load Current



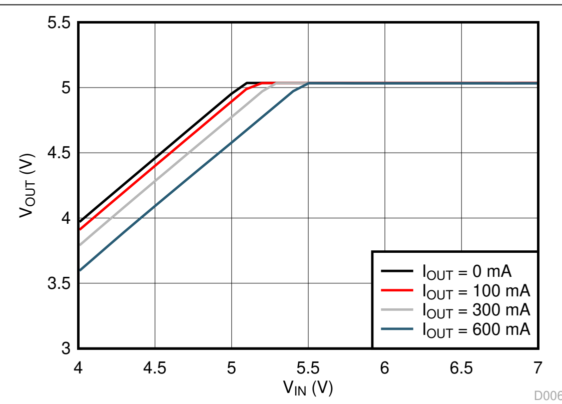
V_{OUT} = 5 V FPWM version

Figure 7-4. Load Regulation



V_{OUT} = 5 V FPWM version

Figure 7-5. Line Regulation

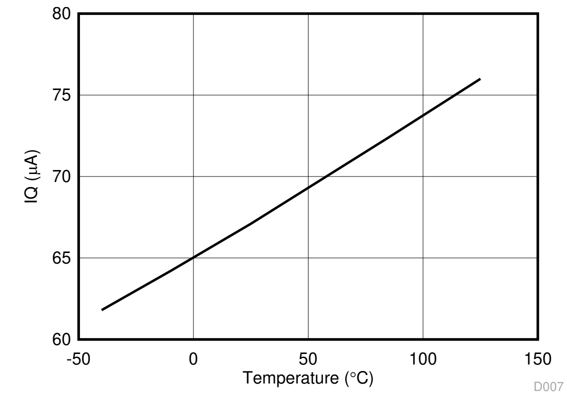


V_{OUT} = 5 V FPWM version

Figure 7-6. Dropout

7.8 Typical Characteristics (continued)

V_{IN} = 12 V, f_{SW} = 1.1 MHz, T_A = 25°C, unless otherwise specified.



V_{FB} = 1.1 V PFM verison

Figure 7-7. I_Q vs Temperature

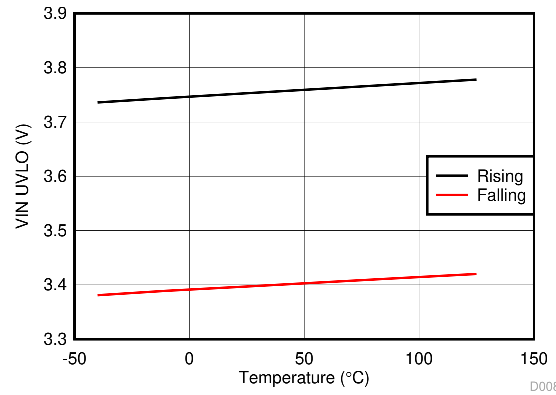


Figure 7-8. V_{IN} UVLO vs Temperature

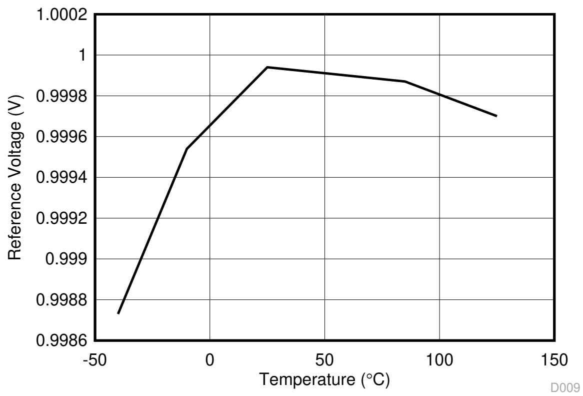


Figure 7-9. Reference Voltage vs Temperature

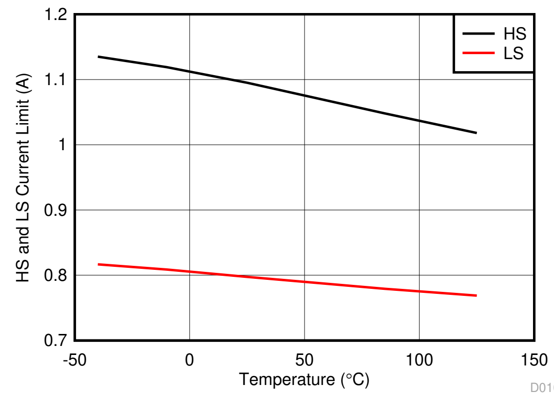


Figure 7-10. HS and LS Current Limit vs Temperature

8 Detailed Description

8.1 Overview

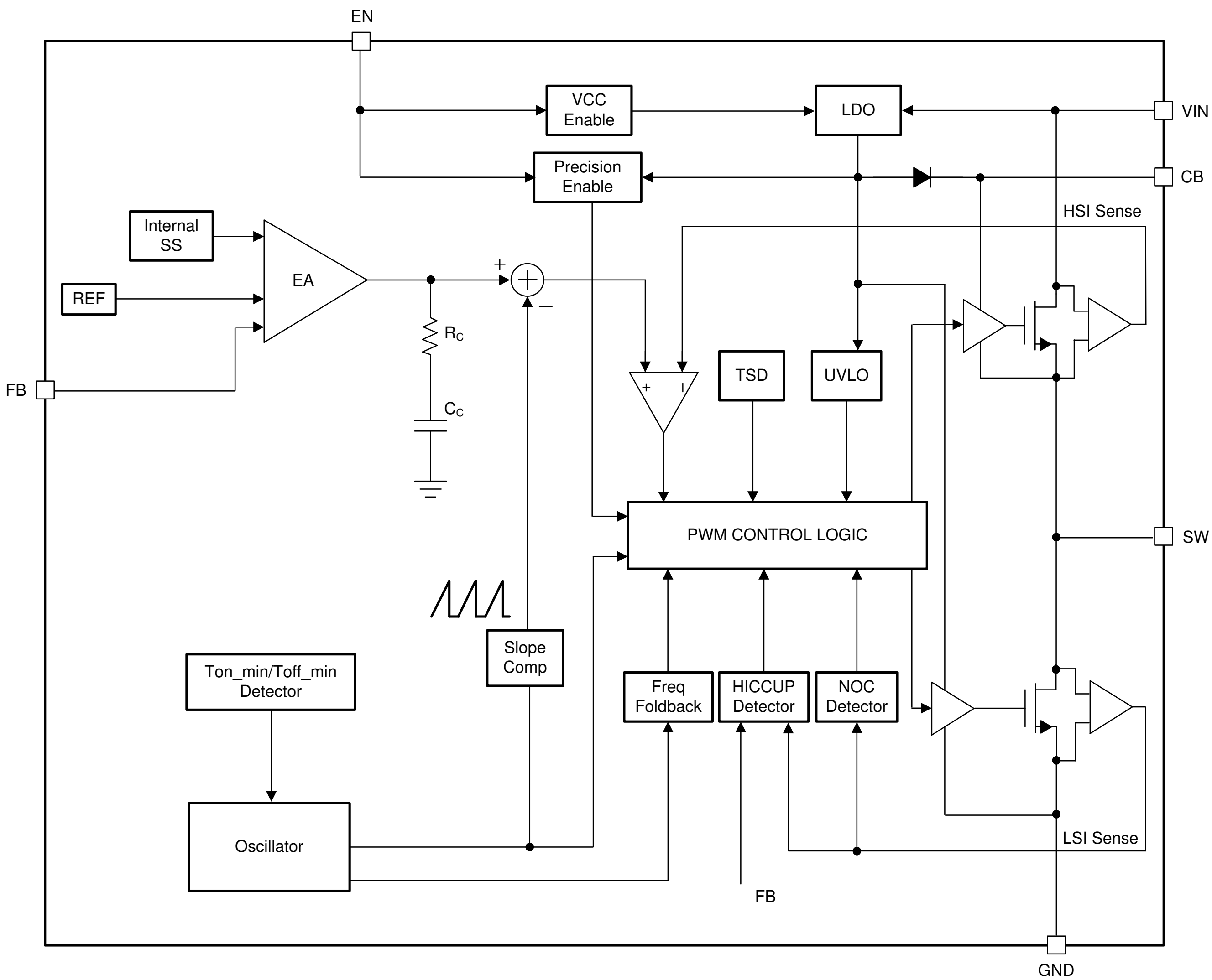
The LV3842 regulator is an easy to use synchronous step-down DC-DC converter operating from 4-V to 36-V supply voltage. The device is capable of delivering up to 600-mA DC load current in a very small solution size.

The LV3842 employs fixed-frequency peak-current mode control. The device enters PFM Mode at light load to achieve high efficiency for PFM version. And FPWM version is provided to achieve low output voltage ripple, tight output voltage regulation, and constant switching frequency at light load. The device is internally compensated, which reduces design time, and requires few external components.

Additional features such as precision enable and internal soft start provide a flexible and easy to use solution for a wide range of applications. Protection features include thermal shutdown, V_{IN} undervoltage lockout, cycle-by-cycle current limit, and hiccup mode short-circuit protection.

The LV3842 requires very few external components and has a pin-out designed for simple, optimum PCB layout.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fixed Frequency Peak Current Mode Control

The following operation description of the LV3842 will refer to the Section 8.2 and to the waveforms in Figure 8-1. LV3842 is a step-down synchronous buck regulator with integrated high-side (HS) and low-side (LS) switches (synchronous rectifier). The LV3842 supplies a regulated output voltage by turning on the HS and LS NMOS switches with controlled duty cycle. During high-side switch ON time, the SW pin voltage swings up to approximately V_{IN}, and the inductor current i_L increases with linear slope $(V_{IN} – V_{OUT}) / L$. When the HS switch is turned off by the control logic, the LS switch is turned on after an anti-shoot-through dead time. Inductor current discharges through the low-side switch with a slope of $–V_{OUT} / L$. The control parameter of a buck converter is defined as Duty Cycle $D = t_{ON} / T_{SW}$, where t_{ON} is the high-side switch ON time and T_{SW} is the switching period. The regulator control loop maintains a constant output voltage by adjusting the duty cycle D. In an idea Buck converter, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: $D = V_{OUT} / V_{IN}$.

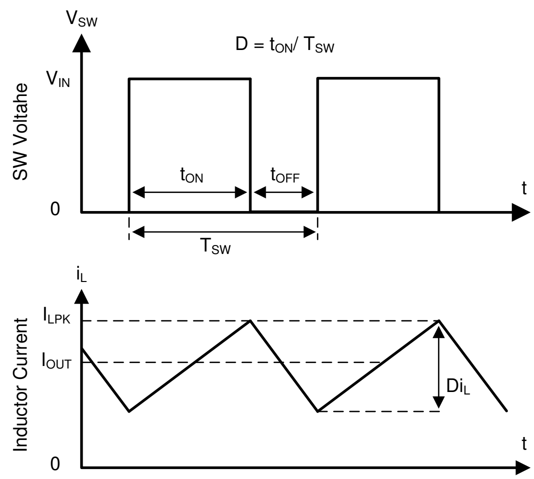


Figure 8-1. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

The LV3842 employs fixed-frequency peak-current mode control. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak-current command based on voltage offset. The peak inductor current is sensed from the high-side switch and compared to the peak current threshold to control the ON time of the high-side switch. The voltage feedback loop is internally compensated, which allows for fewer external components, makes it easy to design, and provides stable operation with almost any combination of output capacitors. The regulator operates with fixed switching frequency at normal conditions. At light-load condition, the LV3842 operates in PFM mode to maintain high efficiency (PFM version) or in FPWM mode for low output voltage ripple, tight output voltage regulation, and constant switching frequency (FPWM version).

8.3.2 Adjustable Output Voltage

A precision 1.0-V reference voltage V_{REF} is used to maintain a tightly regulated output voltage over the entire operating temperature range. The output voltage is set by a resistor divider from output voltage to the FB pin. TI recommends to use 1% tolerance resistors with a low temperature coefficient for the FB divider. Select the bottom-side resistor R_{FBB} for the desired divider current and use Equation 1 to calculate top-side resistor R_{FBT}. TI recommends R_{FBT} in the range from 10 kΩ to 100 kΩ for most applications. Lower R_{FBT} reduces efficiency at very light load. Less static current goes through a larger R_{FBT} and can be more desirable when light-load efficiency is critical. But TI does not recommend R_{FBT} larger than 1 MΩ because it makes the feedback path more susceptible to noise. Larger R_{FBT} value requires more carefully designed feedback path on the PCB. The tolerance and temperature variation of the resistor dividers affect the output voltage regulation.

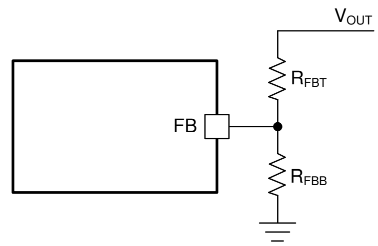


Figure 8-2. Output Voltage Setting

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (1)$$

8.3.3 Enable

The voltage on the EN pin controls the ON or OFF operation of LV3842 . A voltage of less than 0.95 V shuts down the device, while a voltage of more than 1.36 V is required to start the regulator. The EN pin is an input and cannot be left open or floating. The simplest way to enable the operation of the LV3842 is to connect the EN to VIN. This allows self-start-up of the LV3842 when V_{IN} is within the operating range.

Many applications benefit from the employment of an enable divider R_{ENT} and R_{ENB} (Figure 8-3) to establish a precision system UVLO level for the converter. System UVLO can be used for supplies operating from utility power as well as battery power. System UVLO can be used for sequencing, ensuring reliable operation, or supply protection, such as a battery discharge level. An external logic signal can also be used to drive EN input for system sequencing and protection. Note that the EN pin voltage must never be higher than V_{IN} + 0.3 V. TI does not recommend to apply EN voltage when V_{IN} is 0 V.

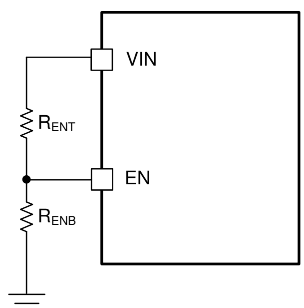


Figure 8-3. System UVLO by Enable Divider

8.3.4 Minimum ON-Time, Minimum OFF-Time and Frequency Foldback

Minimum ON-time, T_{ON_MIN}, is the smallest duration of time that the HS switch can be on. T_{ON_MIN} is typically 70 ns in the LV3842 . Minimum OFF-time, T_{OFF_MIN}, is the smallest duration that the HS switch can be off. T_{OFF_MIN} is typically 100 ns. In CCM operation, T_{ON_MIN} and T_{OFF_MIN} limit the voltage conversion ratio without switching frequency foldback.

The minimum duty cycle without frequency foldback allowed is

$$D_{MIN} = T_{ON\_MIN} \times f_{SW} \quad (2)$$

The maximum duty cycle without frequency foldback allowed is

$$D_{MAX} = 1 - T_{OFF\_MIN} \times f_{SW} \quad (3)$$

Given a required output voltage, the maximum V_{IN} without frequency foldback can be found by

$$V_{IN\_MAX} = \frac{V_{OUT}}{f_{SW} \times T_{ON\_MIN}} \tag{4}$$

The minimum V_{IN} without frequency foldback can be calculated by

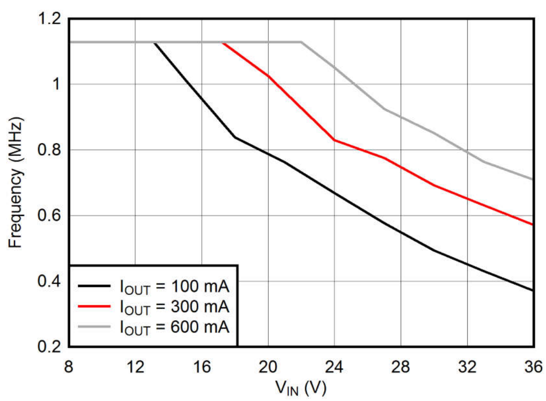
$$V_{IN\_MIN} = \frac{V_{OUT}}{1 - f_{SW} \times T_{OFF\_MIN}} \tag{5}$$

In the LV3842, a frequency foldback scheme is employed after the T_{ON_MIN} or T_{OFF_MIN} is triggered, which can extend the maximum duty cycle or lower the minimum duty cycle.

The on-time decreases while V_{IN} voltage increases. After the on-time decreases to T_{ON_MIN}, the switching frequency starts to decrease while V_{IN} continues to go up, which lowers the duty cycle further to keep V_{OUT} in regulation according to Equation 2.

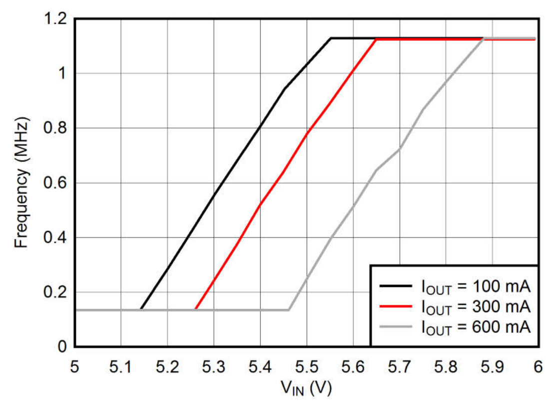
The frequency foldback scheme also works after larger duty cycle is needed under low V_{IN} conditions. The frequency decreases after the device hits its T_{OFF_MIN}, which extends the maximum duty cycle according to Equation 3. In such condition, the frequency can be as low as about 133-kHz minimum. Wide range of frequency foldback allows the LV3842 output voltage stay in regulation with a much lower supply voltage V_{IN}. This leads to a lower effective drop-out voltage.

With frequency foldback, V_{IN_MAX} is raised, and V_{IN_MIN} is lowered to overcome T_{ON_MIN} or T_{OFF_MIN} limitation.



V_{OUT} = 1 V

Figure 8-4. Frequency Foldback at T_{ON_MIN}



V_{OUT} = 5 V

Figure 8-5. Frequency Foldback at T_{OFF_MIN}

8.3.5 Bootstrap Voltage

The LV3842 provides an integrated bootstrap voltage regulator. A small capacitor between the CB and SW pins provides the gate drive voltage for the high-side MOSFET. The bootstrap capacitor is refreshed when the high-side MOSFET is off and the low-side switch conducts. The recommended value of the bootstrap capacitor is 0.1 µF. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 16 V or higher for stable performance over temperature and voltage.

8.3.6 Overcurrent and Short-Circuit Protection

The LV3842 is protected from overcurrent conditions by cycle-by-cycle current limit on both the peak and valley of the inductor current. Hiccup mode is activated if a fault condition persists to prevent over-heating.

High-side MOSFET overcurrent protection is implemented by the nature of the Peak Current Mode control. The HS switch current is sensed when the HS is turned on after a set blanking time. The HS switch current is compared to the output of the Error Amplifier (EA) minus slope compensation every switching cycle. Please refer to Section 8.2 for more details. The peak current of HS switch is limited by a clamped maximum peak current threshold I_{HS_LIMIT} which is constant.

The current going through LS MOSFET is also sensed and monitored. When the LS switch turns on, the inductor current begins to ramp down. The LS switch is not turned OFF at the end of a switching cycle if its current is above the LS current limit I_{LS_LIMIT}. The LS switch is kept ON so that inductor current keeps ramping down, until the inductor current ramps below the LS current limit I_{LS_LIMIT}. Then the LS switch is turned OFF and the HS switch is turned on after a dead time. This is somewhat different to the more typical peak current limit, and results in Equation 6 for the maximum load current.

$$I_{OUT\_MAX} = I_{LS} + \frac{\left(V_{IN} - V_{OUT}\right)}{2 \times f_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}} \tag{6}$$

If the feedback voltage is lower than 40% of the V_{REF}, the current of the LS switch triggers LS current limit for 256 consecutive cycles, hiccup current protection mode is activated. In hiccup mode, the regulator shuts down and keeps off for a period of hiccup, T_{HICCUP} (135-ms typical), before the LV3842 tries to start again. If overcurrent or short-circuit fault condition still exist, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe over-current conditions, prevents over-heating and potential damage to the device.

For FPWM version, the inductor current is allowed to go negative. If this current exceeds the LS negative current limit I_{LS_NEG}, the LS switch is turned off and HS switch is turned on immediately. This is used to protect the LS switch from excessive negative current.

8.3.7 Soft Start

The integrated soft-start circuit prevents input inrush current impacting the LV3842 and the input power supply. Soft-start is achieved by slowly ramping up the target regulation voltage when the device is first enabled or powered up. The typical soft-start time is 1.8 ms.

The LV3842 also employs over-current protection blanking time T_{OCP_BLK} (33 ms typical) at the beginning of power-up. Without this feature, in applications with a large amount of output capacitors and high V_{OUT}, the inrush current is large enough to trigger the current-limit protection, which can make the device entering into hiccup mode. The device tries to restart after the hiccup period, then hit current-limit and enter into hiccup mode again, so V_{OUT} cannot ramp up to the setting voltage ever. By introducing OCP blanking feature, the hiccup protection function is disabled during T_{OCP_BLK}, and LV3842 charges the V_{OUT} with its maximum limited current, which maximizes the output current capacity during this period. Kindly note that, the peak current limit (I_{HS_LIMIT}) and valley current limit (I_{LS_LIMIT}) protection function is still available during T_{OCP_BLK}, so there is no concern of inductor current running away.

8.3.8 Thermal Shutdown

The LV3842 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 170°C. Both HS and LS FETs stop switching in thermal shutdown. After the die temperature falls below 158°C, the device reinitiates the power up sequence controlled by the internal soft-start circuitry.

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control for the LV3842 . When V_{EN} is below 0.95 V, the device is in shutdown mode. The LV3842 also employs V_{IN} under voltage lock out (UVLO) protection. If V_{IN} voltage is below its UVLO threshold 3.25 V, the regulator is turned off.

8.4.2 Active Mode

The LV3842 is in Active Mode when both V_{EN} and V_{IN} are above their respective operating threshold. The simplest way to enable the LV3842 is to connect the EN pin to VIN pin. This allows self-startup when the input voltage is in the operating range: 4.0 V to 36 V. Please refer to Section 8.3.3 section for details on setting these operating levels.

In Active Mode, depending on the load current, the LV3842 will be in one of four modes:

1. Continuous conduction mode (CCM) with fixed switching frequency when load current is above half of the peak-to-peak inductor current ripple (for both PFM and FPWM versions).
2. Discontinuous conduction mode (DCM) with fixed switching frequency when load current is lower than half of the peak-to-peak inductor current ripple in CCM operation (only for PFM version).
3. Pulse frequency modulation mode (PFM) when switching frequency is decreased at very light load (only for PFM version).
4. Forced pulse width modulation mode (FPWM) with fixed switching frequency even at light load (only for FPWM version).

8.4.3 CCM Mode

Continuous Conduction Mode (CCM) operation is employed in the LV3842 when the load current is higher than half of the peak-to-peak inductor current. In CCM operation, the frequency of operation is fixed, output voltage ripple is at a minimum in this mode and the maximum output current of 600 mA can be supplied by the LV3842.

8.4.4 Light-Load Operation (PFM Version)

For PFM version, when the load current is lower than half of the peak-to-peak inductor current in CCM, the LV3842 operates in Discontinuous Conduction Mode (DCM), also known as Diode Emulation Mode (DEM). In DCM operation, the LS switch is turned off when the inductor current drops to I_{LS_ZC} (20 mA typical) to improve efficiency. Both switching losses and conduction losses are reduced in DCM, compared to forced PWM operation at light load.

At even lighter current load, Pulse Frequency Modulation (PFM) mode is activated to maintain high efficiency operation. When either the minimum HS switch ON time t_{ON_MIN} or the minimum peak inductor current I_{PEAK_MIN} (150mA typical) is reached, the switching frequency decreases to maintain regulation. In PFM mode, switching frequency is decreased by the control loop to maintain output voltage regulation when load current reduces. Switching loss is further reduced in PFM operation due to less frequent switching actions.

8.4.5 Light-Load Operation (FPWM Version)

For FPWM version, LV3842 is locked in PWM mode at full load range. This operation is maintained, even in no-load condition, by allowing the inductor current to reverse its normal direction. This mode trades off reduced light load efficiency for low output voltage ripple, tight output voltage regulation, and constant switching frequency.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LV3842 is a step down DC-to-DC regulator. The device is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 600 mA. The following design procedure can be used to select components for the LV3842.

9.2 Typical Application

The LV3842 only requires a few external components to convert from a wide voltage range supply to a fixed output voltage. Figure 9-1 shows a basic schematic.

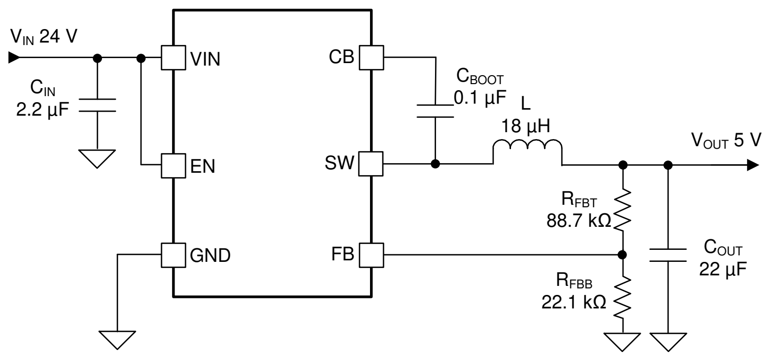


Figure 9-1. Application Circuit

The external components have to fulfill the needs of the application, but also the stability criteria of the device control loop. Table 9-1 can be used to simplify the output filter component selection.

Table 9-1. L and C_{OUT} Typical Values

f_{SW} (MHz)	V_{OUT} (V)	L (µH)	C_{OUT} (µF) (1)	R_{FBT} (kΩ)	R_{FBB} (kΩ)
1.1	3.3	12	22 µF / 10 V	51	22.1
	5	18	22 µF / 10 V	88.7	22.1
	12	33	10 µF / 25 V	243	22.1

(1) Ceramic capacitor is used in this table.

9.2.1 Design Requirements

Detailed design procedure is described based on a design example. For this design example, use the parameters listed in Table 9-2 as the input parameters.

Table 9-2. Design Example Parameters

PARAMETER	VALUE
Input voltage, V_{IN}	12 V typical, range from 6 V to 36 V
Output voltage, V_{OUT}	5 V ± 3%
Maximum output current, I_{OUT_MAX}	600 mA
Minimum output current, I_{OUT_MIN}	30 mA
Output overshoot/ undershoot (0mA to 600mA)	5%
Output voltage ripple	0.5%
Operating frequency	1.1 MHz

9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Set-Point

The output voltage of the LV3842 device is externally adjustable using a resistor divider network. The divider network is comprised of top feedback resistor R_{FBT} and bottom feedback resistor R_{FBB}. Equation 7 is used to determine the output voltage of the converter:

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \tag{7}$$

Choose the value of R_{FBB} to be 22.1 kΩ. With the desired output voltage set to 5 V and the V_{REF} = 1.0 V, the R_{FBT} value can then be calculated using Equation 7. The formula yields to a value 88.4 kΩ, a standard value of 88.7 kΩ is selected.

9.2.2.2 Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current and the RMS current. The inductance is based on the desired peak-to-peak ripple current Δi_L. Because the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L_{MIN}. Use Equation 9 to calculate the minimum value of the output inductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current of the device. A reasonable value of K_{IND} must be 20% – 40%. During an instantaneous over current operation event, the RMS and peak inductor current can be high. The inductor current rating must be a bit higher than current limit.

$$\Delta i_L = \frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT}\right)}{V_{IN\_MAX} \times L \times f_{SW}} \tag{8}$$

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \tag{9}$$

In general, it is preferable to choose lower inductance in switching power supplies, because it usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. But too low of an inductance can generate too large of an inductor current ripple such that over current protection at the full load can be falsely triggered. It also generates more inductor core loss because the current ripple is larger. Larger inductor current ripple also implies larger output voltage ripple with same output capacitors. With peak current mode control, TI does note recommend to have too small of an inductor current ripple. A larger peak current ripple improves the comparator signal to noise ratio.

For this design example, choose K_{IND} = 0.4, the minimum inductor value is calculated to be 16.3 µH. Choose the nearest standard 18 µH ferrite inductor with a capability of 1 A RMS current and 1.5 A saturation current.

9.2.2.3 Output Capacitor Selection

The device is designed to be used with a wide variety of LC filters. It is generally desired to use as little output capacitance as possible to keep cost and size down. The output capacitors, C_{OUT}, must be chosen with care because it directly affects the steady state output voltage ripple, loop stability and the voltage over/undershoot during load current transients. The output voltage ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance (ESR) of the output capacitors:

$$\Delta V_{OUT\_ESR} = \Delta i_L \times ESR = K_{IND} \times I_{OUT} \times ESR \tag{10}$$

The other is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT\_C} = \frac{\Delta i_L}{8 \times f_{SW} \times C_{OUT}} = \frac{K_{IND} \times I_{OUT}}{8 \times f_{SW} \times C_{OUT}} \tag{11}$$

The two components in the voltage ripple are not in phase, so the actual peak-to-peak ripple is smaller than the sum of the two peaks.

Output capacitance is usually limited by transient performance specifications if the system requires tight voltage regulation with presence of large current steps and fast slew rate. When a large load step happens, output capacitors provide the required charge before the inductor current can slew up to the appropriate level. The regulator control loop usually needs 8 or more clock cycles to regulate the inductor current equal to the new load level. The output capacitance must be large enough to supply the current difference for 8 clock cycles to maintain the output voltage within the specified range. Equation 12 shows the minimum output capacitance needed for specified output over/undershoot.

$$C_{OUT} > \frac{1}{2} \times \frac{8 \times \left(I_{OH} - I_{OL}\right)}{f_{SW} \times \Delta V_{OUT\_SHOOT}} \tag{12}$$

where

- K_{IND} = Ripple ratio of the inductor ripple current (Δi_L / I_{OUT})
- I_{OL} = Low level output current during load transient
- I_{OH} = High level output current during load transient
- V_{OUT_SHOOT} = Target output voltage over/undershoot

For this design example, the target output ripple is 30 mV. Presuppose ΔV_{OUT_ESR} = ΔV_{OUT_C} = 30 mV, and chose K_{IND} = 0.4. Equation 10 yields ESR no larger than 125 mΩ and Equation 11 yields C_{OUT} no smaller than 0.91 µF. For the target over/undershoot range of this design, ΔV_{OUT_SHOOT} = 5% × V_{OUT} = 250 mV. The C_{OUT} can be calculated to be no smaller than 8.3 µF by Equation 12. In summary, the most stringent criteria for the output capacitor is 8.3 µF. Consider of derating, one 22 µF, 10 V, X7R ceramic capacitor with 10 mΩ ESR is used.

9.2.2.4 Input Capacitor Selection

The LV3842 device requires high frequency input decoupling capacitors and a bulk input capacitor, depending on the application. The typical recommended value for the high frequency decoupling capacitor is 2.2 µF or higher. TI recommends a high-quality ceramic type X5R or X7R with sufficiency voltage rating. The voltage rating must be greater than the maximum input voltage. To compensate the derating of ceramic capacitors, TI recommends a voltage rating of twice the maximum input voltage. Additionally, some bulk capacitance can be required, especially if the LV3842 circuit is not located within approximately 5 cm from the input voltage source. This capacitor is used to provide damping to the voltage spiking due to the lead inductance of the cable or trace. The value for this capacitor is not critical but must be rated to handle the maximum input voltage including ripple. For this design, one 2.2 µF, X7R dielectric capacitor rated for 50 V is used for the input decoupling capacitor. The equivalent series resistance (ESR) is approximately 10 mΩ, and the current rating is 1 A. Include a capacitor with a value of 0.1 µF for high-frequency filtering and place it as close as possible to the device pins.

9.2.2.5 Bootstrap Capacitor

Every LV3842 design requires a bootstrap capacitor, C_{BOOT}. The recommended bootstrap capacitor is 0.1 µF and rated at 16 V or higher. The bootstrap capacitor is located between the SW pin and the CB pin. The bootstrap capacitor must be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

9.2.2.6 Undervoltage Lockout Set-Point

The system undervoltage lockout (UVLO) is adjusted using the external voltage divider network of R_{ENT} and R_{ENB}. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. The following equation can be used to determine the V_{IN} UVLO level.

$$V_{IN\_RISING} = V_{ENH} \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \tag{13}$$

The EN rising threshold (V_{ENH}) for LV3842 is set to be 1.23 V (typical). Choose the value of R_{ENB} to be 200 kΩ to minimize input current from the supply. If the desired V_{IN} UVLO level is at 6.0 V, then the value of R_{ENT} can be calculated using Equation 14:

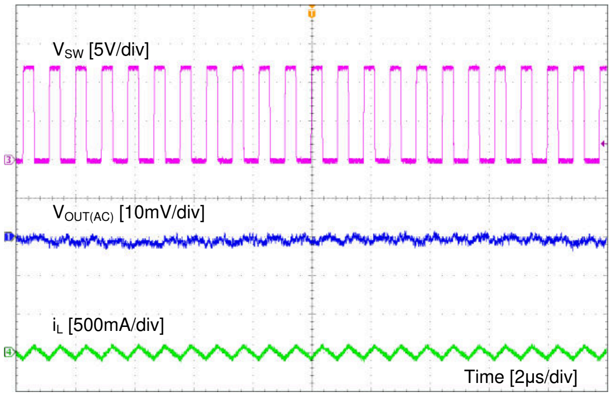
$$R_{ENT} = \left(\frac{V_{IN\_RISING}}{V_{ENH}} - 1 \right) \times R_{ENB} \tag{14}$$

The above equation yields a value of 775.6 kΩ, a standard value of 768 kΩ is selected. The resulting falling UVLO threshold, equals 5.3 V, can be calculated by Equation 15, where EN hysteresis (V_{EN_HYS}) is 0.13 V (typical).

$$V_{IN\_FALLING} = \left(V_{ENH} - V_{EN\_HYS} \right) \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \tag{15}$$

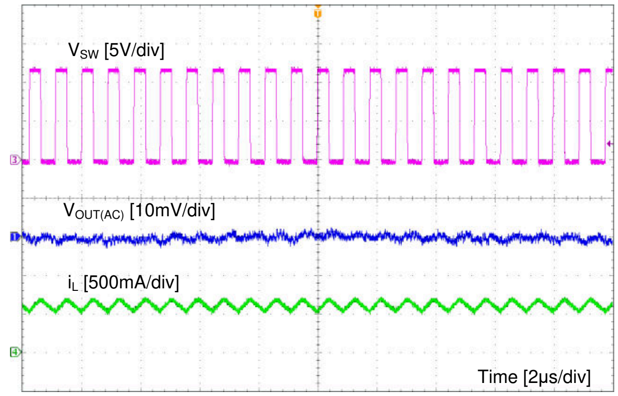
9.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, V_{OUT} = 5 V, f_{SW} = 1.1 MHz, L = 18 µH, C_{OUT} = 22 µF, T_A = 25 °C



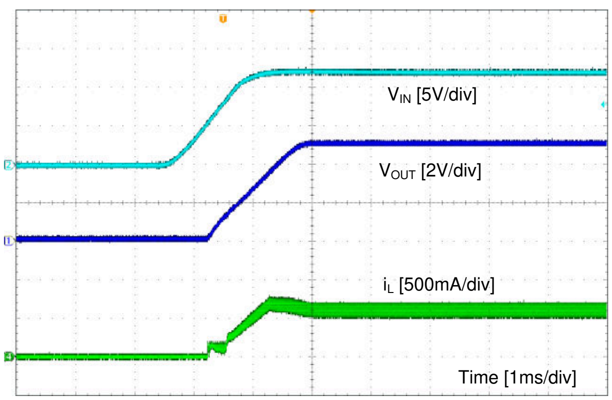
I_{OUT} = 0 mA FPWM Version

Figure 9-2. Ripple at No Load



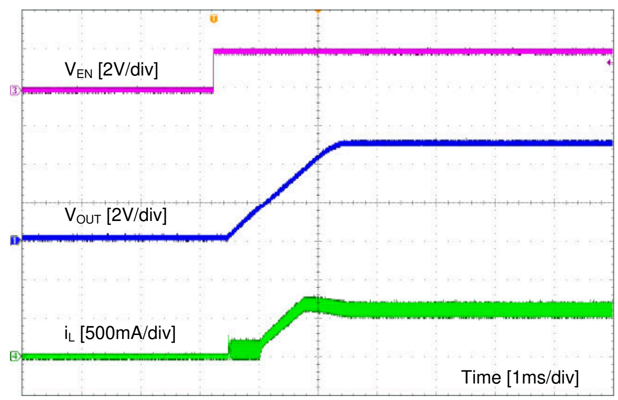
I_{OUT} = 600 mA FPWM Version

Figure 9-3. Ripple at Full Load



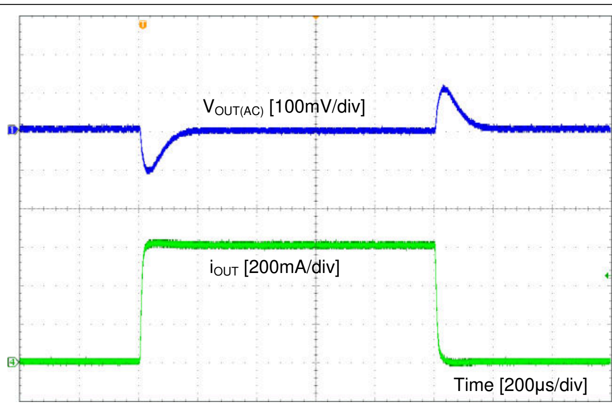
I_{OUT} = 600 mA FPWM Version

Figure 9-4. Start-up by V_{IN}



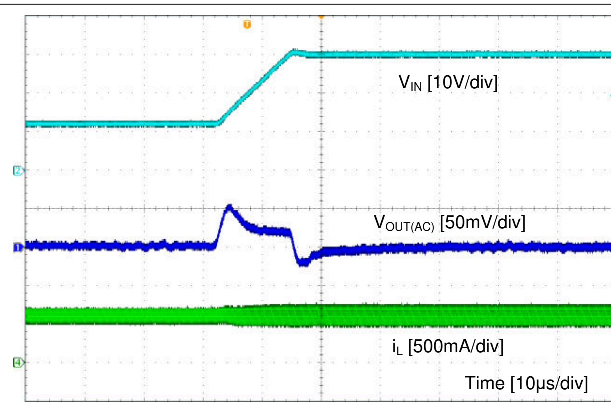
I_{OUT} = 600 mA FPWM Version

Figure 9-5. Start-up by EN



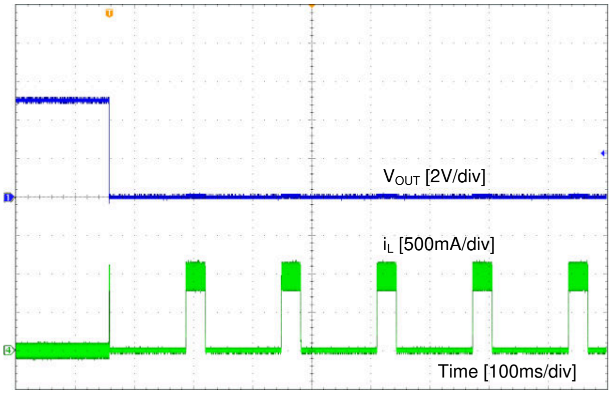
I_{OUT} = 0 to 600 mA, 100 mA / µs FPWM Version

Figure 9-6. Load Transient



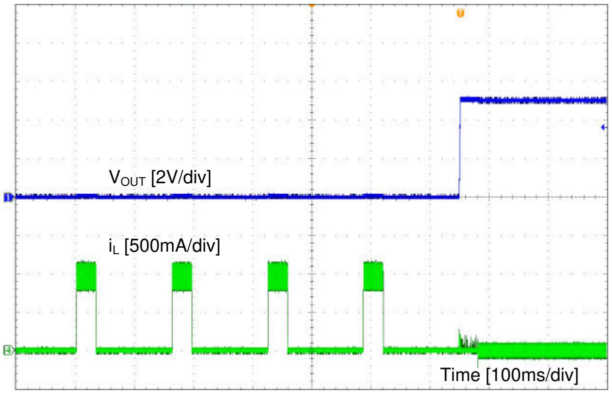
V_{IN} = 12 V to 30 V, 0.18 V / µs I_{OUT} = 600 mA FPWM Version

Figure 9-7. Line Transient



I_{OUT} = 0 mA to short FPWM Version

Figure 9-8. Short Protection



A. I_{OUT} = short to 0 mA FPWM Version

Figure 9-9. Short Recovery

9.3 Power Supply Recommendations

The LV3842 is designed to operate from an input voltage supply range between 4.0 V and 36 V. This input supply must be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LV3842 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LV3842 additional bulk capacitance can be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 10 µF or 22 µF electrolytic capacitor is a typical choice.

9.4 Layout

9.4.1 Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. The input bypass capacitor C_{IN} must be placed as close as possible to the VIN and GND pins. Grounding for both the input and output capacitors must consist of localized top side planes that connect to the GND pin.
2. Minimize trace length to the FB pin net. Both feedback resistors, R_{FBT} and R_{FBB} must be located close to the FB pin. If V_{OUT} accuracy at the load is important, make sure V_{OUT} sense is made at the load. Route V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a shielded layer.
3. Use ground plane in one of the middle layers as noise shielding and heat dissipation path if possible.
4. Make V_{IN}, V_{OUT} and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
5. Provide adequate device heat-sinking. GND, VIN and SW pins provide the main heat dissipation path, make the GND, VIN and SW plane area as large as possible. Use an array of heat-sinking vias to connect the top side ground plane to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, these thermal vias can also be connected to inner layer heat-spreading ground planes. Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125 °C.

9.4.2 Compact Layout for EMI Reduction

Radiated EMI is generated by the high di/dt components in pulsing currents in switching converters. The larger area covered by the path of a pulsing current, the more EMI is generated. High frequency ceramic bypass capacitors at the input side provide primary path for the high di/dt components of the pulsing current. Placing ceramic bypass capacitors as close as possible to the VIN and GND pins is the key to EMI reduction.

The SW pin connecting to the inductor must be as short as possible, and just wide enough to carry the load current without excessive heating. Short, thick traces or copper pours (shapes) must be used for high current conduction path to minimize parasitic resistance. The output capacitors must be placed close to the V_{OUT} end of the inductor and closely grounded to GND pin.

9.4.3 Feedback Resistors

To reduce noise sensitivity of the output voltage feedback path, it is important to place the resistor divider close to the FB pin, rather than close to the load. The FB pin is the input to the error amplifier, so it is a high impedance node and very sensitive to noise. Placing the resistor divider closer to the FB pin reduces the trace length of FB signal and reduces noise coupling. The output node is a low impedance node, so the trace from V_{OUT} to the resistor divider can be long if short path is not available.

If voltage accuracy at the load is important, make sure voltage sense is made at the load. Doing so will correct for voltage drops along the traces and provide the best output accuracy. The voltage sense trace from the load to the feedback resistor divider must be routed away from the SW node path and the inductor to avoid contaminating the feedback signal with switch noise, while also minimizing the trace length. This is most important when high value resistors are used to set the output voltage. TI recommends to route the voltage sense trace and place the resistor divider on a different layer than the inductor and SW node path, such that there is a ground plane in between the feedback trace and inductor/SW node polygon. This provides further shielding for the voltage feedback path from EMI noises.

9.4.4 Layout Example

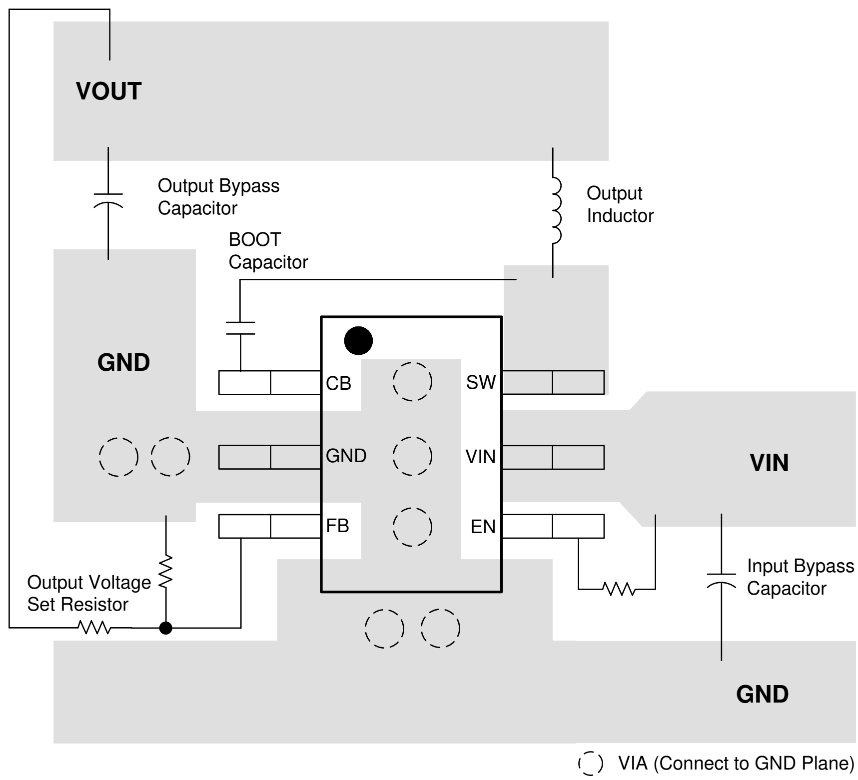


Figure 9-10. Layout

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies* application report

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LV3842XDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1S1F	Samples
LV3842XFDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	VAXF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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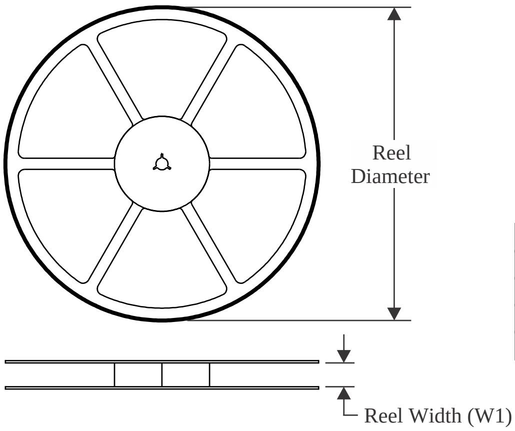
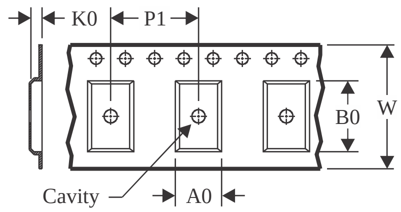
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

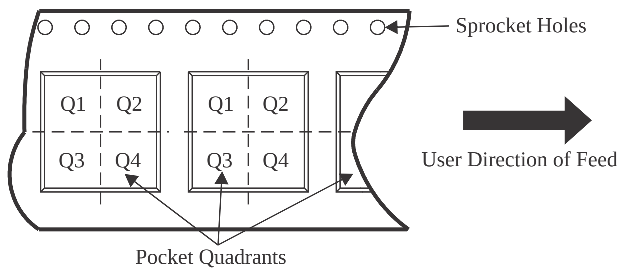


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

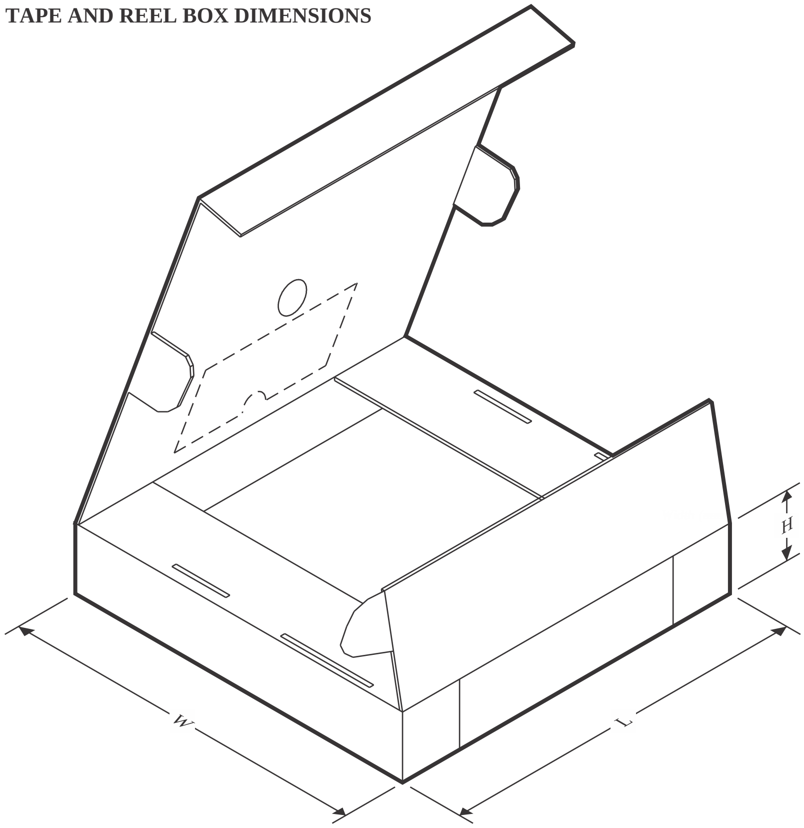
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

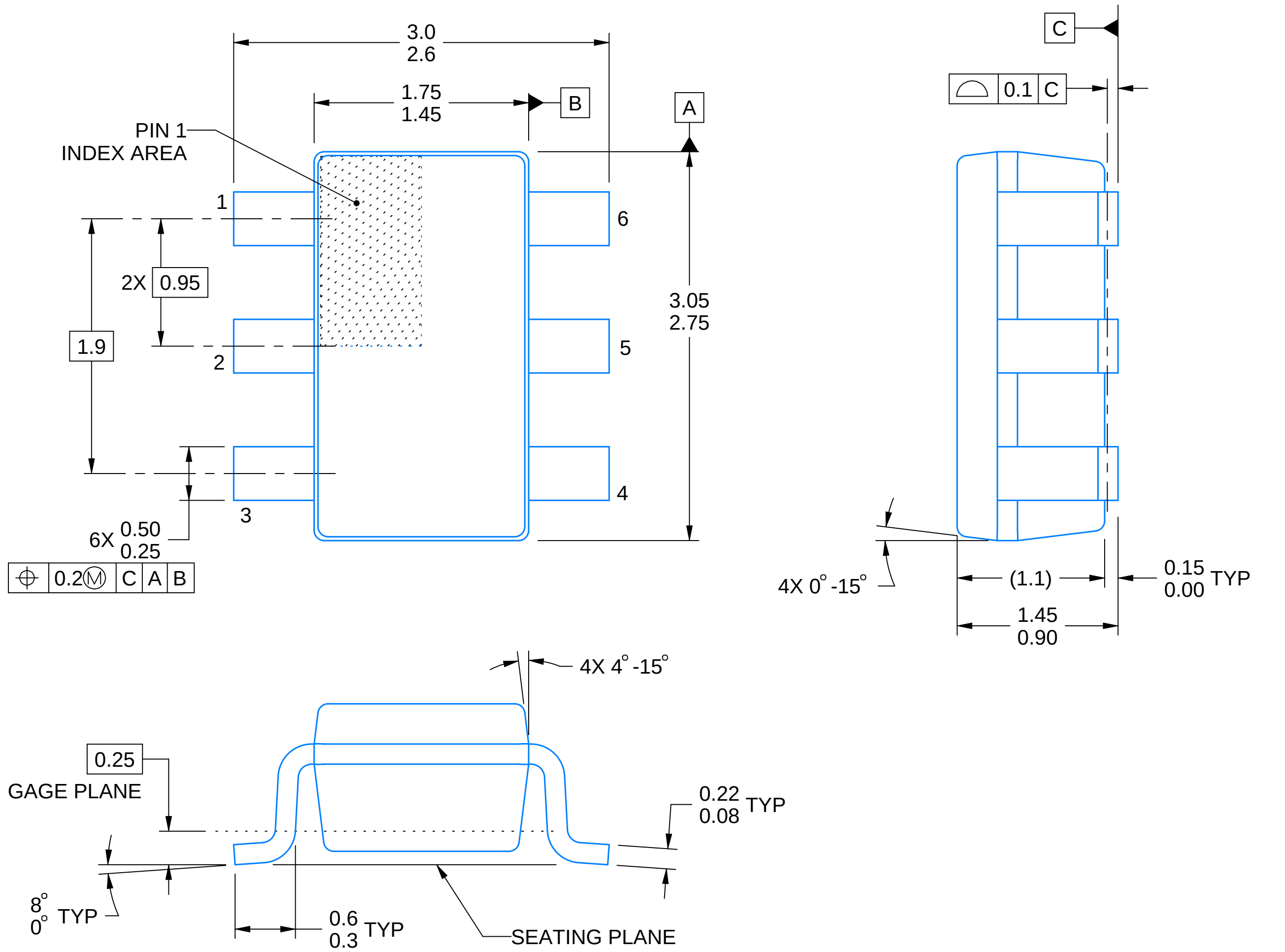
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LV3842XDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LV3842XFDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LV3842XDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
LV3842XFDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0



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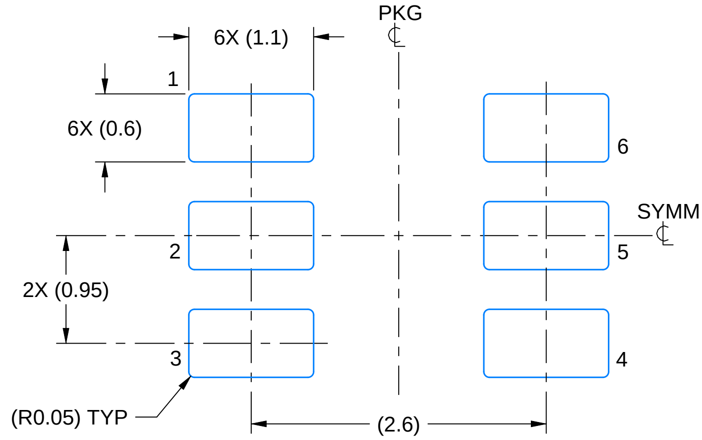
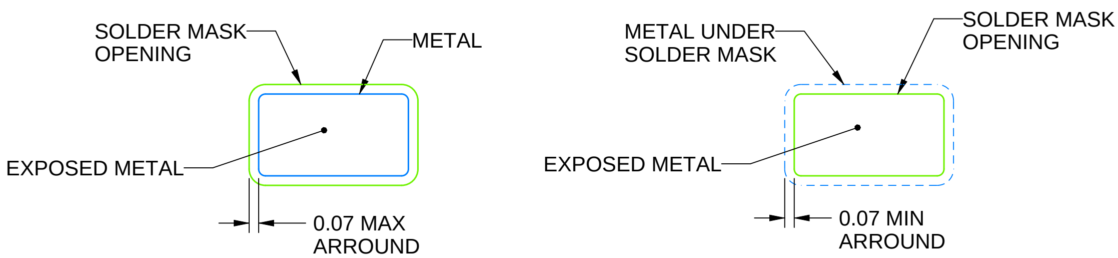
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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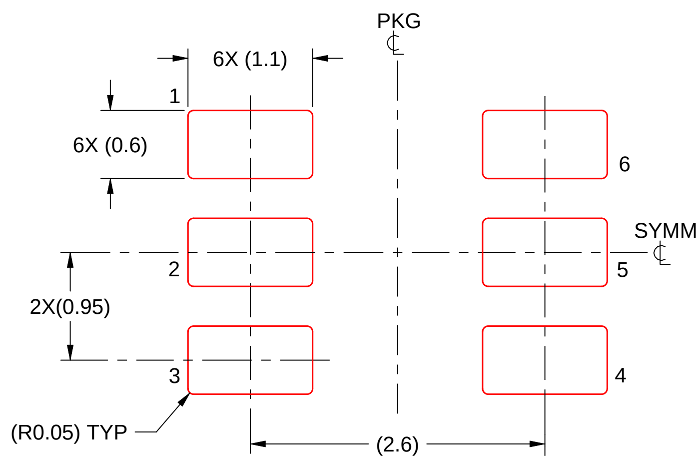
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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