LV284 High-Efficiency, Wide, Input-Voltage-Range Buck Regulator

1 Features

- New product available:
  - LMR43610 3 to 36-V, 1-A, 200-kHz to 2.2-MHz synchronous converter
- For faster time to market:
  - TLVM23615 3 to 36-V, 1.5-A, 200-kHz to 2.2-MHz power module
- Input range 4 V to 40 V with 45-V transients
- 0.7-MHz switching frequency
- Ultra-high efficiency for light load with Eco-mode
- Low dropout operation
- Output current up to 1 A
- Precision enable input
- Overcurrent protection
- Internal compensation
- Internal soft start
- Small overall solution size (TSOT-6L package)

2 Applications

- Power meter
- Collector
- Concentrator
- Industrial distributed power applications

3 Description

The LV284 is a PWM DC/DC buck (step-down) regulator. With a wide input range from 4 V to 40 V, the device is designed for a wide range of applications from industrial to automotive. An ultra-low, 1-µA shutdown current prolongs battery life. Operating frequency is fixed at 0.7 MHz allowing the use of small external components while still being able to have low output ripple voltage. Soft-start and compensation circuits are implemented internally, and these allow the device to be used with minimum external components.

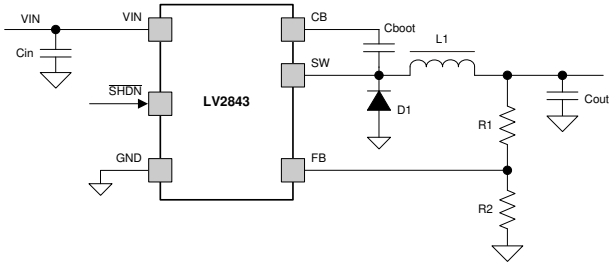
The LV284 is optimized for up to 1-A load current. The device has a 0.765-V nominal feedback voltage.

The device has built-in protection features such as pulse-by-pulse current limit, thermal sensing and shutdown due to excessive power dissipation. The LV284 is available in a low profile TSOT-6L package (2.9 mm × 1.6 mm × 0.85 mm).

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LV284	DDC (TSOT-6L, 6)	2.90 mm × 2.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

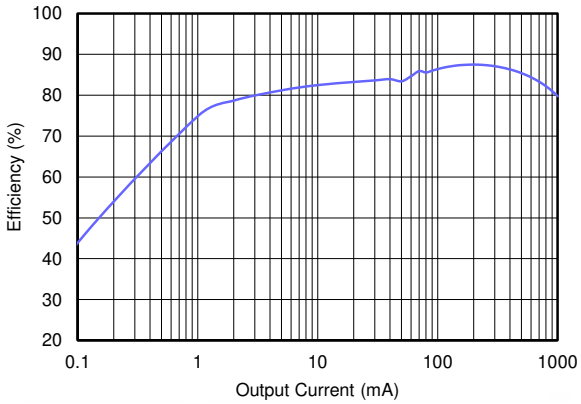


Figure 3-1. Efficiency vs. Current (f_{SW}= 0.7 MHz, V_{IN} = 12 V, V_{OUT} = 3.3 V)

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2015) to Revision B (September 2023)	Page
• First public release	1
• Updated the generic part number to LV284	1
• Added links to LMR43610 and TLVM23615	1
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated *Package Information* table to current standards	1
• Moved the storage temperature range row to the *Absolute Maximum Ratings* table	4
• Updated the *ESD Ratings* table to current standards	4
• Updated the *Thermal Information* table to current standards	4
• Added the *Device Functional Modes* section	8

Changes from Revision * (July 2014) to Revision A (January 2015)	Page
• Changed from Product Preview to Production Data and still a custom document for the China customers	1

5 Pin Configuration

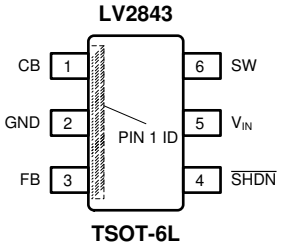


Figure 5-1. DDC Package, 6-Pin TSOT-6L (Top View)

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CB	1	I	SW FET gate bias voltage. Connect C_{boot} cap between CB and SW.
GND	2	G	Ground Connection.
FB	3	I	Feedback Pin. Set feedback voltage divider ratio with $V_{OUT} = V_{FB}$ (1+(R1/R2))
$\overline{SHDN}$	4	I	Enable and disable input pin(high voltage tolerant). Internal pull-up current source. Pull below 1.25 V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors.
VIN	5	I	Power input voltage pin. Input for internal supply and drain node input for internal high-side MOSFET.
SW	6	O	Switch node. Connect to inductor, diode and C_{boot} cap.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Voltages	V_{IN} to GND	–0.3	45	V
	$\overline{SHDN}$ to GND	–0.3	45	
	FB to GND	–0.3	7	
	CB to SW	–0.3	7	
Output Voltages	SW to GND	–1	45	V
	SW to GND less than 30-ns transients	–2	45	
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature range	–55	165	°C

(1) Stresses at or beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)		1000	V
		Charged device model (CDM), per JEDEC specification JESD22- C101, all pins(2)		500	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process, CB PIN passes 500-V test.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Buck regulator	Vin	4	40	V
	CB		46	
	CB to SW		6	
	SW	–0.7	40	
	FB	0	5	
Control	$\overline{SHDN}$	0	40	
Temperature	Operating junction temperature, T_J	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		SOT (DDC) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.9	
ψ_{JB}	Junction-to-board characterization parameter	28.4	

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

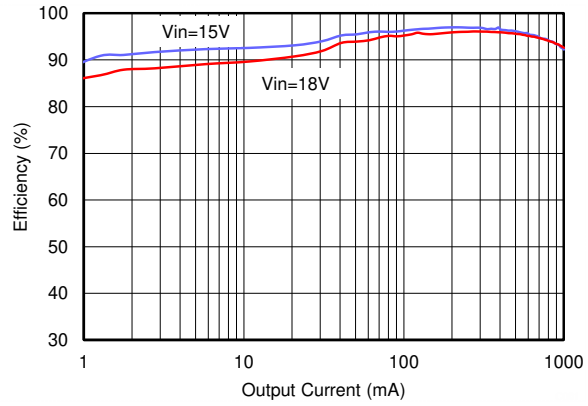
V_{IN} = 12 V, $\overline{SHDN}$ = V_{IN}, T_J = 25°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} (INPUT POWER SUPPLY)					
Operating input voltage		4		40	V
Shutdown supply current	EN = 0 V		1	3	µA
Undervoltage lockout thresholds	Rising			4	V
	Falling	3			V
I_Q	Eco-mode, no load, V_{IN} = 12 V, not switching		30		µA
$\overline{SHDN}$ AND UVLO					
Rising $\overline{SHDN}$ Threshold Voltage		1.05	1.25	1.38	V
$\overline{SHDN}$ PIN current	$\overline{SHDN}$ = 2.3 V		-4.2		µA
	$\overline{SHDN}$ = 0.9 V		-1		
Hysteresis current			-3		µA
HIGH-SIDE MOSFET					
On-resistance	V_{IN} = 12 V, CB to SW = 5.8 V		500		mΩ
t_{ON-MIN} (1)			95		ns
D_{MAX} : Maximum duty cycle(1)			96%		
V_{FB} : Feedback voltage		0.74	0.765	0.79	V
CURRENT LIMIT					
Current limit threshold	V_{IN} = 12 V		1500		mA
f_{SW} Switching frequency		550	700	850	kHz
THERMAL PERFORMANCE					
$T_{SHUTDOWN}$ Thermal shutdown trip point(1)			170		°C
T_{HYS} (1)	Hysteresis		10		°C

(1) Specified by design.

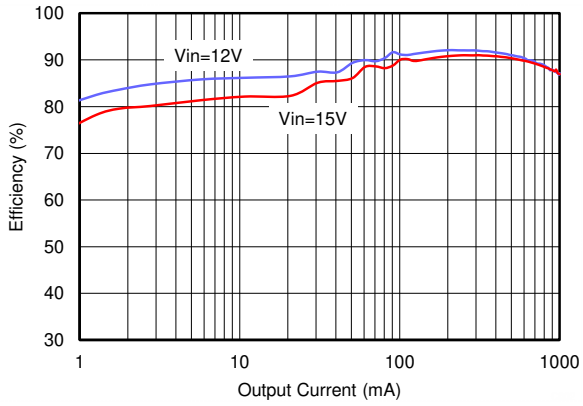
6.6 Typical Characteristics

Unless otherwise noted, V_{IN} = 12 V, L = 22 µH, C_{OUT} = 22 µF, T_A = 25°C



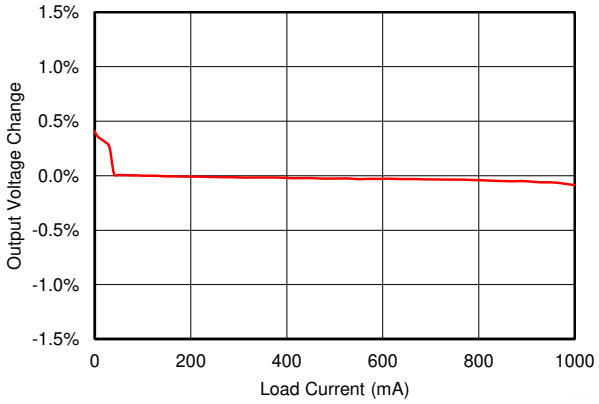
f_{SW} = 0.7 MHz V_{OUT} = 12 V

Figure 6-1. Efficiency vs Load Current



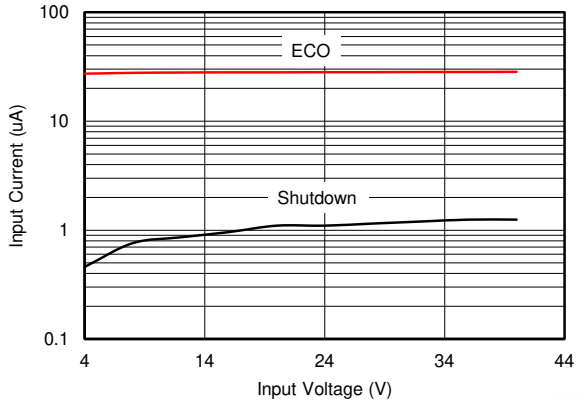
f_{SW} = 0.7 MHz V_{OUT} = 5 V

Figure 6-2. Efficiency vs Load Current



V_{IN} = 18 V V_{OUT} = 12 V

Figure 6-3. Load Regulation



V_{OUT} = 5 V

Figure 6-4. Supply Current vs Input Voltage (No Load)

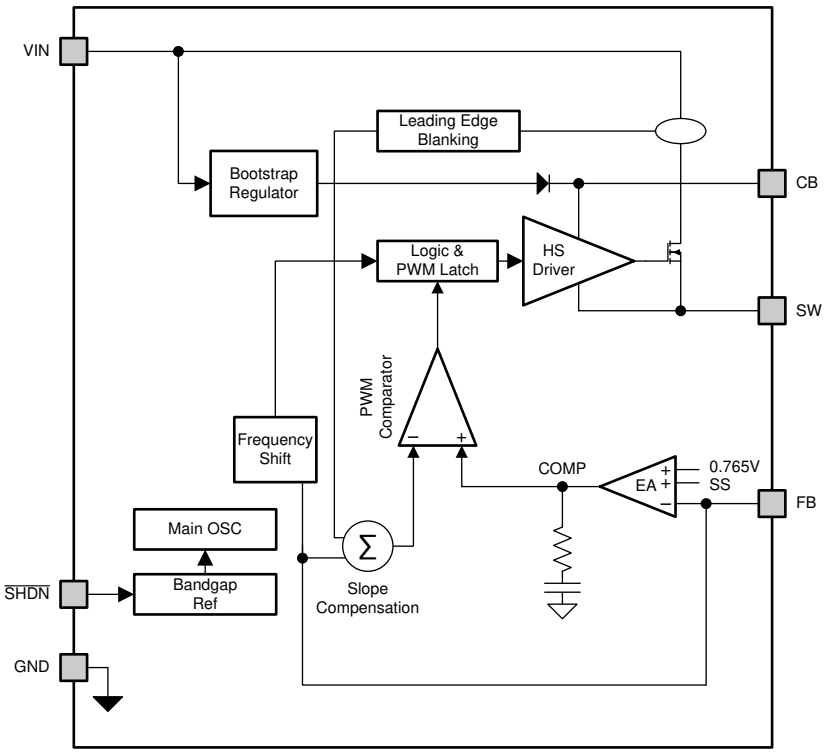
7 Detailed Description

7.1 Overview

The LV284 device is a 40 V, 1 A step-down (buck) regulator. The buck regulator has a very low quiescent current during the light load to prolong the battery life.

The LV284 improves performance during line and load transients by implementing a constant frequency, current mode control which reduces output capacitance and simplifies frequency compensation design. The LV284 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high side MOSFET is supplied by a capacitor on the CB to SW pin. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high side MOSFET off when the boot voltage falls below a preset threshold. The LV284 can operate at high duty cycles because of the boot UVLO and small refresh FET. The output voltage can be stepped down to as low as the 0.765 V reference. Internal soft start is featured to minimize inrush currents.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed Frequency PWM Control

The LV284 operates at a fixed frequency, and it implements peak current mode control. The output voltage is compared through external resistors on the FB pin to an internal voltage reference by an error amplifier which drives the internal COMP node. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output is compared to the high side power switch current. When the power switch current reaches the level set by the internal COMP voltage, the power switch is turned off. The internal COMP node voltage will increase and decrease as the output current increases and decreases. The device implements a current limit by clamping the COMP node voltage to a maximum level.

7.3.2 Bootstrap Voltage (CB)

The LV284 has an integrated boot regulator, and requires a small ceramic capacitor between the CB and SW pins to provide the gate drive voltage for the high side MOSFET. The CB capacitor is refreshed when the high side MOSFET is off and the low side diode conducts.

To improve drop out, the LV284 is designed to operate at 96% duty cycle as long as the CB to SW pin voltage is greater than 3.2 V. When the voltage from CB to SW drops below 3.2 V, the high-side MOSFET is turned off using an UVLO circuit which allows the low side diode to conduct and refresh the charge on the CB capacitor. Because the supply current sourced from the CB capacitor is low, the high-side MOSFET can remain on for more switching cycles than are required to refresh the capacitor, thus the effective duty cycle of the switching regulator is high.

Attention must be taken in maximum duty cycle applications with light load. To ensure SW can be pulled to ground to refresh the CB capacitor, an internal circuit will charge the CB capacitor when the load is light or the device is working in dropout condition.

7.3.3 Setting the Ouput Voltage

The output voltage is set using the feedback pin and a resistor divider connected to the output as shown on the front page schematic. The feedback pin voltage 0.765 V, so the ratio of the feedback resistors sets the output voltage according to the following equation: V_{OUT} = 0.765 V (1+(R1/R2)). Typically R2 will be given as 1 kΩ to 100 kΩ for a starting value. To solve for R1 given R2 and V_{OUT} uses R1 = R2 ((V_{OUT}/0.765 V) – 1).

7.3.4 Enable ($\overline{SHDN}$) and V_{IN} Undervoltage Lockout

The LV284 $\overline{SHDN}$ pin is a high voltage tolerant input with an internal pull up circuit. The device can be enabled even if the $\overline{SHDN}$ pin is floating. The regulator can also be turned on using 1.25 V or higher logic signals. If the use of a higher voltage is desired due to system or other constraints it can be used. TI recommends a 100 kΩ or larger resistor between the applied voltage and the $\overline{SHDN}$ pin to protect the device. When $\overline{SHDN}$ is pulled down to 0 V, the chip is turned off and enters the lowest shutdown current mode. In shutdown mode the supply current decreases to approximately 1 µA. If the shutdown function is not to be used, the $\overline{SHDN}$ pin can be tied to V_{IN}. The maximum voltage to the $\overline{SHDN}$ pin must not exceed 40 V.

The LV284 has an internal UVLO circuit to shutdown the output if the input voltage falls below an internally fixed UVLO threshold level. This circuit ensures that the regulator is not latched into an unknown state during low input voltage conditions. The regulator powers up when the input voltage exceeds the UVLO voltage level. If there is a requirement for a higher UVLO voltage, the $\overline{SHDN}$ can be used to adjust the input voltage UVLO by using external resistors.

7.3.5 Current Limit

The LV284 implements current mode control which uses the internal COMP voltage to turn off the high side MOSFET on a cycle by cycle basis. Each cycle the switch current and internal COMP voltage are compared, when the peak switch current intersects the COMP voltage, the high side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier will respond by driving the COMP node high, increasing the switch current. The error amplifier output is clamped internally, which functions as a switch current limit.

7.3.6 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 170°C (typ). The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. After the junction temperature decreases below 160°C (typ), the device reinitiates the power up sequence.

7.4 Device Functional Modes

7.4.1 Continuous Conduction Mode

The LV284 steps the input voltage down to a lower output voltage. In continuous conduction mode (when the inductor current never reaches zero at steady state), the buck regulator operates in two cycles. The power

switch is connected between VIN and SW. In the first cycle of operation, the transistor is closed and the diode is reverse biased. Energy is collected in the inductor, the load current is supplied by C_{OUT} and the current through the inductor is rising. During the second cycle the transistor is open and the diode is forward biased due to the fact that the inductor current cannot instantaneously change direction. The energy stored in the inductor is transferred to the load and output capacitor. The ratio of these two cycles determines the output voltage. The output voltage is defined approximately as: $D = V_{OUT}/V_{IN}$ and $D' = (1-D)$ where D is the duty cycle of the switch, D and D' is required for design calculations.

7.4.2 Eco-mode

The LV284 operates in Eco-mode at light load currents to improve efficiency by reducing switching and gate drive losses. For Eco-mode operation, the LV284 senses peak current, not average or load current, so the load current where the device enters Eco-mode is dependent on V_{IN}, V_{OUT} and the output inductor value. When the load current is low and the output voltage is within regulation, the device enters Eco-mode (see Figure12) and draws only 28-µA input quiescent current.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LV284 is a step down DC-to-DC regulator. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 1 A. The following design procedure can be used to select components for the LV284. This section presents a simplified discussion of the design process.

8.2 Typical Applications

8.2.1 5 V Output Application

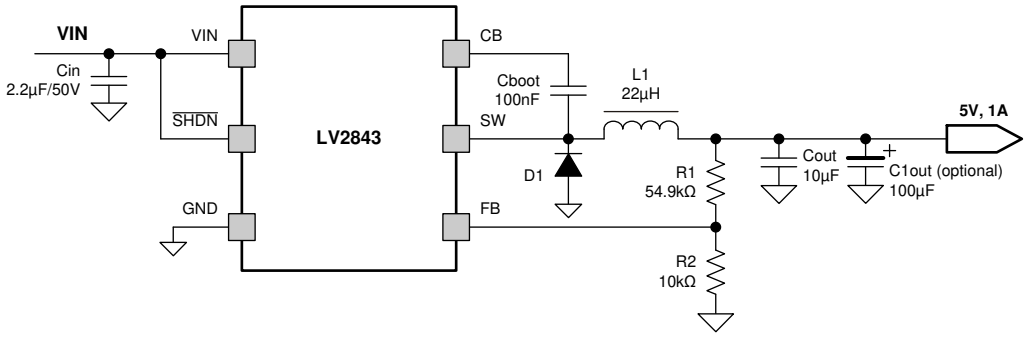


Figure 8-1. Application Circuit, 5 V Output

8.2.1.1 Design Requirements

8.2.1.1.1 Design Guide – Step By Step Design Procedure

This example details the design of a high frequency switching regulator using ceramic output capacitors. A few parameters must be known to start the design process. These parameters are typically determined at the system level:

Input voltage, VIN		9 V to 16 V, typical 12 V
Output voltage, VOUT		5.0 V ± 3%
Maximum output current example I_{O_max}		1 A
Minimum output current example I_{O_min}		0.1 A
Transient response 0.03 A to 0.6 A		5%
Output voltage ripple		1%
Switching frequency f_{SW}		700 kHz
Target during load transient	Overvoltage peak value	106% of output voltage
	Undervoltage value	91% of output voltage

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Output Inductor Selection

The most critical parameters for the inductor are the inductance, peak current and the DC resistance. The inductance is related to the peak-to-peak inductor ripple current, the input and the output voltages. Because the ripple current increases with the input voltage, the maximum input voltage is always used to determine

the inductance. Equation 1 is used to calculate the minimum value of the output inductor, where K_{IND} is ripple current percentage. A reasonable value is setting the ripple current to be 30%(K_{IND}) of the DC output current. For this design example, the minimum inductor value is calculated to be 16.4 µH, and a nearest standard value was chosen: 22 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 3 and Equation 4. The inductor ripple current is 0.22 A, and the RMS current is 1 A. As the equation set demonstrates, lower ripple currents will reduce the output voltage ripple of the regulator but will require a larger value of inductance. A good starting point for most applications is 22 µH with a 1.6 A current rating. Using a rating near 1.6 A will enable the LV284 to current limit without saturating the inductor. This is preferable to the LV284 going into thermal shutdown mode and the possibility of damaging the inductor if the output is shorted to ground or other long-term overload.

$$L_{o\,\min} = \frac{V_{in\,\max} - V_{out}}{I_o \times K_{IND}} \times \frac{V_{out}}{V_{in\,\max} \times f_{sw}} \tag{1}$$

$$I_{ripple} = \frac{V_{out} \times (V_{in\,\max} - V_{out})}{V_{in\,\max} \times L_o \times f_{sw}} \tag{2}$$

$$I_{L\text{-}RMS} = \sqrt{I_o^{\,2} + \frac{1}{12} I_{ripple}^{\,2}} \tag{3}$$

$$I_{L-peak} = I_o + \frac{I_{ripple}}{2} \tag{4}$$

8.2.1.2.2 Output Capacitor Selection

The selection of C_{OUT} is mainly driven by three primary considerations. The output capacitor will determine the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 5 shows the minimum output capacitance necessary to accomplish this. For this example, the transient load response is specified as a 3% change in Vout for a load step from 0.1 A to 1 A (full load). For this example, ΔI_{OUT} = 1 - 0.1 = 0.9 A and ΔV_{OUT} = 0.03 × 5 = 0.15 V. Using these numbers gives a minimum capacitance of 17.1 µF. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. Aluminum electrolytic and tantalum capacitors have higher ESR that must be taken into account.

The stored energy in the inductor will produce an output voltage overshoot when the load current rapidly decreases. The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high load current to a lower load current. Equation 6 is used to calculate the minimum capacitance to keep the output voltage overshoot to a desired value. Where L is the value of the inductor, I_{OH} is the output current under heavy load, I_{OL} is the output under light load, Vf is the final peak output voltage, and Vi is the initial capacitor voltage. For this example, the worst case load step will be from 1 A to 0.1 A. The output voltage will increase during this load transition and the stated maximum in our specification is 3 % of the output voltage. This will make Vo_overshoot = 1.03 × 5 = 5.15 V. Vi is the initial capacitor voltage which is the nominal output voltage of 5 V. Using these numbers in Equation 6 yields a minimum capacitance of 14.3 µF.

Equation 7 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where fsw is the switching frequency, Vo_ripple is the maximum allowable output voltage ripple, and IL_ripple is the inductor ripple current. Equation 7 yields 0.26 µF.

Equation 8 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 8 indicates the ESR must be less than 680 mΩ. Additional capacitance de-ratings for aging, temperature and dc bias must be factored in which will increase this minimum value. For this example, 22

µF ceramic capacitors will be used. Capacitors in the range of 4.7 µF to 100 µF are a good starting point with an ESR of 0.7 Ω or less.

$$C_{out} > \frac{2 \times \Delta I_{out}}{fsw \times \Delta V_{out}} \quad (5)$$

$$C_{out} > L_o \times \frac{(Ioh^2 - Iol^2)}{(Vf^2 - Vi^2)} \quad (6)$$

$$C_{out} > \frac{1}{8 \times fsw} \times \frac{1}{\frac{V_{o\_ripple}}{I_{L\_ripple}}} \quad (7)$$

$$R_{ESR} < \frac{V_{o\_ripple}}{I_{L\_ripple}} \quad (8)$$

8.2.1.2.3 Schottky Diode Selection

The breakdown voltage rating of the diode is preferred to be 25% higher than the maximum input voltage. In the target application, the current rating for the diode must be equal to the maximum output current for best reliability in most applications. In cases where the input voltage is not much greater than the output voltage the average diode current is lower. In this case it is possible to use a diode with a lower average current rating, approximately (1-D)×IOUT, however the peak current rating must be higher than the maximum load current. A 1 A to 2 A rated diode is a good starting point.

8.2.1.2.4 Input Capacitor Selection

A low ESR ceramic capacitor is needed between the VIN pin and ground pin. This capacitor prevents large voltage transients from appearing at the input. Use a 1 µF - 10 µF value with X5R or X7R dielectric. Depending on construction, a ceramic capacitor value can decrease up to 50% of its nominal value when rated voltage is applied. Consult with the capacitor manufactures data sheet for information on capacitor derating overvoltage and temperature. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the LV284. The input ripple current can be calculated using below Equations.

For this example design, one 2.2 µF, 50 V capacitor is selected. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 10. Using the design example values, I_{OUTMAX} = 1 A, C_{IN} = 2.2 µF, f_{SW} = 700 kHz, yields an input voltage ripple of 162 mV and a rms input ripple current of 0.5 A.

$$I_{cirms} = I_{out} \times \sqrt{\frac{V_{out}}{V_{in\,\min}} \times \frac{(V_{in\,\min} - V_{out})}{V_{in\,\min}}} \quad (9)$$

$$\Delta V_{in} = \frac{I_{out\,\max} \times 0.25}{C_{in} \times fsw} \quad (10)$$

8.2.1.2.5 Bootstrap Capacitor Selection

TI recommends a 0.1-µF ceramic capacitor or larger for the bootstrap capacitor (C_{boot}). For applications where the input voltage is close to output voltage a larger capacitor is recommended, generally 0.1 µF to 1 µF to ensure plenty of gate drive for the internal switches and a consistently low R_{DSON}. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher because of the stable characteristics over temperature and voltage.

Below are the recommended typical output voltage inductor and capacitor combinations for optimized total solution size.

P/N	V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (µH)	C_{OUT} (µF)
LV284	5	54.9 (1%)	10 (1%)	22	22
LV284	5.7	64.9 (1%)	10 (1%)	22	22
LV284	12	147 (1%)	10 (1%)	22	10

8.2.1.3 Application Performance Curves

Unless otherwise noted, V_{IN} = 12 V, L = 22 µH, C_{OUT} = 22 µF, T_A = 25°C

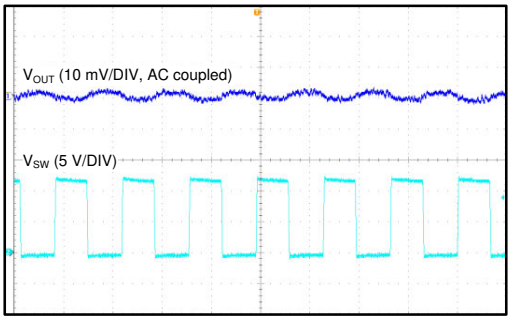


Figure 8-2. Switching Node and Output Voltage Waveform (V_{IN} = 12 V, V_{OUT} = 5 V, I_{Load} = 1 A)

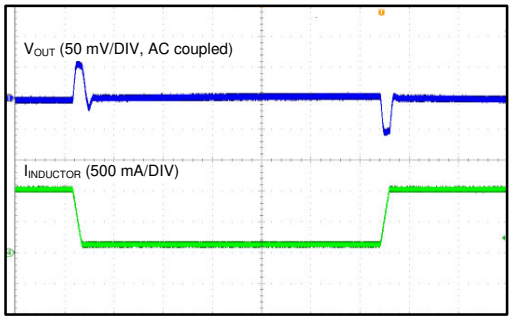


Figure 8-3. Load Transient Between 0.1 A and 1 A (V_{IN}= 12 V, V_{OUT} = 5 V)

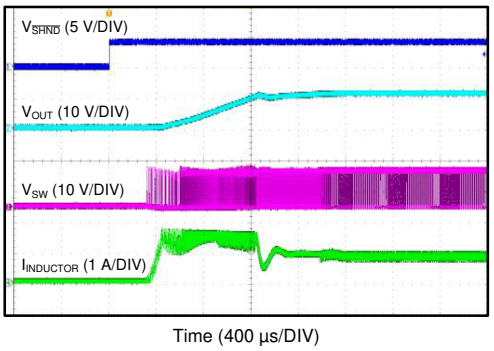


Figure 8-4. Start-up Waveform (V_{IN} = 18 V, V_{OUT}= 12 V, I_{Load} = 800 mA)

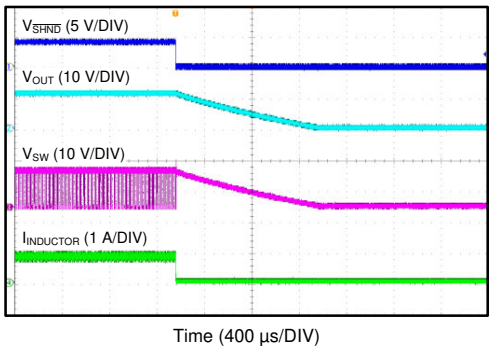


Figure 8-5. Shutdown Waveform (V_{IN} = 18 V, V_{OUT} = 12 V, I_{Load} = 800 mA)

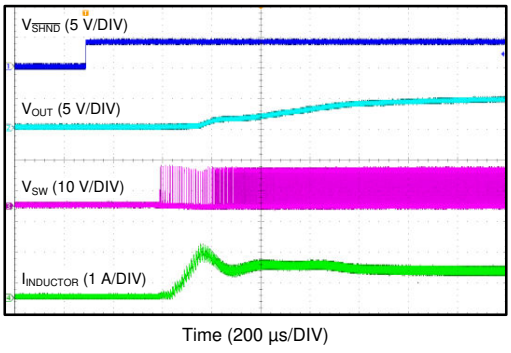


Figure 8-6. Start-up Waveform (V_{IN} = 12 V, V_{OUT} = 5 V, I_{Load} = 800 mA)

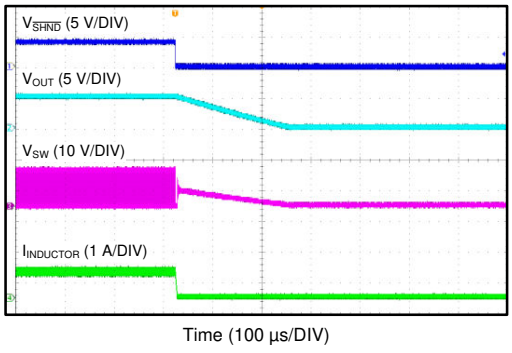


Figure 8-7. Shutdown Waveform (V_{IN} = 12 V, V_{OUT} = 5 V, I_{Load} = 800 mA)

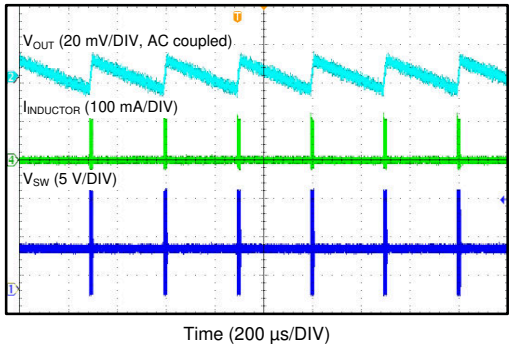


Figure 8-8. Eco-mode Operation (V_{IN} = 12 V, V_{OUT} = 5 V, No Load)

8.3 Power Supply Recommendations

The LV284 is designed to operate from an input voltage supply range between 4 V and 40 V. This input supply must be able to withstand the maximum input current and maintain a voltage above 4 V. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LV284 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LV284, additional bulk capacitance can be required in addition to the ceramic input capacitors.

8.4 Layout

8.4.1 Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. The feedback network, resistors R1 and R2, must be kept close to the FB pin, and away from the inductor to minimize coupling noise into the feedback pin.
2. The input capacitor C_{IN} must be placed close to the V_{IN} pin. This will reduce copper trace inductance which effects input voltage ripple of the IC.
3. The output capacitor C_{OUT} must be placed close to the junction of L1 and the diode D1. The L1, D1 and C_{OUT} trace must be as short as possible to reduce conducted and radiated noise.
4. The inductor L1 must be placed close to the SW pin to reduce magnetic and electrostatic noise.
5. The ground connection for the diode, C_{IN} and C_{OUT} must be tied to the system ground plane in only one spot (preferably at the C_{OUT} ground point) to minimize conducted noise in the system ground plane.
6. For more detail on switching power supply layout considerations see Application Note AN-1149.

8.4.2 Layout Example

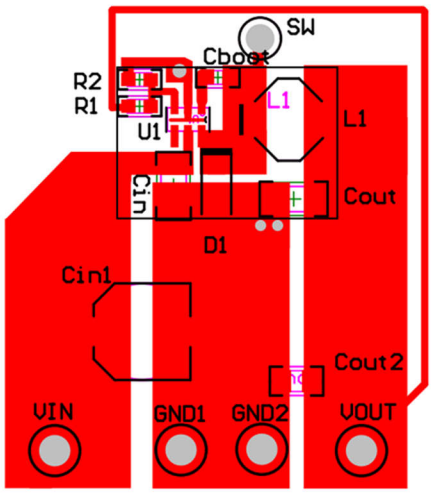


Figure 8-9. Layout Example

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LV2843DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A03X	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

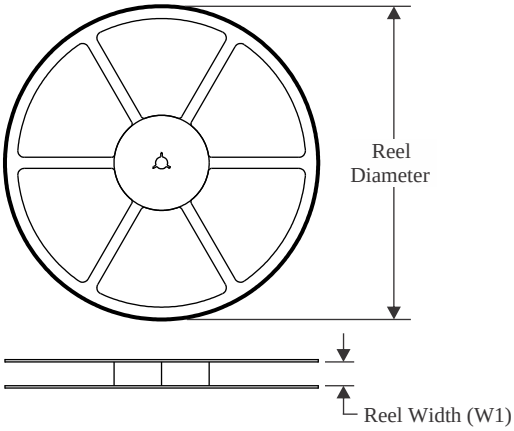
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

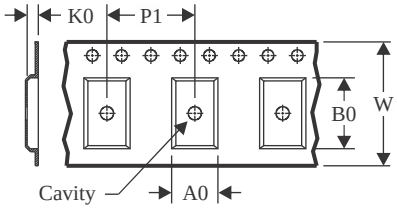
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

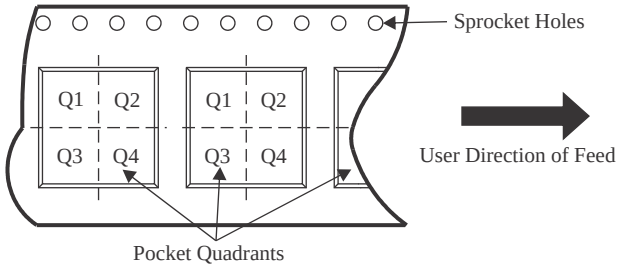


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

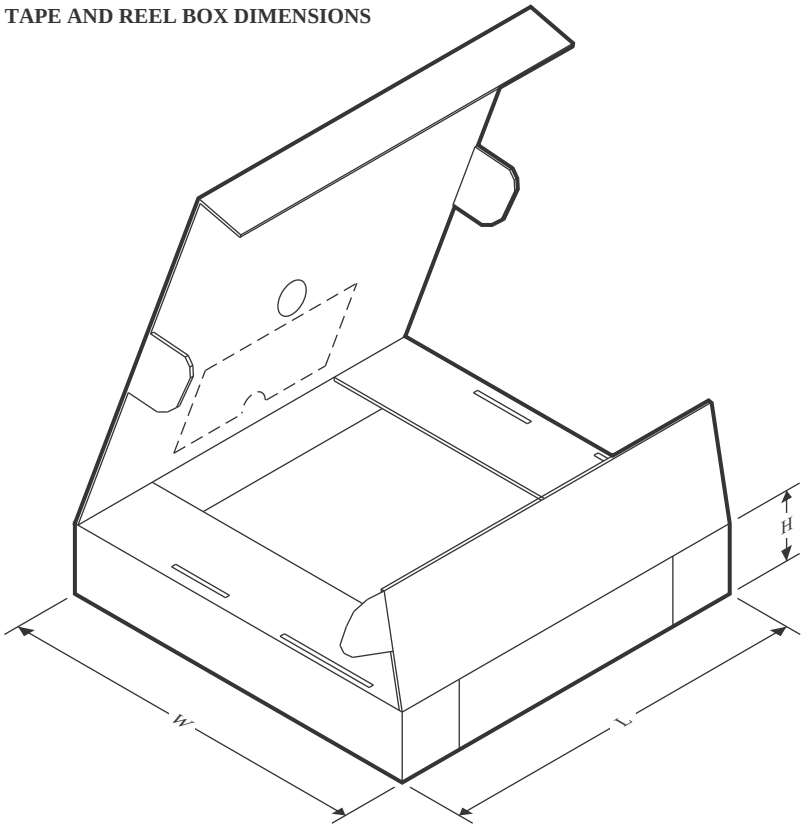
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LV2843DDCR	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

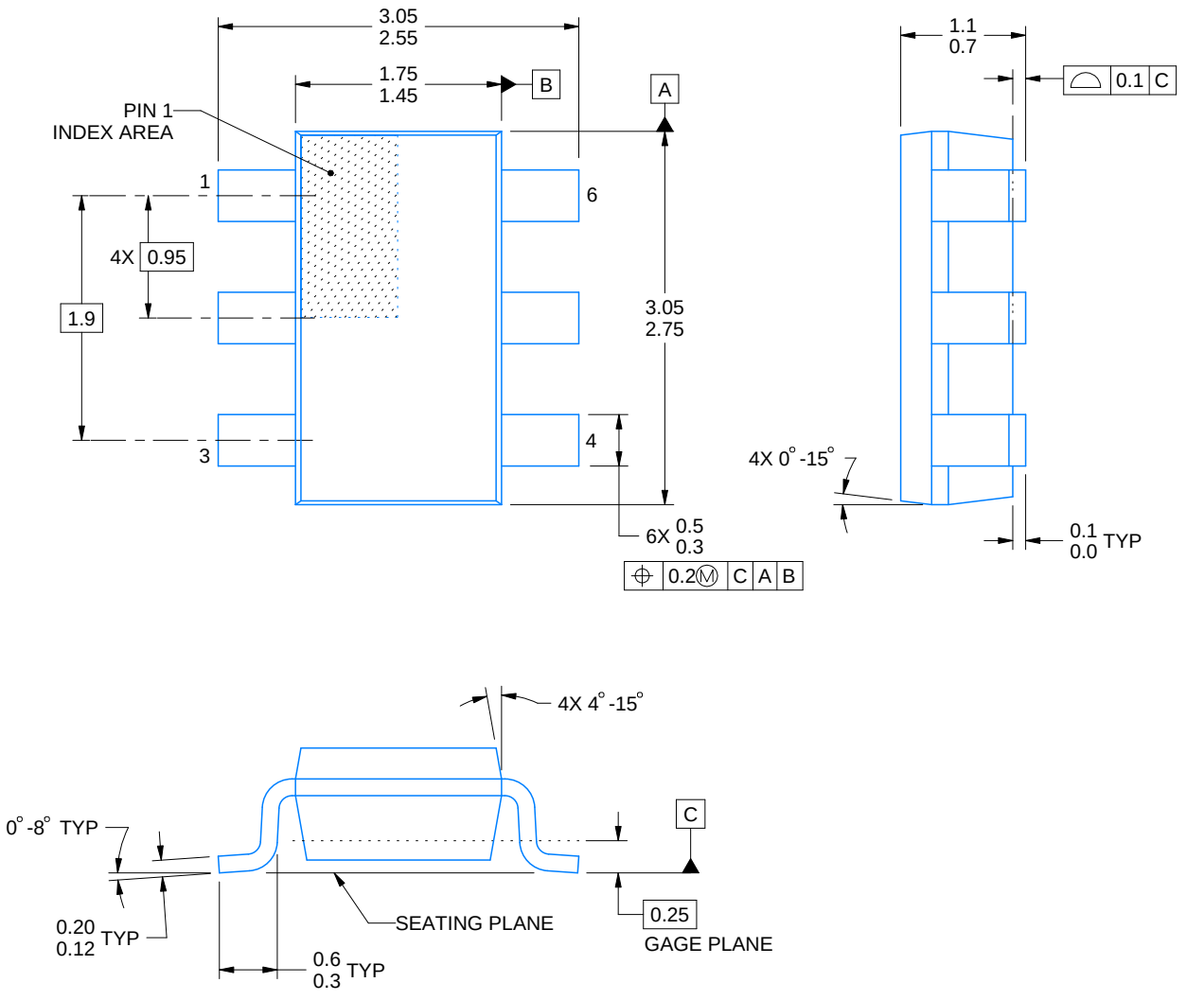
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LV2843DDCR	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



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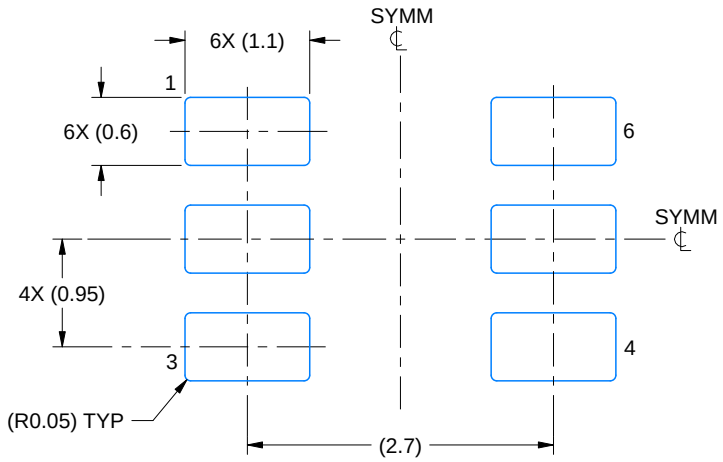
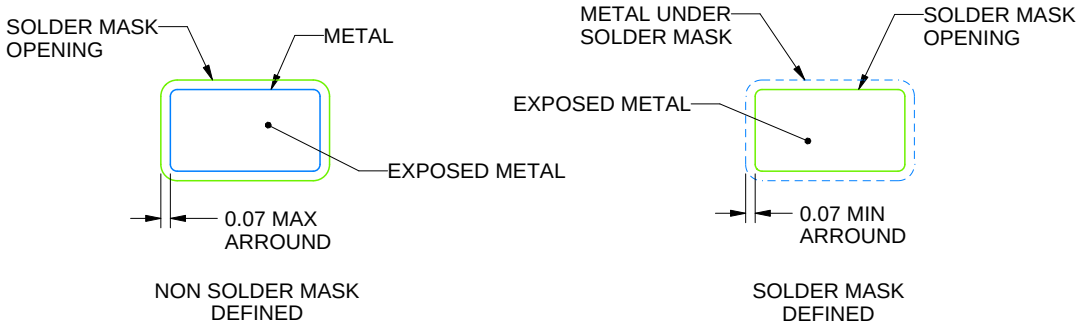
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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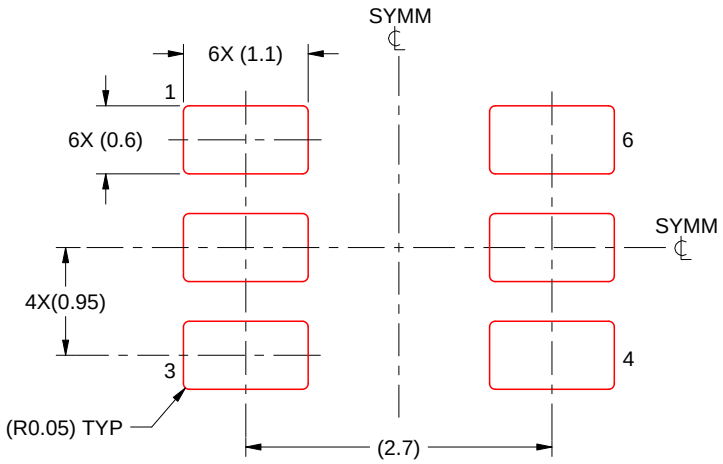
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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