1. DESCRIPTION

The XL555 and XD555 are precision timing circuits capable of producing accurate time delays or oscillation. In the time-delay or mono-stable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the a-stable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

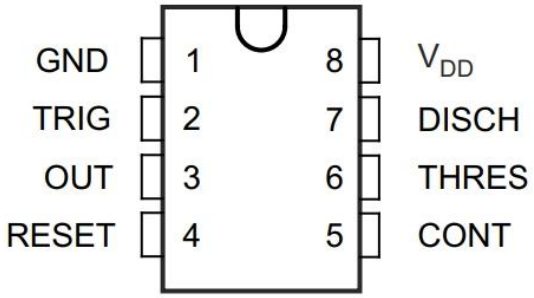
The threshold and trigger levels normally are two-thirds and one-third, respectively, of Vcc. These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set, and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset(RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset, and the output goes low. When the output is low, a low-impedance path is provided between discharge(DISCH) and ground.

The XL555 and XD555 provides reduced supply current spikes during output transitions, which enable the use of lower decoupling capacitors compared to those required by conventional bipolar NE555.

2. FEATURES

- Very low power consumption: 120uA at VDD = 5V (typical)
- Low supply current reduces spikes during output transitions
- High maximum astable frequency of 1.8 MHz
- 2V to 16V single-supply operation
- Supports rail-to-rail swing CMOS outputs
- High output current capability
  - sink current: 100mA (Maximum)
  - sourcing current: 10mA (typical)
- Pin to Pin and functionally interchangeable with bipolar NE555
- ESD Exceeds 1500V as specified in MIL-STD-883C Method 3015.2
- Two available footprint types: SOP8 (XL555) and DIP8 (XD555)

3. PIN CONFIGURATIONS AND FUNCTIONS



(TOP VIEW)

Pin Function Definition:

XL555 / XD555		I/O Type	DESCRIPTION
NAME	PIIN		
GND	1	—	Ground.
TRIG	2	Input	Start of timing input. TRIG < 1/2 CONT sets output high and discharge open.
OUT	3	Output	High current timer output signal.
RESET	4	Input	Active low reset input forces output and discharge low.
CONT	5	Input	Controls comparator thresholds. Outputs 2/3 V_{DD} and allows bypass capacitor connection.
THRES	6	Input	End of timing input. THRES > CONT sets output low and discharge low.
DISCH	7	Output	Open collector output to discharge timing capacitor.
V_{DD}	8	—	Power-supply voltage.

4. FUNCTIONAL BLOCK DIAGRAM

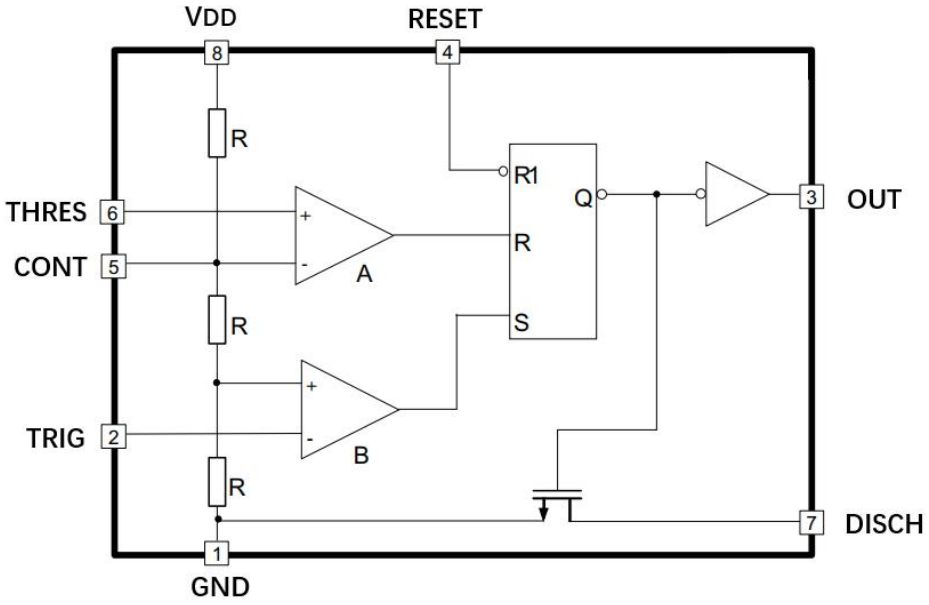


Table 1: Logic Functional

RESET	TRIG (Trigger)	THRES（Threshold）	Output
Low	x	x	Low
High	Low		High
	High	High	Low
		Low	Previous state

Note: Low: level voltage ≤ minimum volta， specified High: level voltage ≥ maximum voltage
specified x: irrelevant

5. SPECIFICATIONS

5.1. Absolute Maximum Ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	+18	V
I_{OUT}	Output current	± 100	mA
R_{thja}	Thermal resistance junction to ambient (1)	130	°C/W
R_{thjc}	Thermal resistance junction to case (1)	65	
T_j	Junction temperature	+150	°C
T_{stg}	Storage temperature range	-50 to +150	
ESD	Human body model (HBM)(2)	1000	V
	Machine model (MM)(3)	200	
	Charged device model (CDM)(4)	750	

1. Short-circuits can cause excessive heating. These values are typical and specified for a four layers PCB.
2. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
3. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins remain floating.
4. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

Table 3. Recommended Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2 to 16	V
I_{OUT}	Output sink current Output source current	<= 10 <= 50	mA
wFreq	Working frequency	<= 1.2	MHz
T_{oper}	Operating free air temperature range	-40 to +85	°C

5.2. Electrical characteristics

Table 4. Static electrical characteristics
V_{CC} = +2 V, T_{amb} = +25 °C, reset to V_{CC} (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current (no load, high and low states) $T_{min} \leq T_{amb} \leq T_{max}$		66	210 210	µA
V_{CL}	Control voltage level $T_{min} \leq T_{amb} \leq T_{max}$	1.2 1.1	1.3	1.4 1.5	V
V_{DIS}	Discharge saturation voltage (I_{dis} = 1 mA) $T_{min} \leq T_{amb} \leq T_{max}$		0.05	0.2 0.25	
I_{DIS}	Discharge pin leakage current		1	150	nA
V_{OL}	Low level output voltage (I_{sink} = 1 mA) $T_{min} \leq T_{amb} \leq T_{max}$		0.1	0.3 0.35	V
V_{OH}	High level output voltage (I_{source} = -0.3 mA) $T_{min} \leq T_{amb} \leq T_{max}$	1.5 1.5	1.9		
V_{TRIG}	Trigger voltage $T_{min} \leq T_{amb} \leq T_{max}$	0.4 0.3	0.67	0.95 1.05	
I_{TRIG}	Trigger current		10		pA
I_{TH}	Threshold current		10		
V_{RESET}	Reset voltage $T_{min} \leq T_{amb} \leq T_{max}$	0.4 0.3	1.1	1.5 2.0	V
I_{RESET}	Reset current		10		pA

Table 5. Static electrical characteristics
V_{CC} = +3 V, T_{amb} = +25 °C, reset to V_{CC} (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current (no load, high and low states) $T_{min} \leq T_{amb} \leq T_{max}$		85	250 250	µA
V_{CL}	Control voltage level $T_{min} \leq T_{amb} \leq T_{max}$	1.8 1.7	2	2.2 2.3	V
V_{DIS}	Discharge saturation voltage (I_{dis} = 1 mA) $T_{min} \leq T_{amb} \leq T_{max}$		0.05	0.2 0.25	V
I_{DIS}	Discharge pin leakage current		1	150	nA
V_{OL}	Low level output voltage (I_{sink} = 1 mA) $T_{min} \leq T_{amb} \leq T_{max}$		0.1	0.3 0.35	V
V_{OH}	High level output voltage (I_{source} = -0.3 mA) $T_{min} \leq T_{amb} \leq T_{max}$	2.5 2.5	2.9		V
V_{TRIG}	Trigger voltage $T_{min} \leq T_{amb} \leq T_{max}$	0.9 0.8	1	1.2 1.3	V
I_{TRIG}	Trigger current		10		pA
I_{TH}	Threshold current		10		pA
V_{RESET}	Reset voltage $T_{min} \leq T_{amb} \leq T_{max}$	0.4 0.3	1.1	1.6 2.1	V
I_{RESET}	Reset current		10		pA

Table 6. Dynamic electrical characteristics
V_{CC} = +3 V, T_{amb} = +25 °C, reset to V_{CC} (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Timing accuracy (monostable)[1] R = 10 kΩ, C = 0.1 µF V_{CC} = 2 V V_{CC} = 3 V		 6 6		%
	Timing shift with supply voltage variations (monostable) R = 10 kΩ, C = 0.1 µF, V_{CC} = 3 V ± 0.3 V [1]		1		%/V
	Timing shift with temperature [1] $T_{min} \leq T_{amb} \leq T_{max}$		100		ppm/°C
f_{max}	Maximum astable frequency [2] R_A = 470 Ω, R_B = 200 Ω, C = 200 pF		1.7		MHz
	Astable frequency accuracy [2] $R_A = R_B$ = 1 kΩto 100 kΩ, C = 0.1 µF	—	10	—	%
	Timing shift with supply voltage variations (astable mode) [2] $R_A = R_B$ = 1 kΩto 100 kΩ, C = 0.1 µF, V_{CC} = 3 to 5 V		1		%/V
t_R	Output rise time (C_{load} = 10 pF)		25		ns
t_F	Output fall time (C_{load} = 10 pF)		20		
t_{PD}	Trigger propagation delay		100		
t_{RPW}	Minimum reset pulse width (V_{trig} = 3 V)		350		

1. See *Figure 1*
2. See *Figure 2*

Table 7. Static electrical characteristics
V_{CC} = +5 V, T_{amb} = +25 °C, reset to V_{CC} (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current (no load, high and low states) $T_{min} \leq T_{amb} \leq T_{max}$		120	270 270	µA
V_{CL}	Control voltage level $T_{min} \leq T_{amb} \leq T_{max}$	2.9 2.8	3.3	3.8 3.9	V
V_{DIS}	Discharge saturation voltage (I_{dis} = 10 mA) $T_{min} \leq T_{amb} \leq T_{max}$		0.2	0.3 0.35	V
I_{DIS}	Discharge pin leakage current		1	160	nA
V_{OL}	Low level output voltage (I_{sink} = 8 mA) $T_{min} \leq T_{amb} \leq T_{max}$		0.3	0.6 0.8	V
V_{OH}	High level output voltage (I_{source} = -2 mA) $T_{min} \leq T_{amb} \leq T_{max}$	4.4 4.4	4.6		V
V_{TRIG}	Trigger voltage $T_{min} \leq T_{amb} \leq T_{max}$	1.36 1.26	1.67	1.98 2.20	V
I_{TRIG}	Trigger current		10		pA
I_{TH}	Threshold current		10		pA
V_{RESET}	Reset voltage $T_{min} \leq T_{amb} \leq T_{max}$	0.4 0.3	1.1	1.6 2.1	V
I_{RESET}	Reset current		10		pA

Table 8. Dynamic electrical characteristics
V_{CC} = +5 V, T_{amb} = +25 °C, reset to V_{CC} (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Timing accuracy (monostable) (1) R = 10 kΩ, C = 0.1 µF		5		%
	Timing shift with supply voltage variations (monostable) (1) R = 10 kΩ, C = 0.1 µF, V_{CC} = 5 V ± 1 V		1		%/V
	Timing shift with temperature (1) $T_{min} \leq T_{amb} \leq T_{max}$5		95		ppm/°C
f_{max}	Maximum astable frequency (2) R_A = 470 Ω, R_B = 200 Ω, C = 200 pF		1.8		MHz
	Astable frequency accuracy (2) R_A = R_B = 1 kΩto 100 kΩ, C = 0.1 µF	—	5	—	%
	Timing shift with supply voltage variations (astable mode) (2) R_A = R_B = 10 kΩ, C = 0.1 µF, V_{CC} = 5 to 12 V		0.9		%/V
t_R	Output rise time (C_{load} = 10 pF)		25		ns
t_F	Output fall time (C_{load} = 10 pF)		20		
t_{PD}	Trigger propagation delay		100		
t_{RPW}	Minimum reset pulse width (V_{trig} = 5 V)		350		

1. See *Figure 1*
2. See *Figure 2*

Table 9. Static electrical characteristics
V_{CC} = +12 V, T_{amb} = +25 °C, reset to V_{CC} (unless otherwise specified)

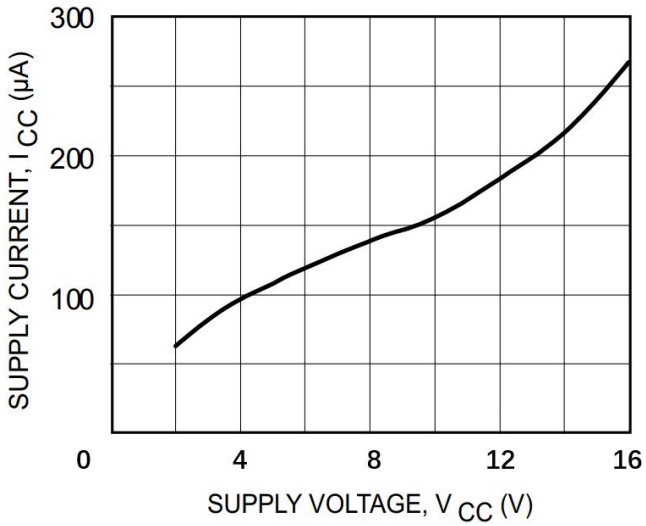
Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current (no load, high and low states) $T_{min} \leq T_{amb} \leq T_{max}$		190	450 450	µA
V_{CL}	Control voltage level $T_{min} \leq T_{amb} \leq T_{max}$	7.4 7.3	8	8.6 8.7	V
V_{DIS}	Discharge saturation voltage (I_{dis} = 80 mA) $T_{min} \leq T_{amb} \leq T_{max}$		0.09	1.5 2.0	
I_{DIS}	Discharge pin leakage current		2	200	nA
V_{OL}	Low level output voltage (I_{sink} = 50 mA) $T_{min} \leq T_{amb} \leq T_{max}$		1.2	2 2.8	V
V_{OH}	High level output voltage (I_{source} = -10 mA) $T_{min} \leq T_{amb} \leq T_{max}$	10.5 10.5	11		
V_{TRIG}	Trigger voltage $T_{min} \leq T_{amb} \leq T_{max}$	3.2 3.1	4	4.9 5.1	
I_{TRIG}	Trigger current		10		pA
I_{TH}	Threshold current		10		
V_{RESET}	Reset Voltage $T_{min} \leq T_{amb} \leq T_{max}$	0.4 0.3	1.1	1.7 2.2	V
I_{RESET}	Reset current		10		pA

Table 10. Dynamic electrical characteristics
V_{CC} = +12 V, T_{amb} = +25 °C, reset to V_{CC} (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Timing accuracy (monostable) (1) R = 10 kΩ, C = 0.1 µF, V_{CC} = +12 V8		6		%
	Timing shift with supply voltage variations (monostable) (1) R = 10 kΩ, C = 0.1 µF, V_{CC} = +5 V ±1 V		0.9		%/V
	Timing shift with temperature $T_{min} \leq T_{amb} \leq T_{max.}$, V_{CC} = +5 V		105		ppm/°C
f_{max}	Maximum astable frequency (2) R_A = 470 Ω, R_B = 200 Ω, C = 200 pF, V_{CC} = +5 V	—	1.8	—	MHz
	Astable frequency accuracy $R_A = R_B$ = 1 kΩto 100 kΩ, C = 0.1 µF, V_{CC} = +12 V		7		%
	Timing shift with supply voltage variations (astable mode) $R_A = R_B$ = 1 kΩto 100 kΩ, C = 0.1 µF, V_{CC} = 5 to +12 V		0.9		%/V

1. See *Figure 1*
2. See *Figure 2*

Figure 3. Supply current (per timer) versus supply voltage

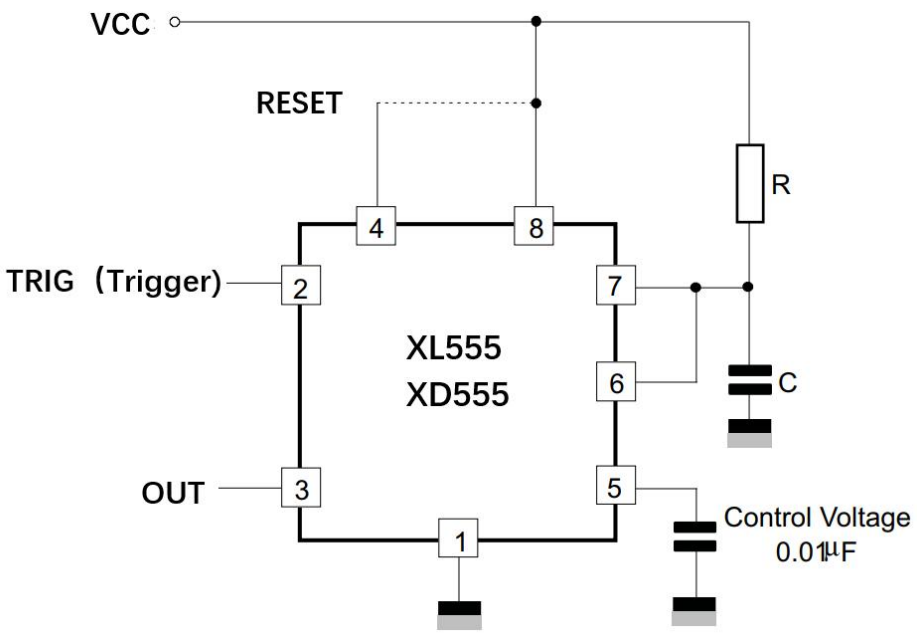


6. Application And PCB Layout

6.1. Monostable operation

In monostable mode, the timer operates like a one-shot generator. The external capacitor is initially held discharged by a transistor inside the timer, as shown following（*Figure 1*).

Figure 1. Application schematic



The circuit triggers on a negative-going input signal when the level reaches 1/3 VCC. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by t = 1.1 R x C.

Since the charge rate and threshold level of the comparator are both directly proportional to the supply voltage, the timing interval is independent of the supply. Applying a negative pulse simultaneously to the reset terminal (pin 4) and the trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle then starts on the positive edge of the reset pulse. While the reset pulse is applied, the output is driven to the LOW state.

When a negative trigger pulse is applied to pin 2, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant τ= R x C.

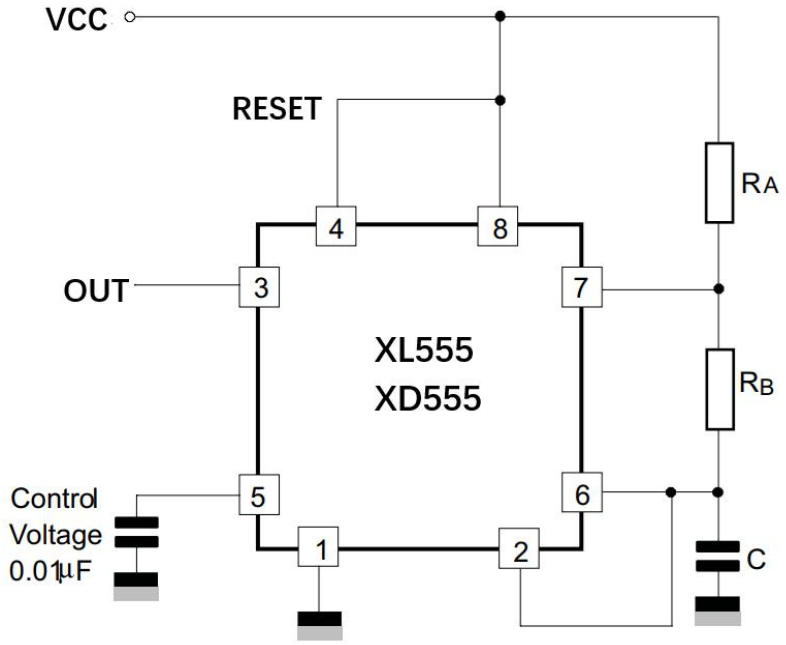
When the voltage across the capacitor equals 2/3 VCC, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state. When reset is not used, it should be tied high to avoid any false triggering.

6.2. Astable operation

When the circuit is connected as shown in Figure 2(pins 2 and 6 connected) it triggers itself and runs as a multi-vibrator. The external capacitor charges through RA and RB and discharges through RB only. Therefore, the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C charges and discharges between 1/3 VCC and 2/3 VCC. As in the triggered mode, the charge and discharge times, and therefore frequency, are independent of the supply voltage.

Figure 2. Application schematic



In this circuit, the charge time (output HIGH) is given by: t1 = 0.693 (RA + RB) C

The discharge time (output LOW) by: t2 = 0.693 x RB x C

Thus the total period T is given by: T = t1 + t2 = 0.693 (RA + 2RB) C

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(RA + 2RB)C}$$

The duty cycle is given by:

$$D = \frac{RB}{RA + 2RB}$$

6.3. Layout Guidelines

Standard PCB rules apply to routing the XL/XD555. The 0.1-µF ceramic capacitor in parallel with a 1- µF electrolytic capacitor must be as close as possible to the XL/XD555. The capacitor used for the time delay must also be placed as close to the discharge pin. A ground plane on the bottom layer can be used to provide better noise immunity and signal integrity.

Figure 3 is the basic layout for various applications， where:

C1—based on time delay calculations

C2—0.01-µF bypass capacitor for control voltage pin

C3—0.1-µF bypass ceramic capacitor

C4—1-µF electrolytic bypass capacitor

R1—based on time-delay calculations

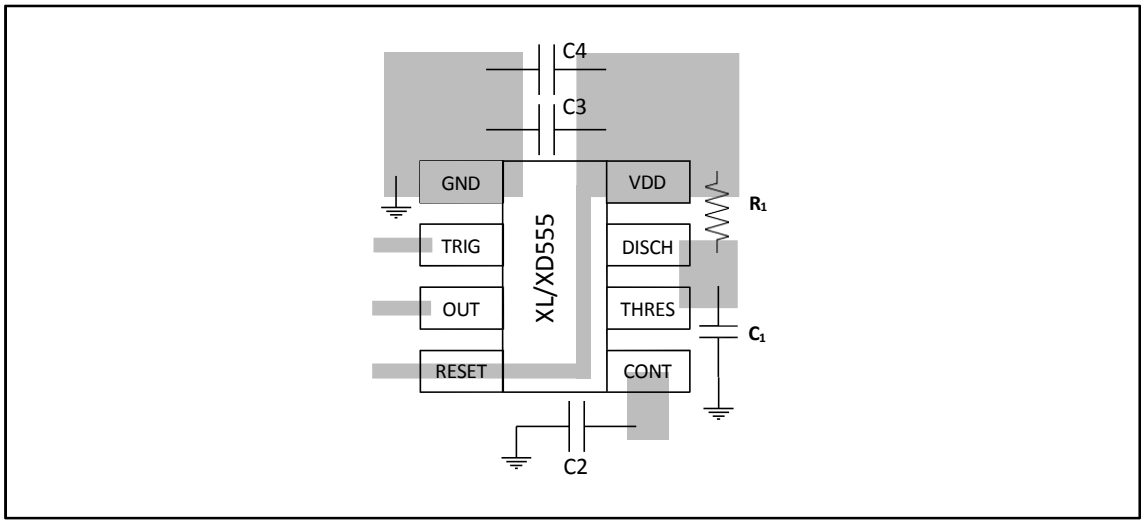


Figure 3. Layout Example

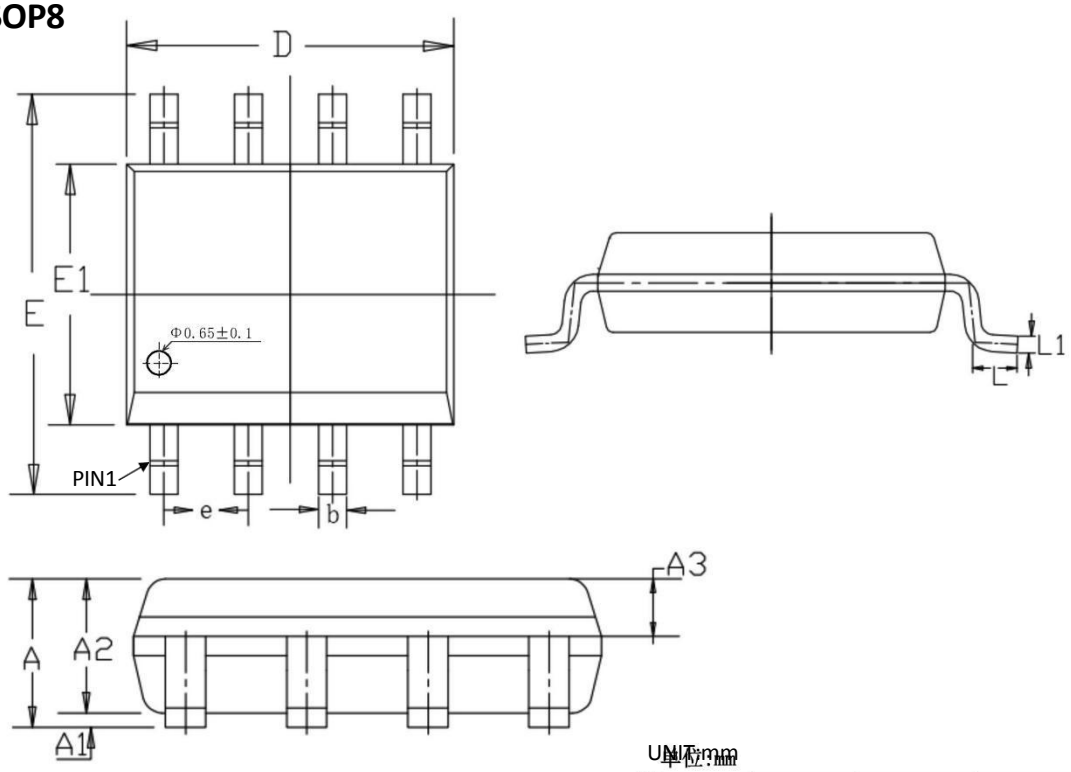
7. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (℃)	MSL	Transport Media	Package Quantity
XL555	XL555	SOP8	4.90 * 3.90	-40 to +85	MSL3	T&R	2500
XD555	XD555	DIP8	9.25 * 6.38	-40 to +85	MSL3	Tube 50	2000

8. DIMENSIONAL DRAWINGS

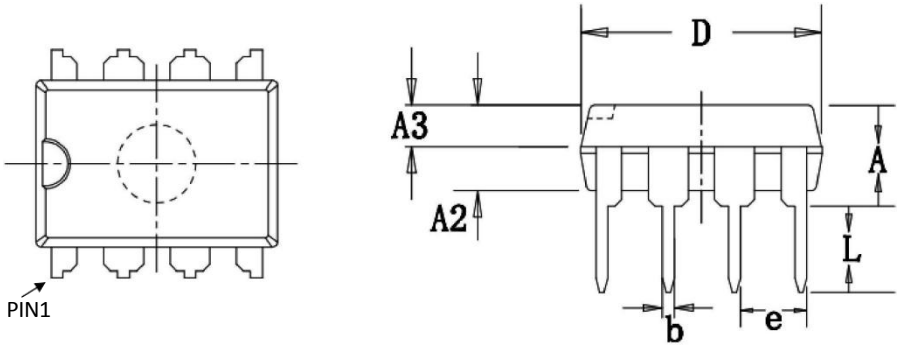
SOP8

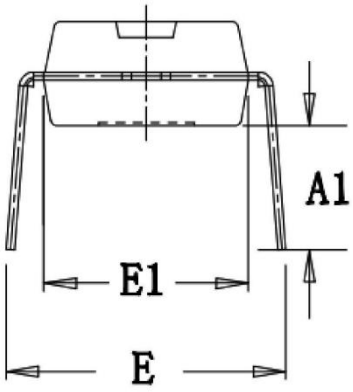


UNIT:mm
单位:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1(站高)	0.100	0.150	0.200
A2(厚度)	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e(脚间距)	1.240	1.270	1.300
D(长度)	4.800	4.900	5.000
E(跨度)	5.800	6.000	6.200
E1(宽度)	3.800	3.900	4.000
L(脚长)	0.450	0.600	0.750
L1	—	0.25BSC	—

DIP8





UNIT:mm

	MIN	NOM	MAX
A	3.600	3.800	4.000
A1	3.786	3.886	3.986
A2	3.200	3.300	3.400
A3	1.550	1.600	1.650
b	0.440	–	0.490
e	2.510	2.540	2.570
D	9.150	9.250	9.350
E(跨度)	7.800	8.500	9.200
E1(宽度)	6.280	6.380	6.480
L(脚长)	3.000	–	–