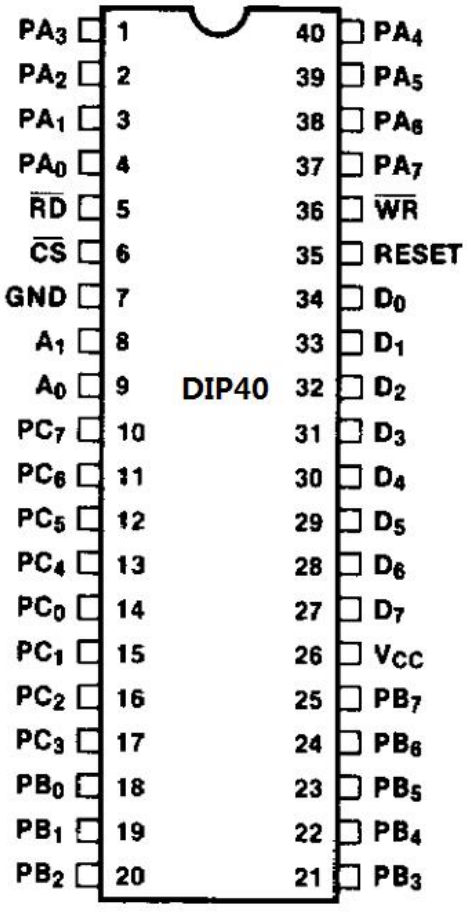
1. DESCRIPTION

The XD8255-2 and XD82C55-5 are general purpose programmable input/output devices designedfor use with 8080/8085 microprocessors.Twenty-four I/O lines may be programmed in two groupsof twelve(group I and group II) and used in three modes of operation.In the basic mode,(Mode0),each group of twelve I/O pins may be programmed in sets of 4 to input or output.In the strobedmode,(MODE 1), each group may be programmed to have 8 lines of input or output.Three of the remaining four pins in each group are used for handshaking strobes and interrupt control signals.The bidirectional bus mode,(MODE 2),uses the 8 lines of port A for a bi-directional bus,and five lines from port C for bus control signals.

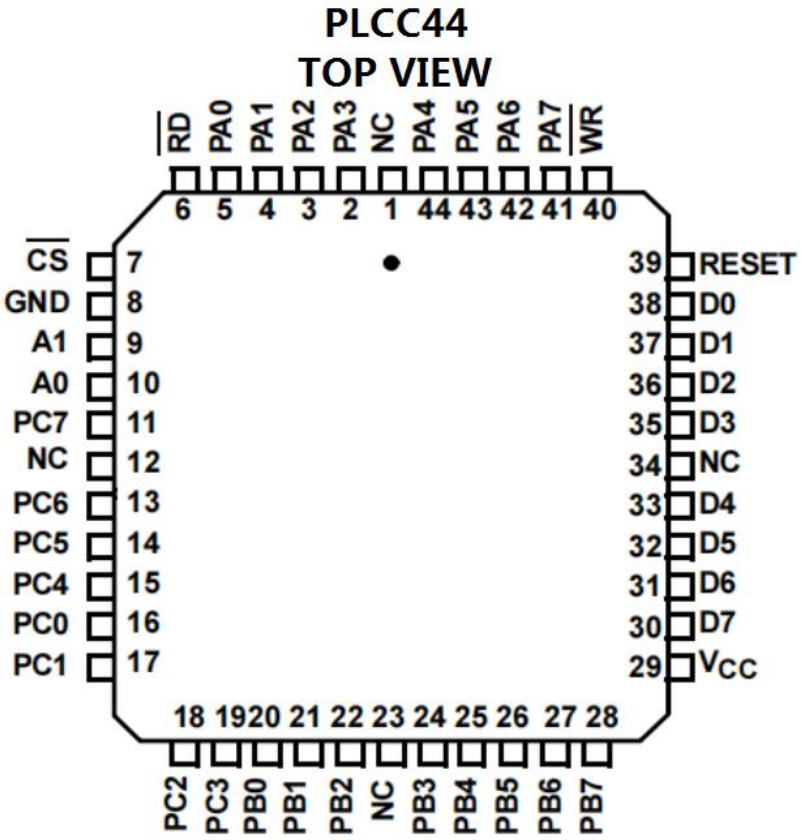
2. FEATURES

- Fully compatible with the 8080/8085 microprocessor families
- All inputs and outputs TTL compatible
- 24 programmable I/O pins
- Direct bit set/reset eases control application interfaces
- Eight Darlington drive outputs for printers and displays
- LSI drastically reduces system package count

3. PIN CONFIGURATION



(Top View)


PLCC44
TOP VIEW
RD
PA0
PA1
PA2
PA3
NC
PA4
PA5
PA6
PA7
WR
6 5 4 3 2 1 44 43 42 41 40
CS 7
GND 8
A1 9
A0 10
PC7 11
NC 12
PC6 13
PC5 14
PC4 15
PC0 16
PC1 17
39 RESET
38 D0
37 D1
36 D2
35 D3
34 NC
33 D4
32 D5
31 D6
30 D7
29 VCC
18 1920 21 22 23 24 25 26 27 28
PC2
PC3
PB0
PB1
PB2
NC
PB3
PB4
PB5
PB6
PB7

4. PIN IDENTIFICATION

No.	Symbol	Function
1-4,37-40	PA7-PA0	Port A(I/O)
5	$\overline{RD}$	Read input
6	CS	Chip select input
7	GND	Ground
8.9	A1,A0	Port address inputs
10-17	PC7-PC0	Port C (I/O)
18-25	PB7-PB0	Port B (I/O)
26	VCC	+5V power supply
27-34	D7-D0	Bidirectional data bus
35	RESET	Reset input
36	$\overline{WR}$	Write input

5. PIN FUNCTIONS

D7-D0(Data Bus Buffer)

These pins form a three-state,bidirectional data bus buffer that is controlled by input and output instructions executed by the processor.Control words and status information are also transmitted via D7-D0.

$\overline{CS}$(Chip Select)

A low input to this pin enables the XD8255 for communication with the 8080A/8085A.

$\overline{RD}$(Read)

A low input to this pin enables the XD8255 for communication with the 8080A/8085A.

$\overline{WR}$(Write)

A low input to this pin enables the data bus buffer to receive data or control words from the processor.

A1,A0 (Port Address)

These inputs are used in conjunction with $\overline{CS}$,$\overline{RD}$,and $\overline{WR}$ to control the selection of one of the three ports on the control word register.A0 and A1 are usually connected to A0 and A1 of the processor address bus.

RESET(Reset)

A high level input to this pin clears the control register and places ports A,B,and C in put mode.The input latches in ports A,B and C are not cleared.

PA7-PA0,PB7-PB0,PC7-PC0(Ports A,B,AND C)

These three 8-bit I/O ports can be configured to meet a variety of functional requirements through system software.The effectiveness and flexibility of the XD8255 are further enhanced by special features unique to each of the ports,as follows:

- Port A has an 8-bit data output latch/buffer,data input latch/buffer,and data input latch.
- Port B has an 8-bit data I/O latch/buffer and an 8-bit data input buffer.
- Port C has an 8-bit output latch/buffer and a data input buffer(input not latched).

Port C may be divided into two independent 4-bit control and status ports for use with ports A and B.

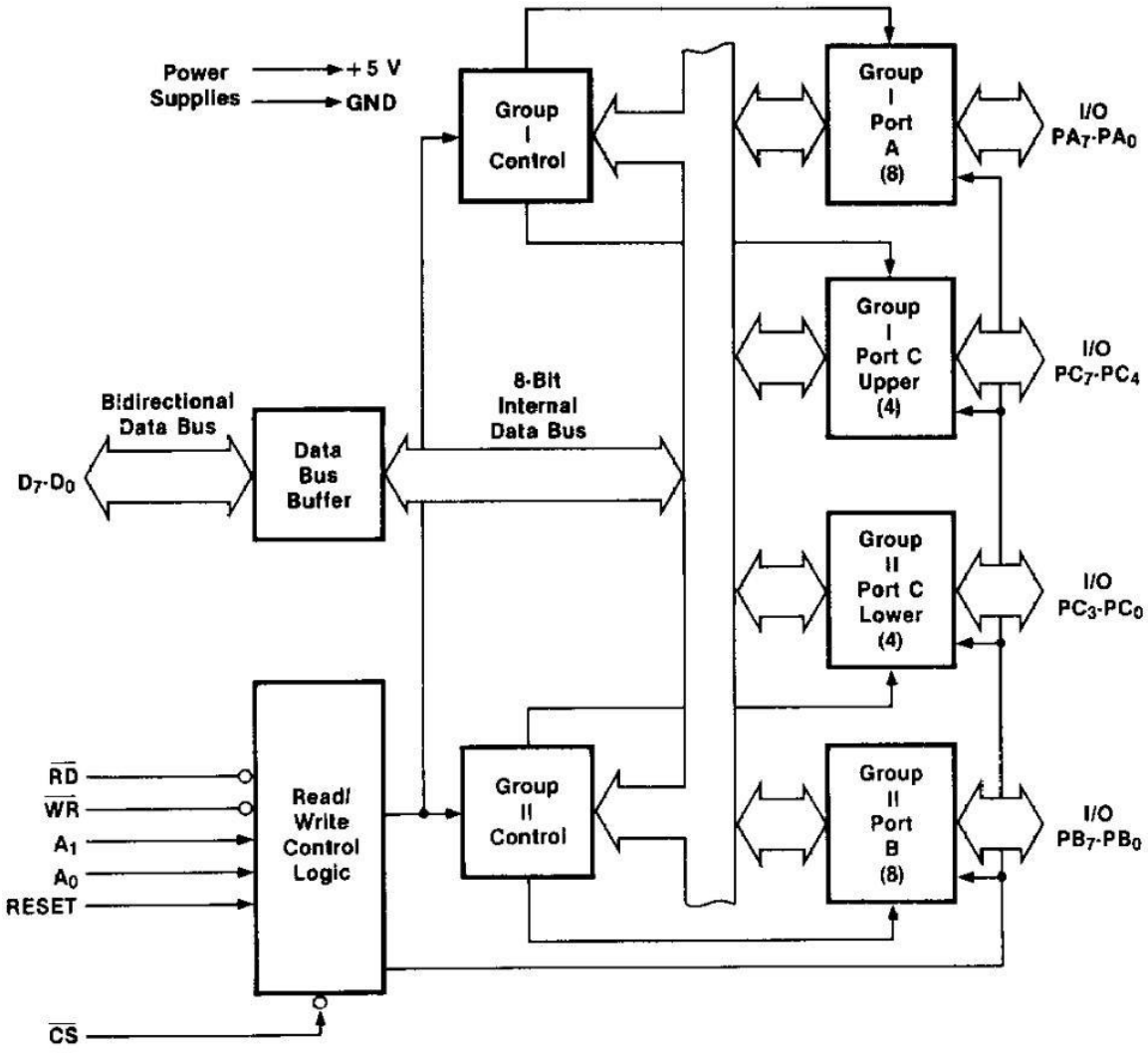
VCC

+5V power supply

GND(Ground)

Connection to ground

6. BLOCK DIAGRAM



7. FUNCTIONAL DESCRIPTION

The read/write and control logic manages all internal and external transfers of data,control,and status.It is through this block that the processor address and control buses control the peripheral interfaces.

Through an OUT instruction in system software from the processor,a control word is transmitted to the XD8255.Information such as the mode,bit set,and bit reset is used to initialize the functional configuration of each I/O port.

Both group I and group II accept commands from the read/write control logic and control words from the internal data bus and in turn controls its associated I/O ports,as follows:

Group I:port A and upper port C(PC7-PC4)

Group II:port B and lower port C(PC3-PC0)

While the control word register can be written to,the contents cannot be read back to the processor.

8. ABSOLUTE MAXIMUM RATINGS

T_A=25℃

Operating temperature,T_{OPT}	0℃ to +70℃
Storage temperature,T_{STG}	-65℃ to +150℃
Voltage on any pin with respect to V_{SS}	--0.5 to +7V

9. DC CHARACTERISTICS

Limits					
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Conditions**
Input low voltage	V_{IL}	-0.5	0.8	V	
Input high voltage	V_{IH}	2	V_{CC}	V	
Output low voltage	V_{OL}		0.45	V	
Output high voltage	V_{OH}	2.4		V	
Darlington drive current	I_{OH}	-1	-4	mA	V_{EXT}=1.5V R_{EXT}=750Ω
Power supply current	I_{CC}		120	mA	V_{CC}=+5V Output open
Input leakage current	I_{LIH}		10	μA	V_{IN}=0.4V
Input leakage current	I_{LIL}		-10	μA	V_{IN}=0.4V
Output leakage current	I_{LOH}		±10	μA	V_{OUT}=V_{CC} CS=2.0V
Output leakage current	I_{LOL}		-10	μA	V_{OUT}=0.4V CS=2.0V

10. CAPACITANCE

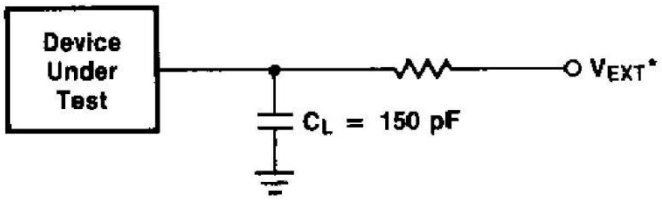
T_A=25℃;V_{CC}=0V

Limits					
Parameter	Symbol	Min	Max	Unit	Conditions
Input capacitance	C_I		10	pF	fc =1MHz Unmeasured pins returned to Vss
I/O capacitance	C_{IO}		20	pF	

11. AC CHARACTERISTICS

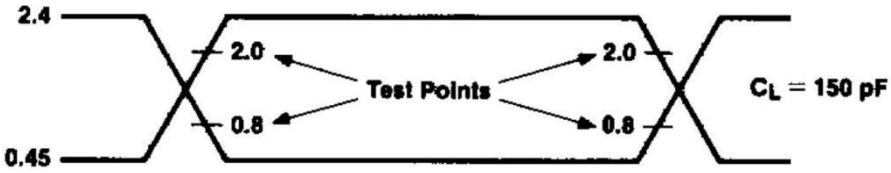
		8255-2 Limits		82C55-5 Limits			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
Address stable before READ	t_{AR}	0		0		ns	
Address stable after READ	t_{RA}	0		0		ns	
READ pulse width	t_{RR}	20		250		ns	
Data valid from $\overline{READ}$	t_{RD}		140		170	ns	C_L=150pF
Data float after $\overline{READ}$	t_{DF}		100		100	ns	C_L=100pF
		10		10			C_L=15pF
Time between $\overline{READ}$S and /$\overline{WRITE}$S	t_{RV}	200		850		ns	
Write							
Address stable before WRITE	t_{AW}	0		0		ns	
Address stable after $\overline{WRITE}$	t_{WA}	20		20		ns	
$\overline{WRITE}$ pulse width	t_{WW}	200		250		ns	
Data valid to $\overline{WRITE}$	t_{DW}	100		100		ns	
Data valid after $\overline{WRITE}$	t_{WD}	0		0		ns	
Other Timing							
$\overline{WR}$=0 to output	t_{WB}		350		350	ns	C_L=150pF
Peripheral data before $\overline{RD}$	t_{IR}	0		0		ns	
Peripheral data after $\overline{RD}$	t_{HR}	0		0		ns	
$\overline{ACK}$ pulse width	t_{AK}	300		300		ns	
$\overline{STB}$ pulse width	t_{ST}	350		350		ns	
Per.data before T.E. of $\overline{STB}$	t_{PS}	0		0		ns	
Per.data after T.E. of STB	t_{PH}	150		150		ns	
$\overline{ACK}$=0 to output	t_{AD}		300		300	ns	C_L=150pF
$\overline{ACK}$=0 to output float	t_{KD}		250		250		C_L=50pF
		20		20		ns	C_L=15pF
$\overline{WR}$=1 to 0BF =0	t_{WOB}		300		650	ns	
$\overline{ACK}$ =0 to OBF=1	t_{AOB}		350		350	ns	
$\overline{STB}$=0 to IBF =1	t_{SIB}		300		300	ns	
$\overline{RD}$ =1 to IBF=0	t_{RIB}		300		300	ns	
$\overline{RD}$ =0 to INTR=0	t_{RIT}		400		400	ns	
$\overline{STB}$ =1 to INTR=1	t_{SIT}		300		300	ns	C_L=150pF
$\overline{ACK}$ =1 to INTR=1	t_{AIT}		350		350	ns	
$\overline{WR}$ =0 to INTR=0	t_{WIT}		450		850	ns	C_L=150pF

12. AC TESTING LOAD CIRCUIT

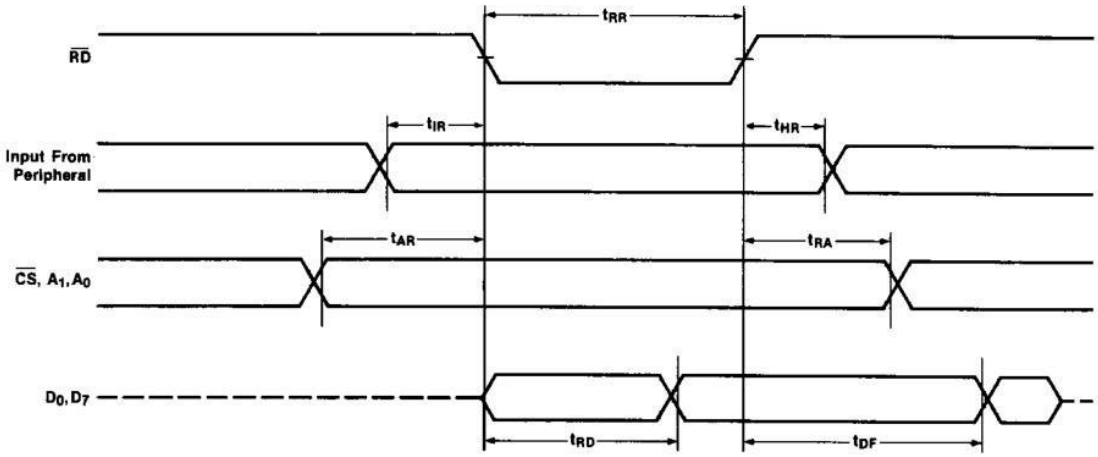


*V_{EXT} is set at various voltages during testing to guarantee the specification

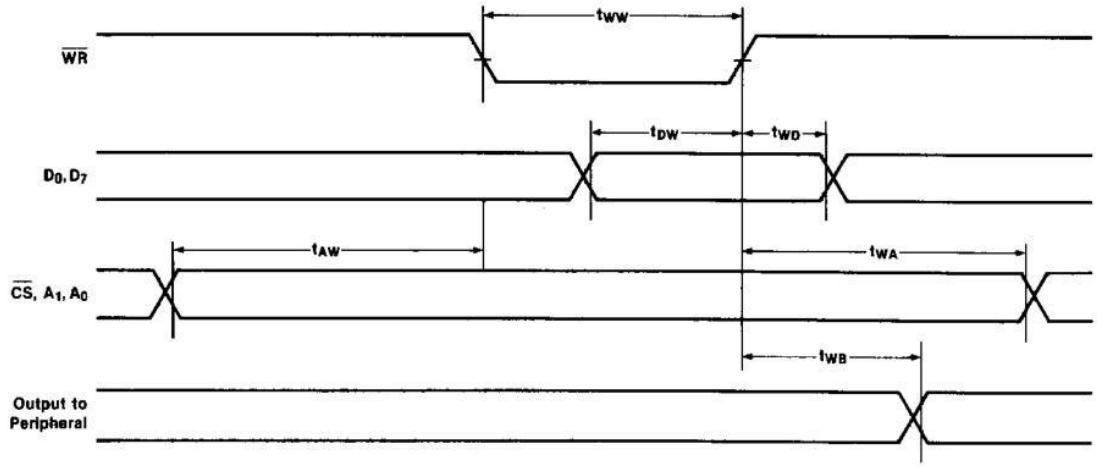
13. TIMING WAVEFORM



Mode 0

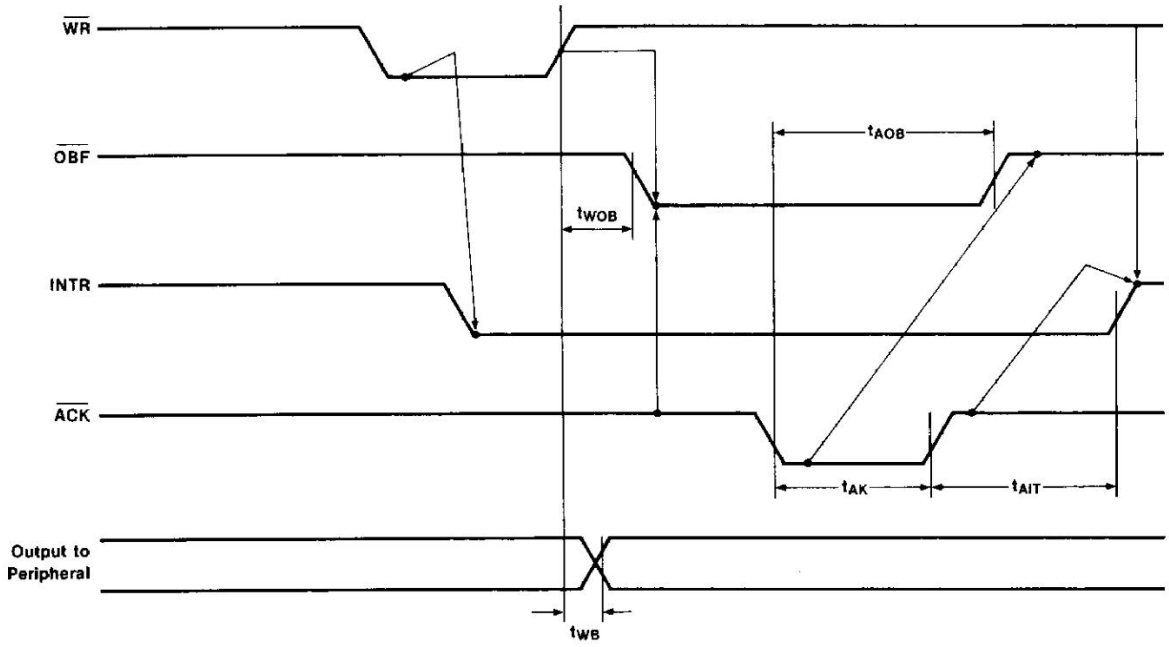


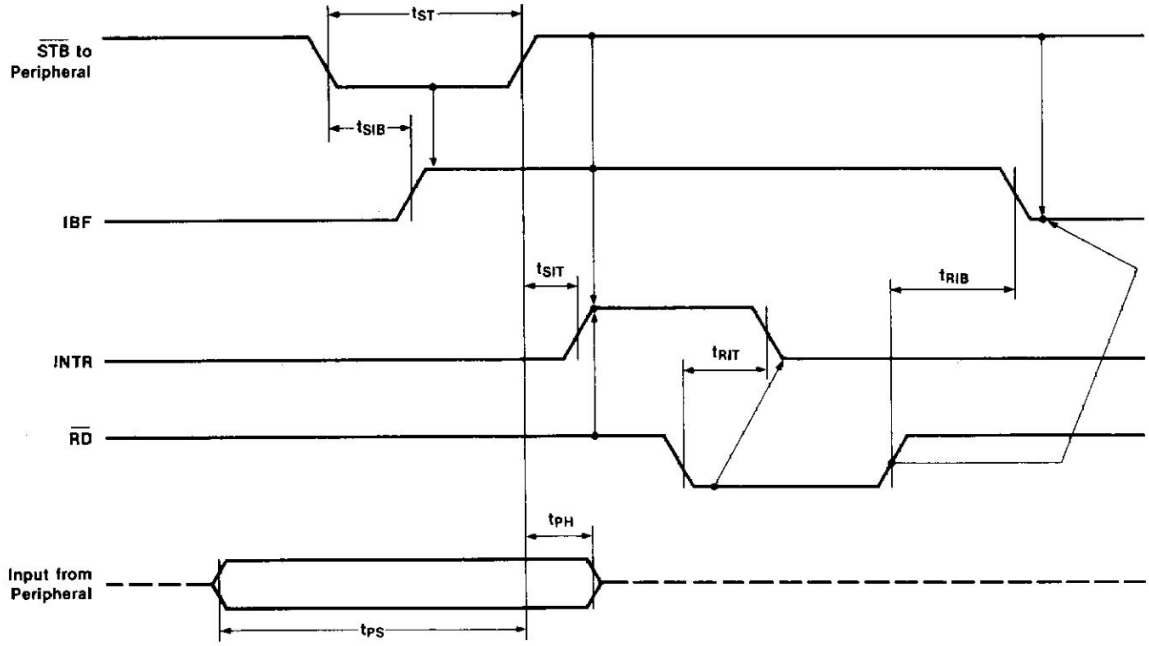
Basic Input (READ)



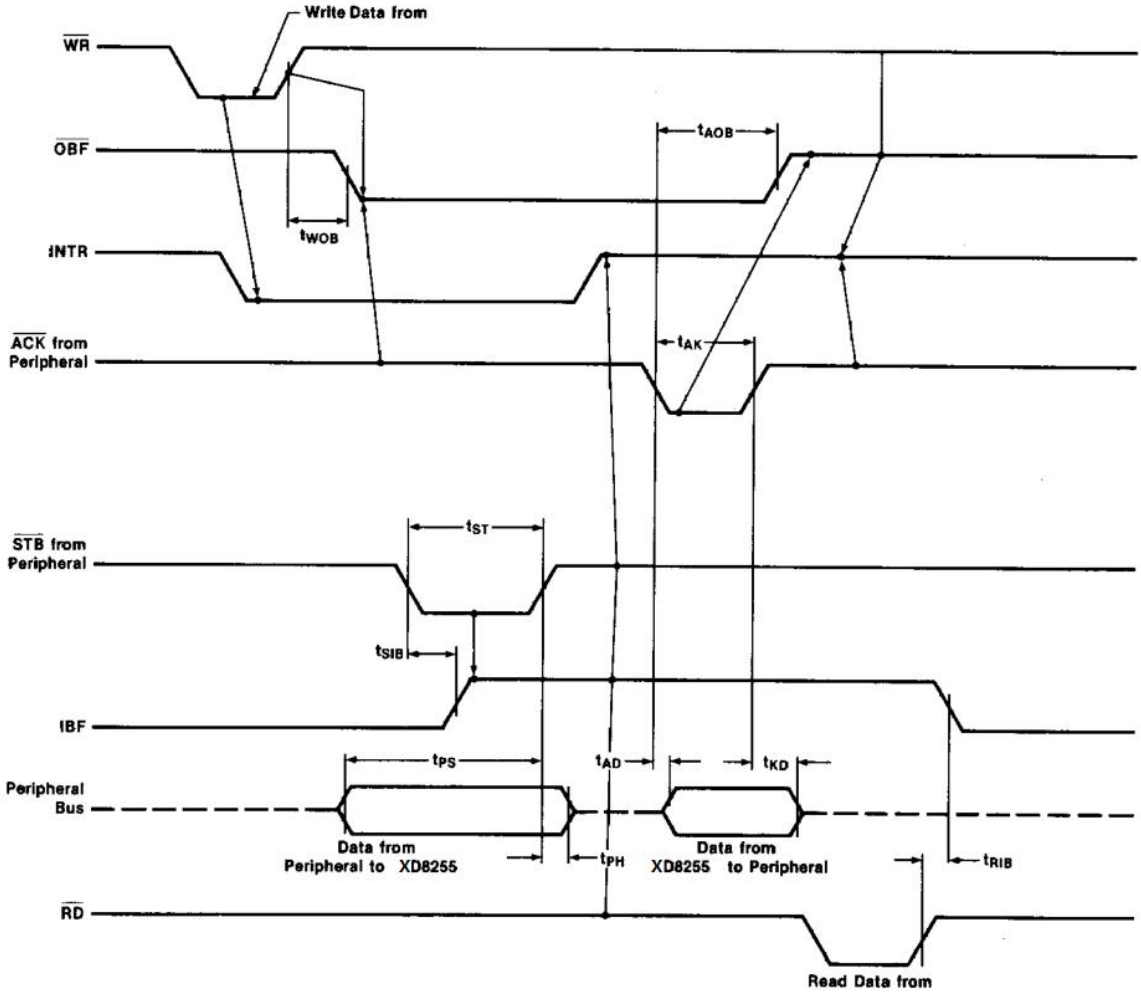
Basic Output (WRITE)

Mode 8


WR
OBF
INTR
ACK
Output to Peripheral
tAOB
tWOB
tAK
tAIT
tWB


STB to Peripheral
IBF
INTR
RD
Input from Peripheral
tST
tSIB
tSIT
tRIB
tRIT
tPH
tPS

Mode 2



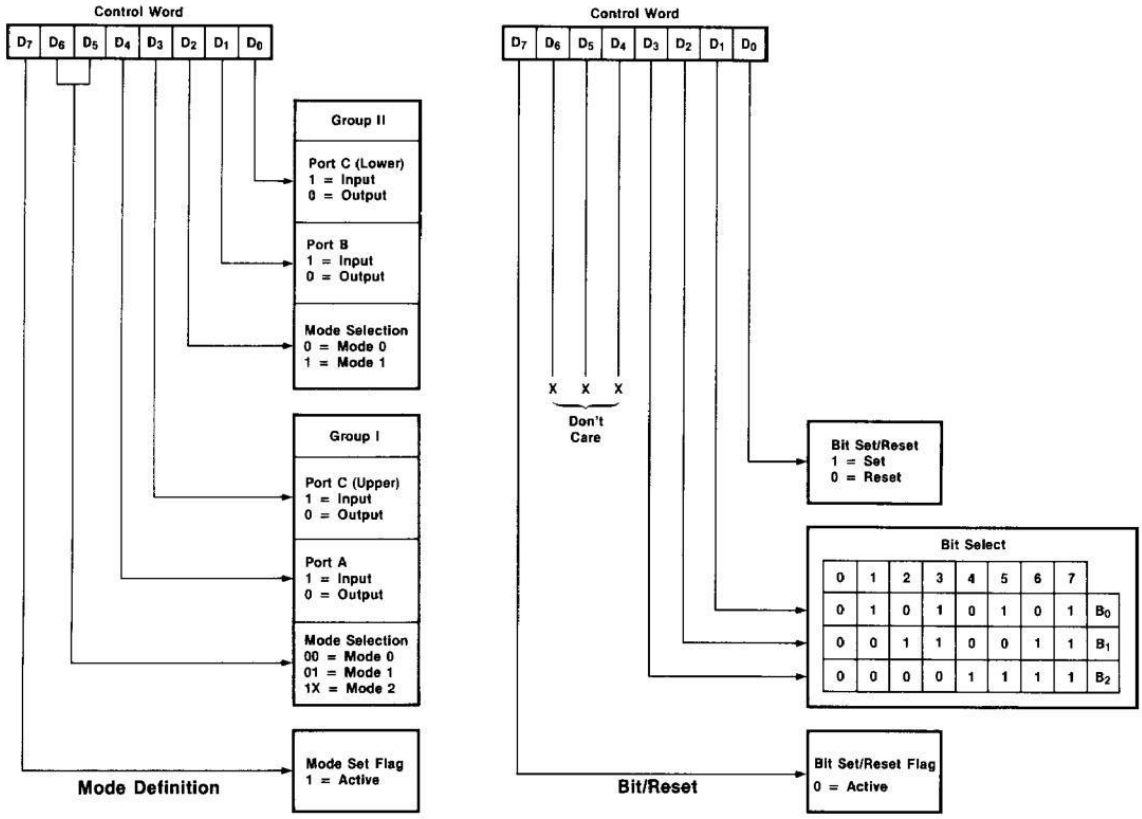
Note:

(1) Any sequence where WR occurs before ACK and STB occurs before RD is permissible (INTR = IBF · MASK · STB · RD+ OBF · MASK · ACK · WR).

(2) When the XD8255 is set to Mode 1 or 2,OBF is reset to be high(logic 1).

14. FORMATS

Mode Definition,Bit/Rest Format



Modes

The XD8255 can be operated in mode 0,1 or 2 which are selected by appropriate control words and detailed below.

Mode 0

Mode 0 provides basic input and output operation through each of the ports A,B,and C.Output data is latched and input data follows the peripheral.No “handshaking”strobes are needed.

- 16 different configurations in mode 0
- Two 8-bit ports and two 4-bit ports
- Inputs are not latched
- Outputs are latched

Mode 1

Mode 1 provides for strobed input and output operations with data transferred through port A or B and handshaking through port C.

- Two I/O groups(I and II)
- Both groups contain an 8-bit data port and a 4-bit control/data port.
- Both 8-bit data ports can be either latched input or latched output

Mode 2

Mode 2 provides for strobed bidirectional operation using PA0PA.7 as the bidirectional latched data bus.PC3PC7 is used for interrupts and “handshaking” bus flow control similar to mode 1.Note that PB0PB7 and PC0PC2 may be defined as mode 0 or 1,input or output in conjunction with port A in mode 2.

- An 8-bit latched bidirectional bus port (PA0-PA7) and a 5-bit control port (PC3PC7)
- Both inputs and outputs are latched
- An additional 8-bit input or output port with a 3-bit control port.

Basic Operation

Input Operation(Read)

A1	A0	RD	WR	CS	
0	0	0	1	0	PORT A→DATA BUS
0	1	0	1	0	PORT B→DATA BUS
1	0	0	1	0	PORT C→DATA BUS

Output Operation(Write)

A1	A0	RD	WR	CS	
0	0	1	0	0	DATA BUS→PORT A
0	1	1	0	0	DATA BUS→PORT B
1	0	1	0	0	DATA BUS→PORT C
1	1	1	0	0	DATA BUS→CONTROL

Disable Function

A1	A0	RD	WR	CS	
X	X	X	X	1	DATA BUS→HIGH Z STATE
X	X	1	1	0	DATA BUS→HIGH Z STATE

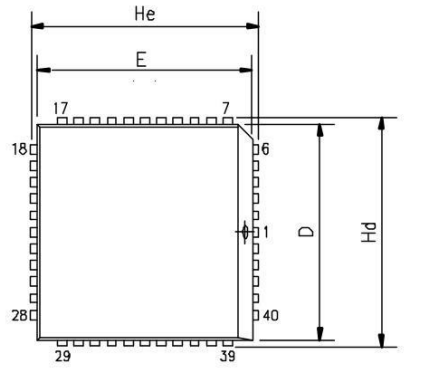
15. ORDERING INFORMATION

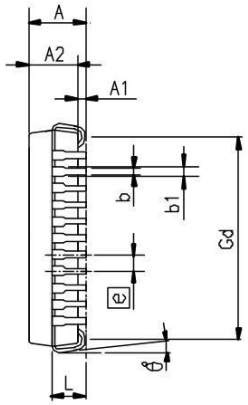
Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XD8255-2	XD8255-2	DIP40	52.32 * 13.80	-40 to +85	MSL3	Tube 9	180
XP8255	XP8255	PLCC44	16.58 * 16.58	-40 to +85	MSL3	T&R	500
XD82C55-5	XD82C55-5	DIP40	52.32 * 13.80	-40 to +85	MSL3	Tube 9	180

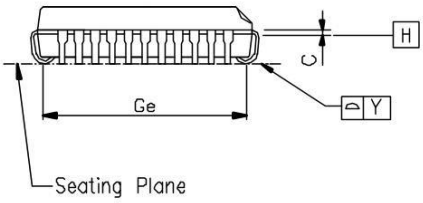
16. DIMENSIONAL DRAWINGS

PLCC44

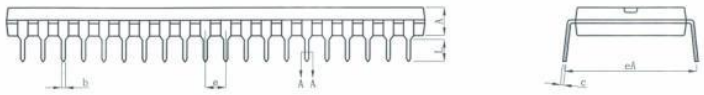




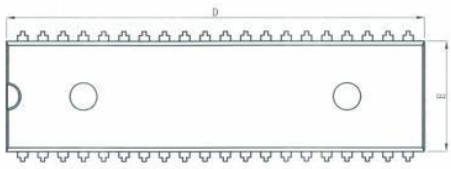
SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	4.191	–	4.572
A1	0.508	–	–
A2	3.734	–	4.013
b1	0.660	0.711	0.813
b	0.330	0.432	0.533
c	0.178	0.254	0.330
D	16.510	16.586	16.662
E	16.510	16.586	16.662
e	1.270 BSC		
Gd	14.986	15.494	16.002
Ge	14.986	15.494	16.002
Hd	17.399	17.526	17.653
He	17.399	17.526	17.653
L	2.540	–	2.845
Y	–	–	0.102

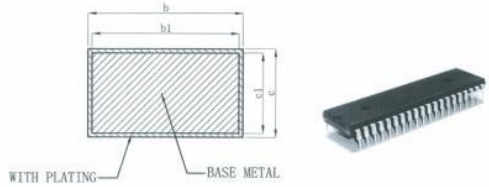


DIP40



symbol	millimeter		
	Min	Nom	Max
A	3.40	3.50	3.60
b	0.44	——	0.53
b1	0.43	0.46	0.49
c	0.25	——	0.30
c1	0.24	0.25	0.26
D	52.22	52.32	52.42
E	13.70	13.80	13.90
e	2.54BSC		
eA	15.24	——	17.21
L	3.00	——	——





SECTION A-A

[if you need help contactus. Xinluda reserves the right to change the above information without prior notice]