Opto-Compatible Single Channel Isolated Smart Gate Driver

1. Features

- 6.0A peak source and sink output current
- 250ns maximum propagation delay
- 1.8A internal active miller clamp
- Desaturation detection: 6.5V/9.0V
- Under voltage lock-out protection (UVLO)
- Open drain isolated fault feedback
- Soft turn-off
- Automatic fault reset /Input signal reset
- 50ns maximum pulse width distortion (PWD)
- 150kV/us minimum CMTI
- Wide V_{CC2} operating range: 13V to 33V
- Wide temperature range: -40°C to 125°C
- RoHS-compliant, WB SOIC-16 package
- Safety and regulatory approvals：
  - ➢ 5700V_{RMS} for 1 minute per UL 1577

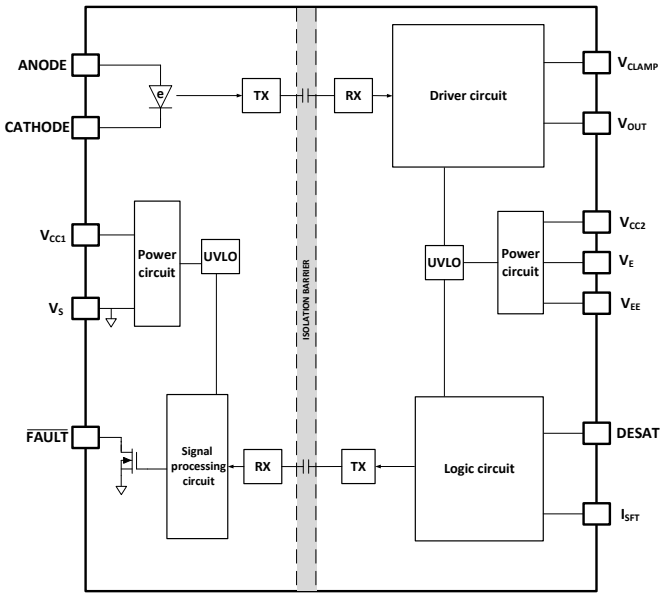
2. Applications

- Industrial inverters
- Uninterruptible Power Supply (UPS)
- AC and Brushless DC motor drive
- Isolated switch mode power supplies
- Isolated IGBT/Power MOSFET gate driver

Device Information

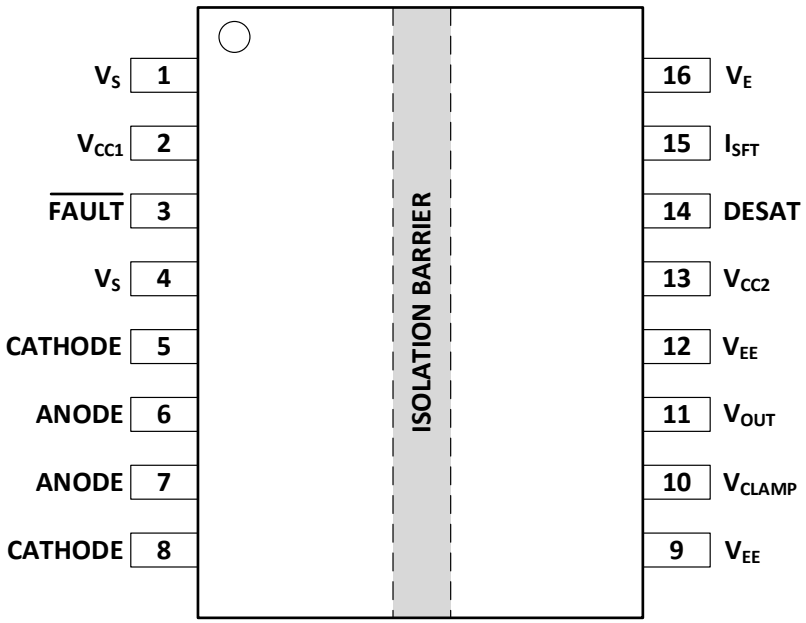
PART NUMBER	V_{DESAT}	RESET	PACKAGE
CI-311J-500E	6.5V	Automatic	WB SOIC-16
CI-311J-500B	9.0V	Automatic	WB SOIC-16
CI-311J-500EA	6.5V	Signal Reset	WB SOIC-16
CI-311J-500BA	9.0V	Signal Reset	WB SOIC-16

Functional Block Diagram



4. Pin Configuration and Functions

CI-331J-500X(WB SOIC-16)



Pin Map and Functions

NAME	NO.	I/O(1)	DESCRIPTION
V_S	1	G	Input power supply and logic ground reference.
V_{CC1}	2	P	Input power supply from 3V to 5.5V, by passing a > 100nF capacitor to GND.
$\overline{FAULT}$	3	O	Fault output.
V_S	4	G	Input power supply and logic ground reference.
CATHODE	5	I	Cathode.
ANODE	6	I	Anode.
ANODE	7	I	Anode.
CATHODE	8	I	Cathode.
V_{EE}	9	P	Negative supply voltage.
V_{CLAMP}	10	O	Internal Active miller clamp.
V_{OUT}	11	O	Gate drive voltage output.
V_{EE}	12	P	Negative supply voltage.
V_{CC2}	13	P	Positive supply voltage.
DESAT	14	I	Desaturation voltage input.
I_{SFT}	15	I	Soft turn off current set.
V_E	16	G	Common (IGBT emitter) output supply voltage.

(1) P = Power, G = Ground, I = Input, O = Output

5. Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Operating Temperature	T_A	-40	125	°C
Average Forward Input Current	$I_{F(AVG)}$		25	mA
Peak Transient Input Current (< 1us pulse width, 300pps)	$I_{F(TRAN)}$		1	A
Reverse Input Voltage	V_R		5	V
Positive Input Supply Voltage	V_{CC1}	-0.5	7.0	V
FAULT Output Current	I_{FAULT}		8.0	mA
FAULT Pin Voltage	V_{FAULT}	-0.5	V_{CC1}	V
Total Output Supply Voltage	(V_{CC2} - V_{EE})	-0.5	36	V
Negative Output Supply Voltage	(V_E - V_{EE})	-0.5	15	V
Positive Output Supply Voltage	(V_{CC2} - V_E)	-0.5	36 - (V_E - V_{EE})	V
Gate Drive Output Voltage	$V_{O(PEAK)}$	-0.5	V_{CC2}	V
Peak Clamping Sinking Current	I_{Clamp}		2	A
Miller Clamping Pin Voltage	V_{Clamp}	-0.5	V_{CC2}	V
DESAT Voltage	V_{DESAT}	V_E	V_{CC2}	V
Output Power Dissipation	P_O		600	mW
Input IC Power Dissipation	P_I		150	mW

5.2 ESD Ratings

PARAMETER		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP155 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Total Output Supply Voltage	(V_{CC2}-V_{EE})	13	33	V
Negative Output Supply Voltage	(V_E - V_{EE})	0	15	V
Positive Output Supply Voltage	(V_{CC2} - V_E)	13	33-(V_E-V_{EE})	V
Input Current (ON)	$I_{F(ON)}$	8	12	mA
Input Voltage (OFF)	$V_{F(OFF)}$	-3.6	0.8	V
Operating Temperature (Ambient)	T_A	-40	125	°C

5.4 Thermal Information

SYMBOL	PARAMETER	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	28.5	°C/W

5.5 Power Ratings

SYMBOL	DESCRIPTION	TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	V_{CC1} = 5V, V_{CC2}-V_E = 20V, V_E-V_{EE} = 5V, IN+/- = 5V, 150kHz, 50% Duty Cycle for 10nF load, T_A=25°C	990	mW
P_{D1}	Maximum power dissipation by transmitter side		120	mW
P_{D2}	Maximum power dissipation by receiver side		870	mW

5.6 Insulation Specifications

SYMBOL	DESCRIPTION	TEST CONDITIONS	VALUE	UNIT
CLR	External clearance	Shortest terminal-to-terminal distance through air	≥ 8	mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	≥ 8	mm
CTI	Comparative tracking index	DIN IEC 112/VDE 0303 Part 1	≥ 600	V
	Material Group	Material Group (DIN VDE 0110, 1/89)	I	
		Rated mains voltage ≤ 600V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17):2021-10				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST}=V_{IOTM}, t = 60s (qualification test) V_{TEST}=1.2 x V_{IOTM}, t = 1s (100% production test)	8060	V_{PK}

V_{IOSM}	Maximum surge isolation voltage	Test method per IEC 62368-1, 1.2/50μs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	6250	V_{PK}
q_{pd}	Apparent charge	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; Vpd(m) = 1.2 × V_{IORM} = 2545V_{PK}, t_m = 10s	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; Vpd(m) = 1.6 × V_{IORM} = 3394V_{PK}, t_m = 10s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test) $V_{ini} = V_{IOTM}$, t_{ini} = 1s; Vpd(m) = 1.875 × V_{IORM} = 3977V_{PK}, t_m = 1s	≤ 5	
C_{IO}	Capacitance (Input to Output)	V_{IO} = 0.4*sin (2πft), f = 1MHz	1	pF
R_{IO}	Insulation resistance, input to output	V_{IO} = 500V, T_A = 25°C	≥ 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	≥ 10^{11}	
		V_{IO} = 500V at T_S = 150°C	≥ 10^9	
Pollution degree			2	
Climatic category			40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	5700	V_{RMS}

5.7 Safety Limiting Values

SYMBOL	DESCRIPTION	TEST CONDITIONS	VALUE	UNIT
I_S	Safety input	$R_{\theta JA}$ =105°C/W, V_{CC2} = 15V, V_{EE}=-5V, T_J = 150°C, T_A= 25°C	90	mA
P_S	Safety input, output, or total power		1000	mW
T_S	Safety temperature (1)		150	°C

(1) $T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.$P_S = I_S \times V_I$, where V_I is the maximum supply voltage.

5.8 Electrical Characteristics

Unless otherwise noted, all typical values at T_A = 25°C, V_{CC2} - V_{EE} = 30 V, V_E - V_{EE} = 0 V; all Minimum/Maximum specifications are at recommended operating conditions.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FAULT}	FAULT Logic Low Output Voltage	I_{FAULT} = 1.1 mA, V_{CC1} = 5.5V		0.1	0.4	V
I_{FAULTH}	FAULT Logic High Output Current	V_{FAULT} = 5.5 V, V_{CC1} = 5.5V		0.02	0.5	uA
I_{OH}	High Level Output Current	V_O = V_{CC2} - 15		6		A
I_{OL}	Low Level Output Current	V_O = V_{EE} + 15		-6		A
I_{OLF}	Low Level Soft Turn-off Current During Fault Condition	V_O - V_{EE} = 14 V		140		mA
V_{OH}	High Level Output Voltage	I_O = -100 mA	V_{CC2}-0.2	V_{CC2}-0.1		V
V_{OL}	Low Level Output Voltage	I_O = 100 mA		0.1	0.2	V
V_{tclamp}	Clamp Pin Threshold Voltage			2		V
I_{CL}	Clamp Low Level Sinking Current	V_O = V_{EE} + 2.5	0.99	1.8	2.8	A
I_{CC2H}	High Level Supply Current	I_O = 0 mA		2.5	5	mA
I_{CC2L}	I_O = 0 mA	I_O = 0 mA		1.7	3	mA
I_{CHG}	Blanking Capacitor Charging Current	V_{DESAT} = 2 V	-0.13	-0.24	-0.33	mA
I_{DSCHG}	Blanking Capacitor Discharge Current	V_{DESAT} = 7.0 V	10	30		mA
V_{DESAT1}	DESAT Threshold Pai8263xE	V_{CC2} -V_E >VUVLO-	6	6.5	7.5	V
V_{DESAT2}	DESAT Threshold Pai8263xF	V_{CC2} -V_E >VUVLO-	8.5	9.0	9.5	V
V_{UVLO+}	UVLO Threshold +	V_O > 5 V	10.5	11.6	12.5	V
V_{UVLO-}	UVLO Threshold -	V_O < 5 V	9.2	10.3	11.1	V
(V_{UVLO+}- V_{UVLO-})	UVLO Hysteresis		0.4	1.3		V
I_{FLH}	Threshold Input Current Low to High	I_O = 0 mA, V_O > 5 V		2	6	mA
V_{FHL}	Threshold Input Voltage High to Low		0.8			V
V_F	Input Forward Voltage	I_F = 10 mA	1.95	2.1	2.25	V
BV_R	Input Reverse Breakdown Voltage		5			V
C_{IN}	Input Capacitance	f = 1 MHz, V_F = 0 V		6		pF

5.9 Switching Characteristics

Unless otherwise noted, all typical values at T_A = 25°C, V_{CC2} - V_{EE} = 30 V, V_E - V_{EE} = 0 V; all Minimum/Maximum specifications are at recommended operating conditions.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation Delay Time to High Output Level	Rg = 10 Ω, Cg = 10 nF, f = 10 kHz, Duty Cycle = 50%, I_F = 10 mA, V_{CC2} = 30 V	100	180	250	ns
t_{PHL}	Propagation Delay Time to Low Output Level		100	180	250	ns
PWD	Pulse Width Distortion |t_{PHL} - t_{PLH}|				50	ns
t_{sp-kk}	Propagation Delay Difference Between Any Two Parts or Channels		-150		150	ns
t_R	Rise Time			50		ns
t_F	Fall Time			50		ns
$t_{DESAT(90\%)}$	DESAT Sense to 90% V_O Delay	C_{DESAT} = 100pF, Rg = 10Ω, Cg = 10 nF, V_{CC2} = 30 V		0.15	0.5	us
$t_{DESAT(10\%)}$	DESAT Sense to 10% V_O Delay	C_{DESAT} = 100pF, Rg = 10Ω, Cg = 10 nF, V_{CC2} = 30 V		2	3	us
$t_{DESAT(FAULT)}$	DESAT Sense to Low Level FAULT Signal Delay	C_{DESAT} = 100 pF, R_F = 2.1 kΩ, C_F = Open, Rg = 10 Ω, Cg = 10 nF, V_{CC2} = 30 V		0.25	0.5	us
$t_{DESAT(LOW)}$	DESAT Sense to DESAT Low Propagation Delay	C_{DESAT} = 100pF, R_F = 2.1 kΩ, Rg = 10 Ω, Cg = 10 nF, V_{CC2} = 30 V		0.25		us
$t_{DESAT(MUTE)}$	DESAT Input Mute	C_{DESAT} = 100pF, R_F = 2.1 kΩ, Rg = 10 Ω, Cg = 10 nF, V_{CC1} = 5.5V, V_{CC2} = 30 V	15	26	40	us
CMTI	Common Mode Transient Immunity		150			kV/μs

5.10 Parameter Measurement Information

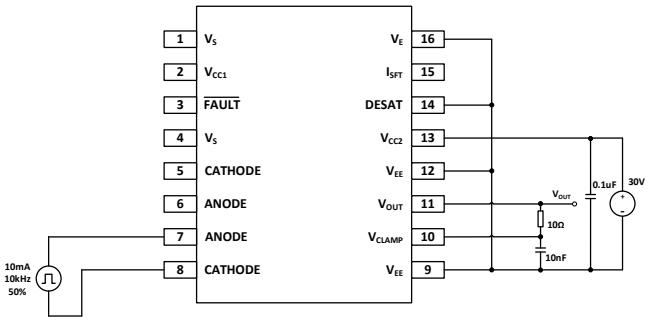


Figure 1. t_{PLH}, t_{PHL}, t_r, t_f, test circuit

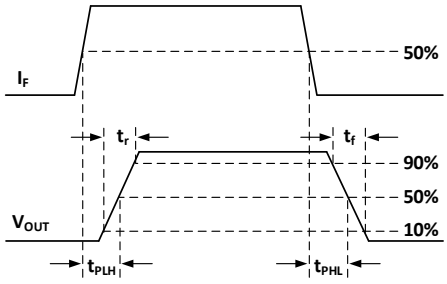


Figure 2. V_{OUT} propagation delay waveforms

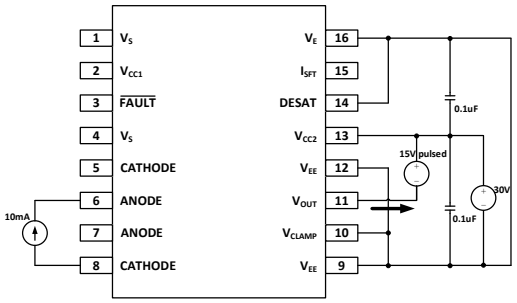


Figure 3. I_{OH} pulsed test circuit

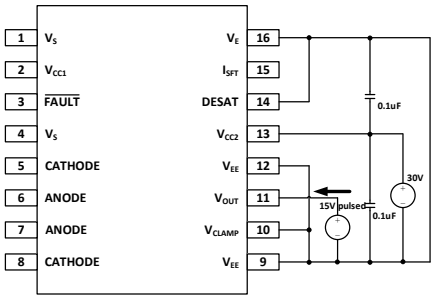


Figure 4. I_{OL} pulsed test circuit

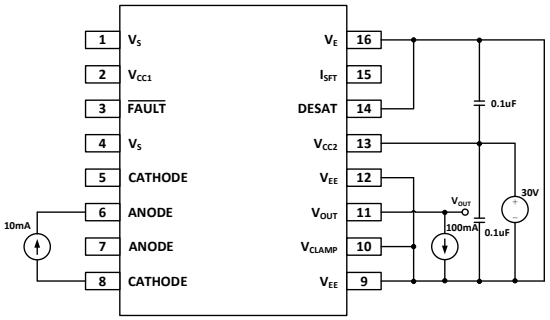


Figure 5. V_{OH} pulsed test circuit

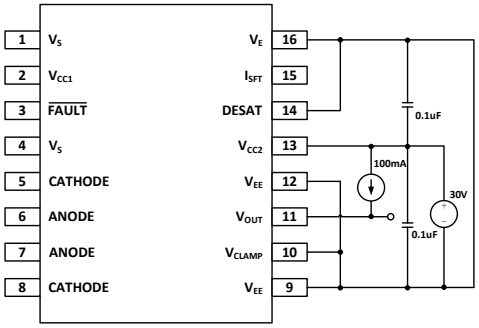


Figure 6. V_{OL} pulsed test circuit

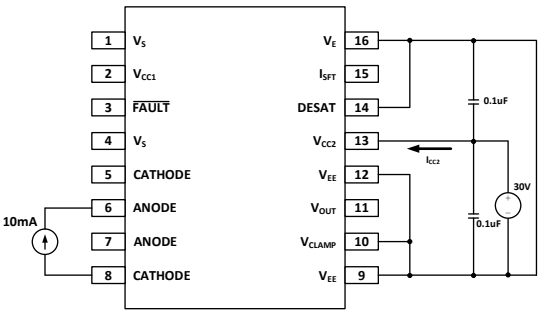


Figure 7. I_{CC2H} test circuit

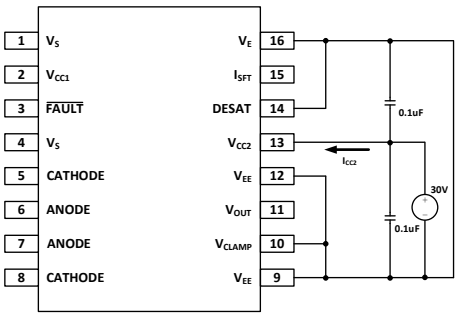


Figure 8. I_{CC2L} test circuit

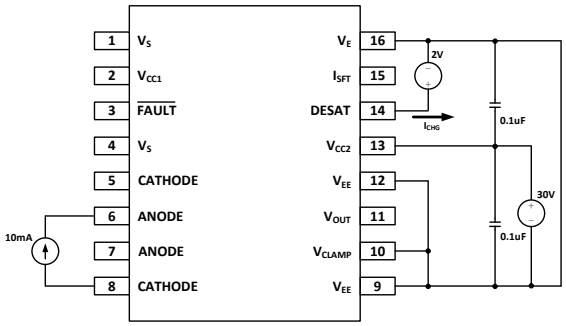


Figure 9. I_{CHG} test circuit

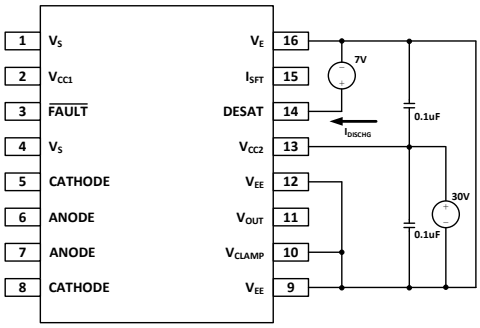


Figure 10. I_{DSCHG} test circuit

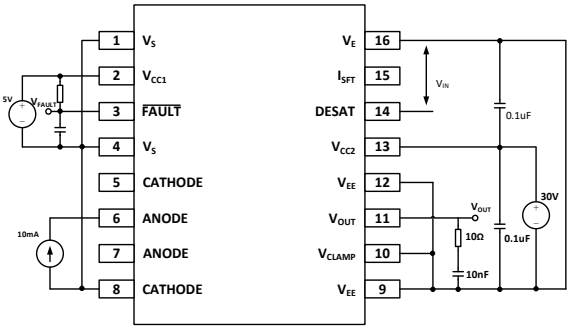


Figure 11. t_{DESAT} fault test circuit

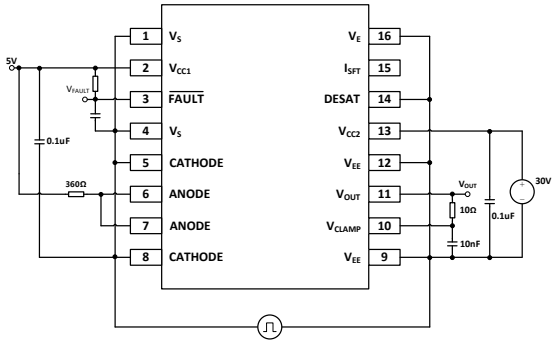


Figure 12. CMTI Test circuit output high

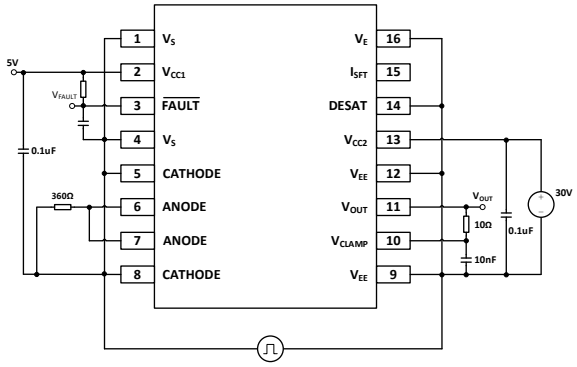


Figure 13. CMTI test circuit output low

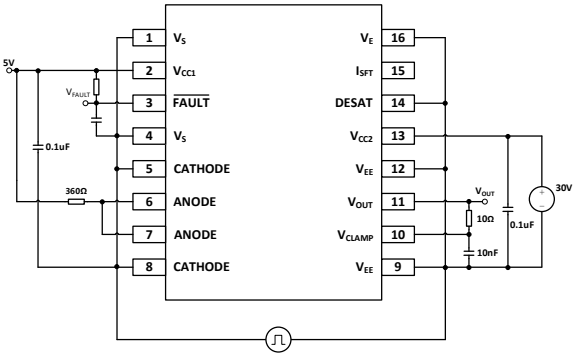


Figure 14. CMTI test circuit fault high

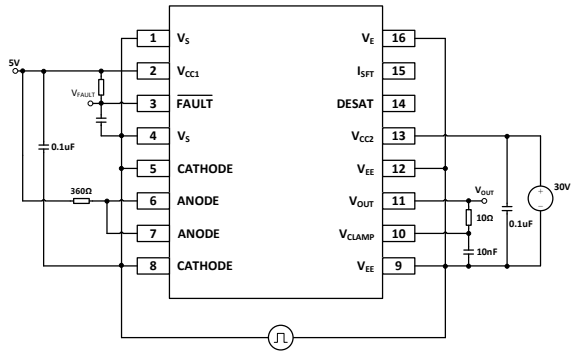


Figure 15. CMTI test circuit fault low

6. Detailed Description

6.1 Overview

The CI-331Jx are highly integrated power control devices. Fault protection, active miller clamp, desaturation detection and soft turn off are the most important features. Active Miller clamp function can prevent fault switching in severe working conditions. CI-331Jx has high current capability that can drive IGBTs with power ratings of up to 15 0A and 1500V. The typical propagation time is 180ns which can minimize the propagation time between the controller and the IGBT. Desaturation detection prevent the damage of power devices during over current, and a second isolation channel provides a fault feedback signal for the controller. UVLO function monitors the power supply voltage to avoid the lower gate voltage of IGBT. This integrated IGBT gate driver is designed to increase the performance and reliability of a motor drive without the cost, size, and complexity of a discrete design. When an IGBT fault is detected, the driver will slowly turn off, reducing the IGBT current to zero slowly to avoid potential IGBT damage from inductive over voltages. At the same time, this fault will be transmitted to the input side.

6.2 Normal Operation

During normal operation, Input current I_F controls the V_{OUT}, when the I_F is high the output is high and the output will be low when I_F is low. The DESAT pin monitor the V_{CE} voltage of IGBT during on stage. The FAULT output is high when no fault condition is detected.

6.3 Fault Condition

When the voltage on the DESAT pin exceeds 6.5V(for CI-331JE/AE) or 9.0V(for CI-331JB/AB) while the IGBT is on, V_{OUT} will slowly turn-off the IGBT and prevent large di/dt induced voltages. the FAULT output low to indicates the fault condition.

6.4 Fault Reset

The output will slowly shut down the power device once detect the fault condition. The input signal will be ignored during the fault period. For CI-331JE/AE, the driver will automatically reset the FAULT pin after a fixed mute time of 26us (Fault Timing diagram Figure 16). For CI-331JB/AB, the driver will reset the FAULT pin after the next rising input signal occurs (Fault Timing diagram Figure 17).

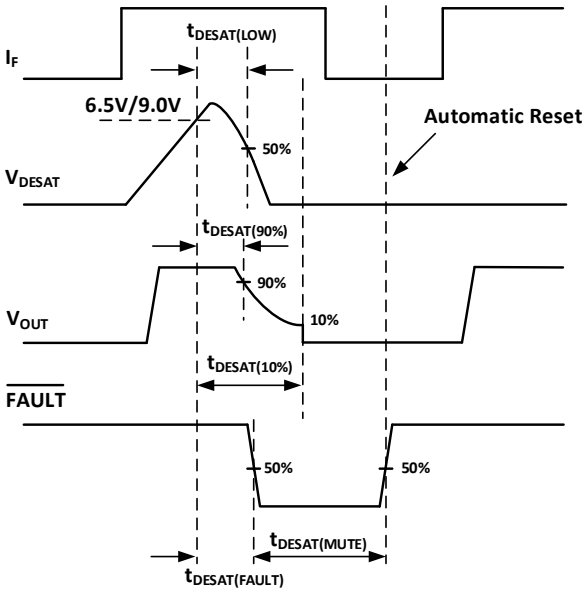


Figure 16. Fault Timing diagram(CI-331JE/AE)

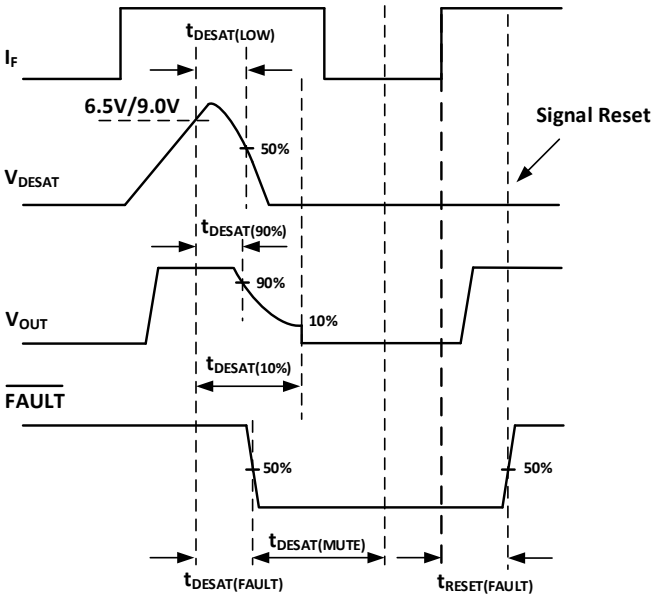


Figure 17. Fault Timing diagram(CI-331JB/AB)

6.5 Desaturation Detection

The internal current source of the DESAT pin is activated only during the driver ON state. During the on state if the current through IGBT is too large the voltage on the DESAT pin will exceed the protection threshold voltage 6.5V(for CI-331JE/AE) or 9.0V(for CI-331JB/BE). By directly measuring the volt age through IGBT, the CI-331Jx limits the power dissipation in the IGBT. Over current or lower gate voltage will cause the voltage on DESAT pin exceed the threshold voltage. V_{OUT} will slowly shut down the IGBT.

6.6 Slow IGBT Gate Discharge

An internal pull-down MOSFET in the CI331Jx output drive stage will 'softly' turn off the IGBT when a desaturation fault is detected. This MOSFET slowly discharges the IGBT gate to prevent fast changes in drain current that could cause overvoltage breakdown. During the soft turn off, the large output pull-down device remains off until the output voltage falls below V_{EE} + 2 Volts, at which time the large pulldown device clamps the IGBT gate to V_{EE}.

6.7 Under Voltage Lockout

The CI-331Jx implements the internal UVLO protection, when the supply voltage is lower than the threshold voltage, the driver output is held as low. The UVLO protection feature not only reduces the power consumption of the driver itself during low power supply voltage condition, but also increases the efficiency of the power stage. At very low gate voltages (below 10 V), the IGBT may operate in the linear region and quickly overheat. The UVLO function causes the output to be clamped whenever insufficient operating supply (V_{CC2}) is applied. Once V_{CC2} exceeds V_{UVLO+} (the positive-going UVLO threshold), the UVLO clamp is released to allow the device output to turn on in response to input signals. With hysteresis and UVLO deglitch filter, the internal UVLO protection block will ignore small noises during the normal switching transients. The table blew shows the relationship between I_F, UVLO, DESAT function, fault and V_{OUT}.

I_F	UVLO on V_{CC2}	DESAT FUNCTION	FAULT OUTPUT	V_{OUT}
ON	< UVLO-	N	High	Low
ON	> UVLO+	Y	Low	Low
ON	> UVLO+	N	High	High
OFF	< UVLO-	N	High	Low
OFF	> UVLO+	N	High	Low

6.8 Active Miller Clamp

Active miller clamp feature is important to prevent the false turn-on while the driver is in OFF state. Miller clamp allows the control of the miller current during a high dv/dt situation and can eliminate the use of a negative supply voltage in most of the applications. During turn-off, the gate voltage is monitored, and the clamp output is activated when gate voltage goes below 2V (relative to V_{EE}).

6.9 Soft Turn-off Current Set

The soft turn-off current can be set through connecting a resistor with I_{SFT} pin. When the pin is left open the current is 140mA(typ).

Resistor Value (kΩ)	Soft turn-off current (mA)
0	140
8.2	70
27	210
75	280
240	420

7. Application and Implementation

7.1 Typical Application Circuit

A set of decoupling capacitors are recommended at the power supplies to stabilize the power supply. 10uF electric capacitor and 0.1uF ceramic capacitor are recommended between V_{CC2} and V_E, V_{EE} and V_E on driver side. A 1uF bypass capacitor is recommended between V_{CC1} and V_S on input side. The decoupling cap should be placed as close as possible to the device.

It is better to add RC filter to eliminate interference. RC filter will introduce longer propagation delay, when selecting the parameter value, the time constant cannot be too large. A 4.7kΩ resistor and 100pF cap can be used as RC filter for $\overline{FAULT}$ pins.

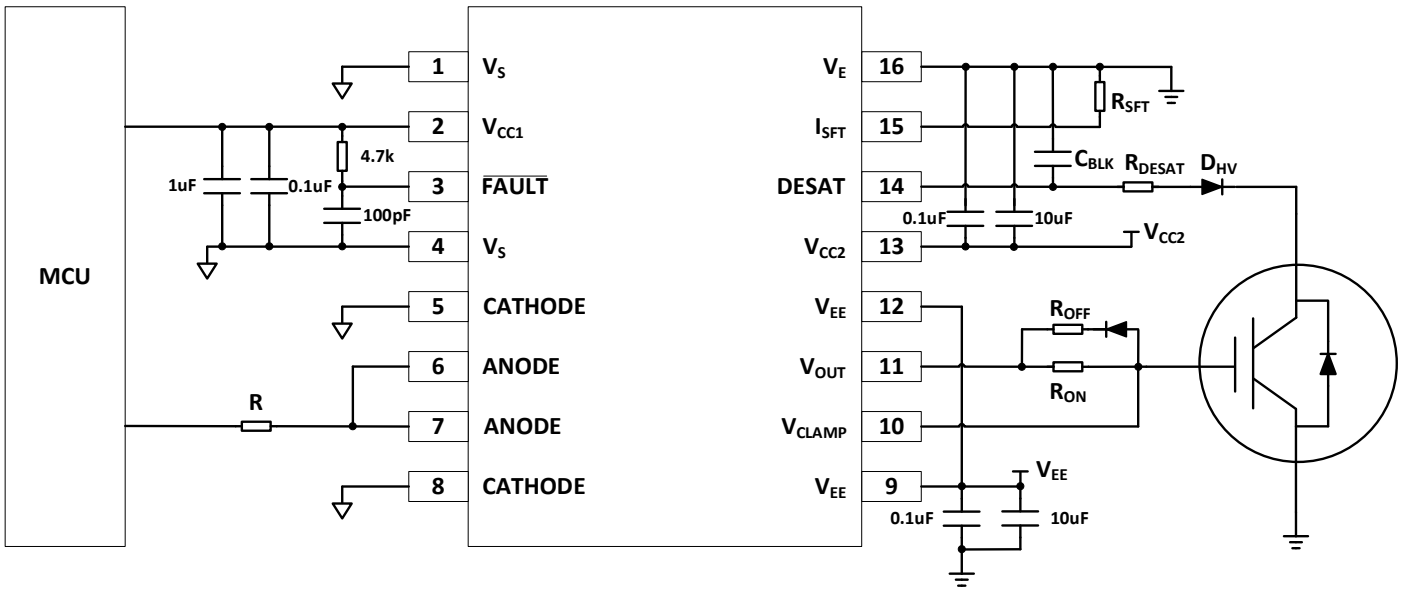


Figure 18. CI-331x typical application schematic

7.2 Design for $\overline{FAULT}$

$\overline{FAULT}$ pin is open-drain output, which means it cannot work without externally pull-up resistor. In this application , a 4.7kΩ pull-up resistor is recommended for $\overline{FAULT}$ pin. A 100pF capacitor can be placed near the device if it is necessary.

7.3 Design for R_{ON} and R_{OFF}

CI-331Jx is featured with split output , so the turn on and off switching speed can be independently controlled. The turn on and turn off resistance determine the peak source and sink current, which can be estimated by the formula:

$$I_{source} = (\frac{V_{CC2} - V_{EE}}{R_{ON} + R_{OH} + R_G}, 6A) \quad (1)$$

$$I_{sink} = (\frac{V_{CC2} - V_{EE}}{R_{OFF} + R_{OL} + R_G}, 6A) \quad (2)$$

Where R_G is the internal resistance of the SiC or IGBT.

7.4 Design for DESAT Protection

DESAT function is important to protect IGBT/SiC MOSFET from overcurrent or short circuit. There is a comparator inside when the voltage on DESAT pin exceed the threshold voltage, The soft turn off circuit will slowly turn off the power device. For typical application, the DESAT diode, DESAT resistor and the blank capacitor are necessary. The DESAT diode function is to conduct forward current and protect the device from high voltage. It is important to choose right diode. To avoid the false detection caused by the reverse recovery spikes, a fast recovery diode with small reverse parasitic capacitance is recommended. DESAT resistor is used to limit the current. A 100Ω resistor is recommended to be added in series with the DESAT diode.

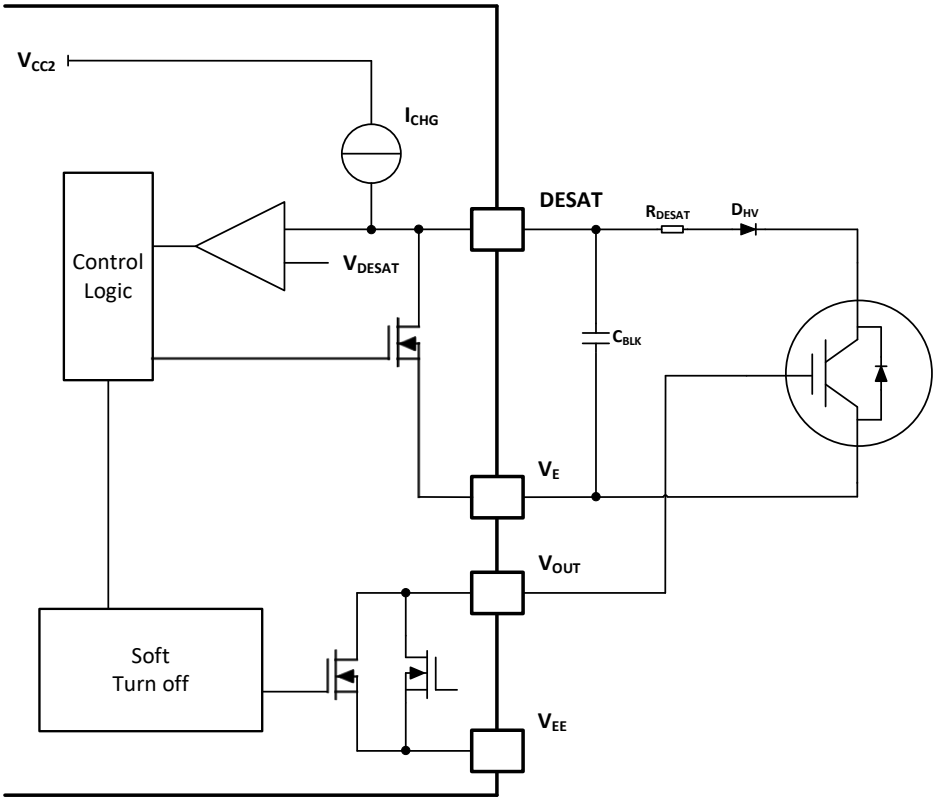


Figure 19. CI-331x DESAT protection

7.5 Design for External Current Buffer

The CI-331Jx device has the strong drive strength. CI-331Jx has 6A source and sink current capability so it can be used to directly drive IGBT/SiC module. If there is a need to increase the IGBT gate drive current totem structure can be used as an external current buffer.

If the over current is detected, the soft turn off circuit is activated. When an external buffer is used, external components must be added to implement soft turn off function. Figure 20 shows the typical circuit, C_{STO} sets the time of soft turn off and R_{STO} limits the inrush current. The minimum R_{STO} and C_{STO} can be estimated by the Equation below.

$$C_{STO} = \frac{I_{STO} * t_{STO}}{VCC2 - VEE} \quad (3)$$

$$R_{STOMIN} = \frac{VCC2 - VEE}{I_{OUTL}} \quad (4)$$

I_{STO} is the internal soft turn off current

t_{STO} is the expected time

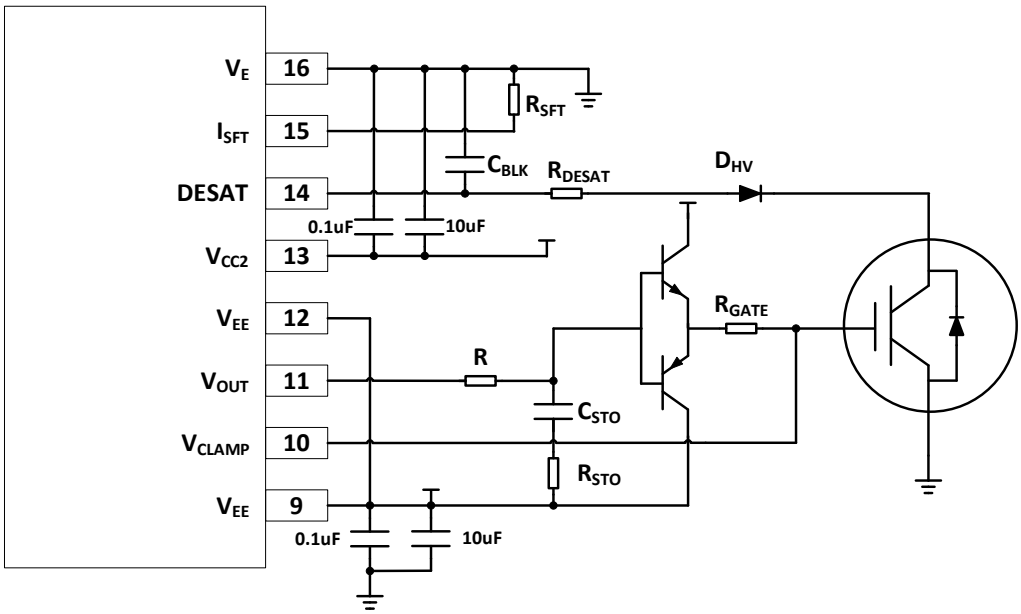


Figure 20. CI-331x external current buffer

8. Layout

The low-ESR ceramic bypass capacitors must be connected between V_{CC1} and V_S, V_{CC2} and V_E, V_{EE} and V_E. The bypass capacitors are placed on the PCB as close to the isolator device as possible. The recommended bypass capacitor value between V_{CC1} and V_S is between 0.1µF and 1µF, bypass capacitor value between V_{CC2} and V_E, V_{EE} and V_E is between 1µF and 10µF. Additional 100nF capacitor in parallel with the isolator device bypass capacitor is recommended for high frequency filtering. To avoid large negative transients on the V_{EE} pins connected to the switch node, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized. Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors. To minimize the impedance of the signal return loop, keep the solid ground plane directly underneath the high-speed signal path, the closer the better. The return path will couple between the nearest ground plane to the signal path. Keep suitable trace width for controlled impedance transmission lines interconnect. Avoid reducing the isolation capability, keep the space underneath the isolator device free from metal such as planes, pads, traces and vias.

9. Outline Dimensions

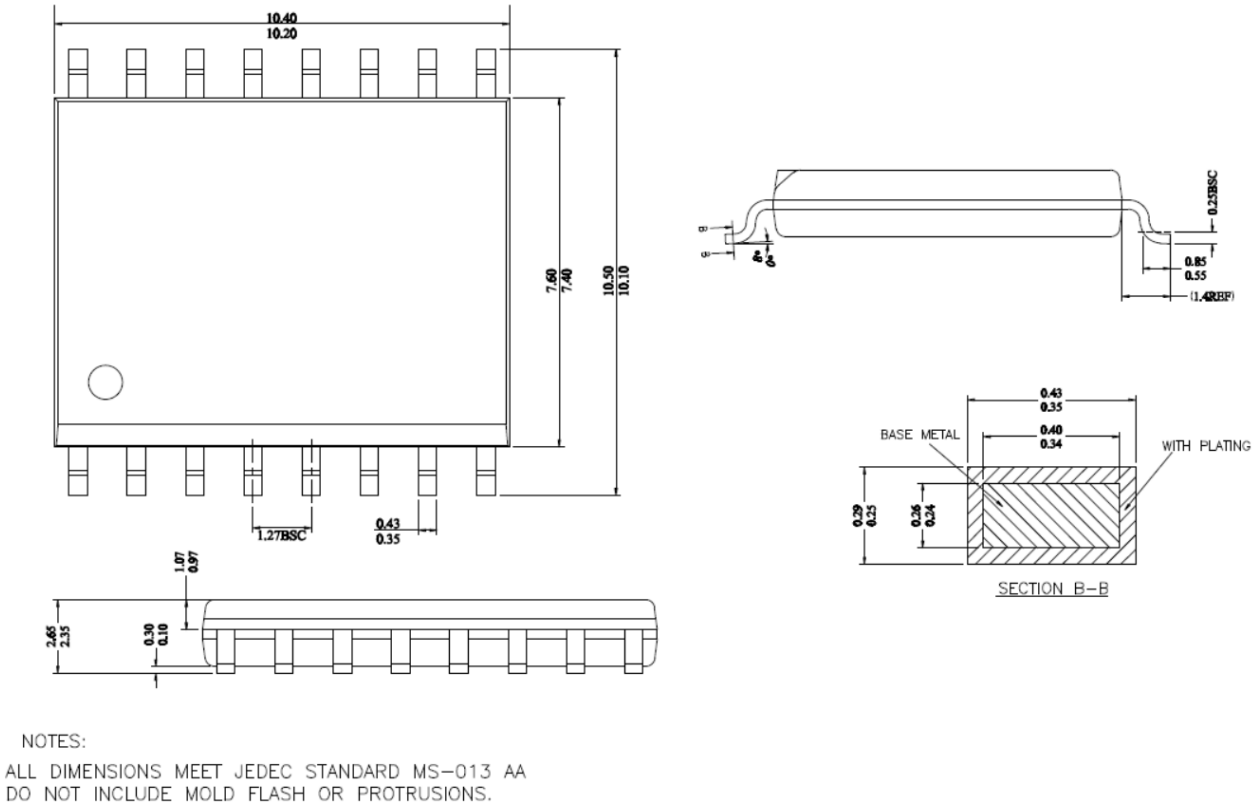


Figure 21. 16-Lead Wide Body Outline Package [16-Lead SOIC_W]

10. Land Patterns

Figure 22 illustrates the recommended land pattern details for the CI-331Jx in a 16 -pin wide-body SOIC package. The table lists the values for the dimensions shown in the illustration.

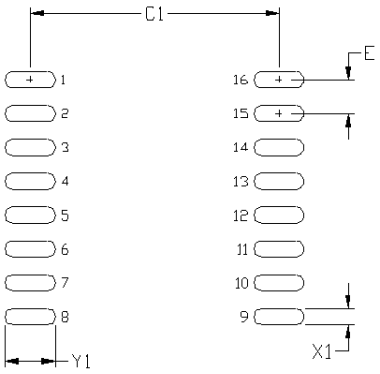


Figure 22. 16-Lead Wide Body SOIC [WB SOIC-16] Land Pattern

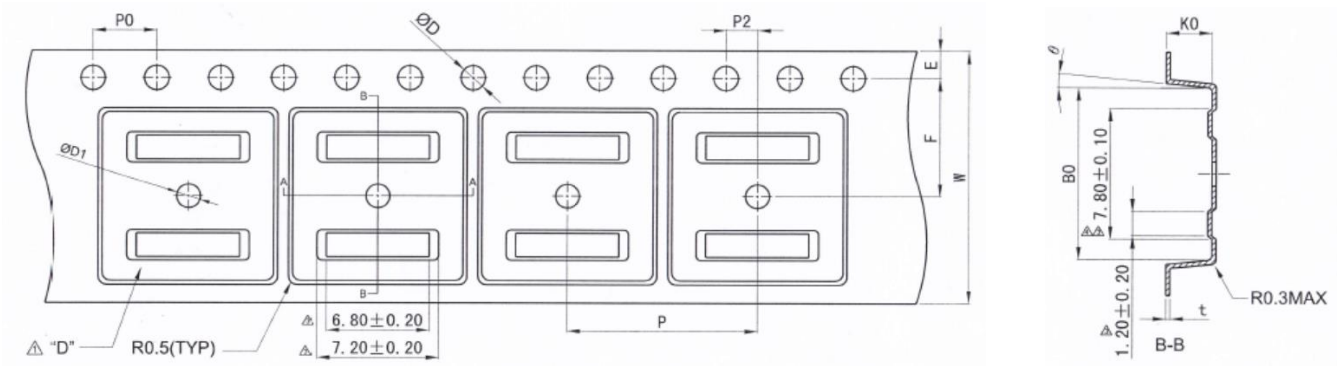
16-Lead Wide Body SOIC [WB SOIC-16] Land Pattern Dimensions

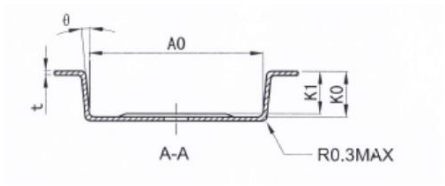
DIMENSION	FEATURE	PARAMETER	UNIT
C1	Pad column spacing	9.40	mm
E	Pad row pitch	1.27	mm
X1	Pad width	0.60	mm
Y1	Pad length	1.90	mm

(1) This land pattern design is based on IPC -7351

(2) All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

11. Reel Information





Items	Size(mm)
E	1.75±0.10
F	7.50±0.05
P2	2.00±0.05
D	1.55±0.05
D1	1.5±0.10
P0	4.00±0.10
10P0	40.00±0.20

Items	Size(mm)
W	16.00±0.30
P	12.00±0.10
A0	10.90±0.10
B0	10.80±0.10
K0	3.00±0.10
t	0.30±0.05
K1	2.70±0.10
θ	5° TYP

Figure 23. 16-Lead Wide Body Outline Package

13. Ordering Guide

MODEL NAME	TEMPERATURE RANGE	V_{DESAT}	RESET	WITHSTAND VOLTAGE RATING(V_{RMS})	PACKAGE DESCRIPTION	MSL PEAK TEMP(1)	QUANTITY PER REEL
CI-311J-500E	−40~125°C	6.5V	Automatic	5700	WB SOIC-16	Level-2-260C-1 YEAR	1500
CI-311J-500B	−40~125°C	9.0V	Automatic	5700	WB SOIC-16	Level-2-260C-1 YEAR	1500
CI-311J-500EA	−40~125°C	6.5V	Signal reset	5700	WB SOIC-16	Level-2-260C-1 YEAR	1500
CI-311J-500BA	−40~125°C	9.0V	Signal reset	5700	WB SOIC-16	Level-2-260C-1 YEAR	1500

(1) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.