

## Features

- Provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768 kHz quartz crystal
- Century flag
- Clock operating voltage: 1.0 V to 5.5 V at room temperature
- Low backup current; typical 0.25  $\mu$ A at  $V_{DD} = 3.0$  V and  $T_{amb} = 25$  °C
- 400 kHz two-wire I<sup>2</sup>C-bus interface (at  $V_{DD} = 1.8$  V to 5.5 V)
- Programmable clock output for peripheral devices (32.768 kHz, 1.024 kHz, 32 Hz, and 1 Hz)
- Alarm and timer functions
- Integrated oscillator capacitor
- Internal Power-On Reset (POR)
- I<sup>2</sup>C-bus slave address: read A3h and write A2h
- Open-drain interrupt pin

## Description

The PCF8563 is a CMOS Real-Time Clock (RTC) and calendar optimized for low power consumption. A programmable clock output, interrupt output, and voltage-low detector are also provided. All addresses and data are transferred serially via a two-line bidirectional I<sup>2</sup>C-bus. Maximum bus speed is 400 kbit/s. The register address is incremented automatically after each written or read day table.

## Applications

- Mobile telephones
- Portable instruments
- Electronic metering
- Battery powered products

## Block Diagram

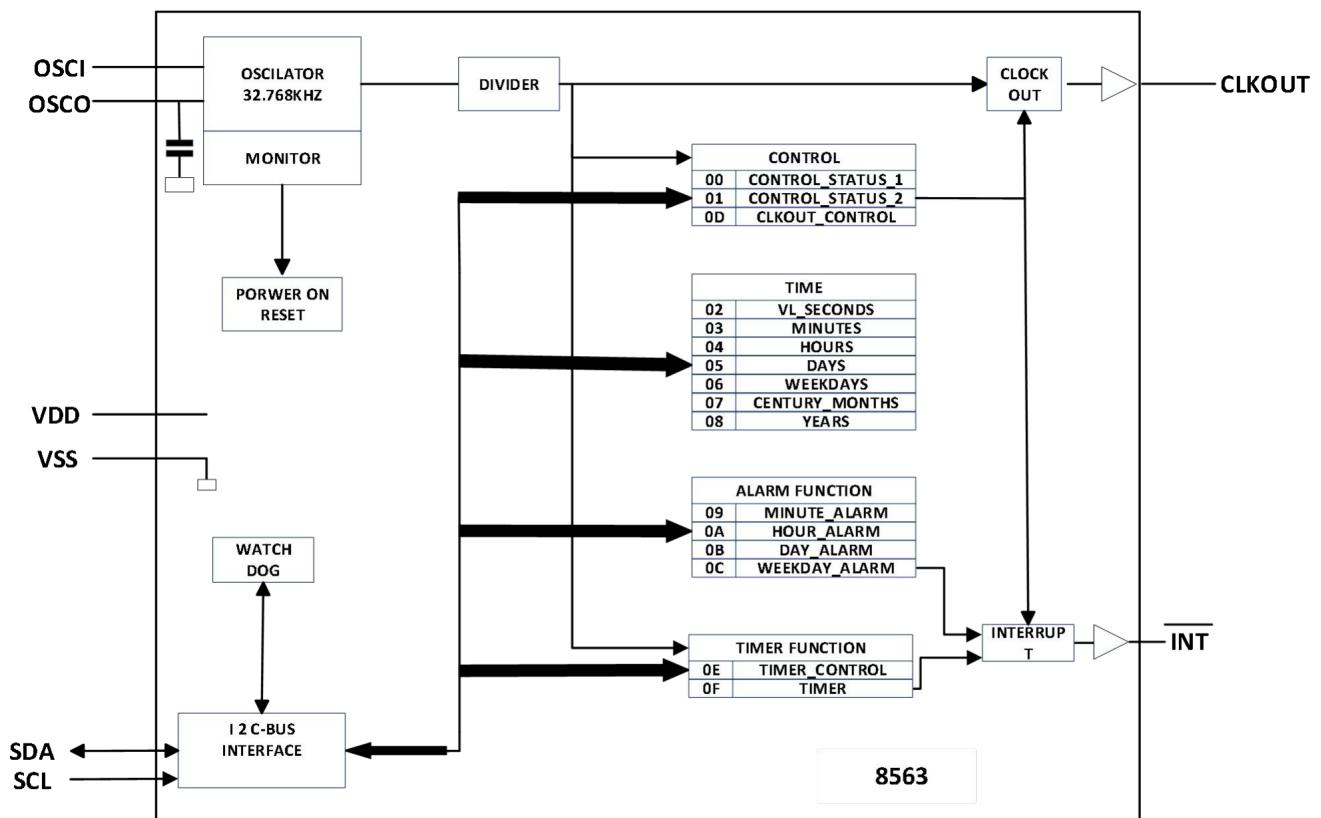


Figure 1. Block diagram of PCF8563

## Pinning Information

### 5.1 Pinning



Figure 2. Pin configuration for PCF8563

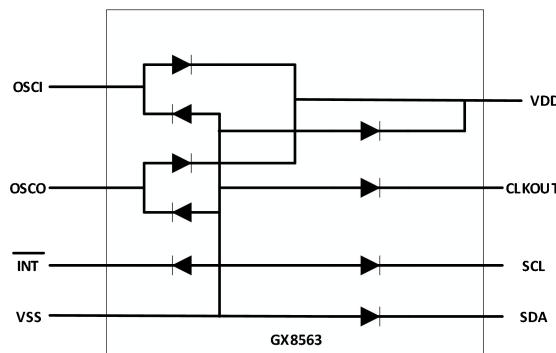
## Pin Description

Table 1. Pin description

SYMBOL	PIN		DESCRIPTION
	MSOP8	SOP8	
OSCI	1	1	oscillator input
OSCO	2	2	oscillator output
INT	3	3	interrupt output (open-drain; active LOW)
V <sub>ss</sub>	4	4	ground
SDA	5	5	serial data input and output
SCL	6	6	serial clock input
CLKOUT	7	7	clock output, open-drain
V <sub>DD</sub>	8	8	supply voltage
n.c.	-		not connected; do not connect and do not use as feed

[1] The die paddle (exposed pad) is wired to V<sub>ss</sub> but should not be electrically connected.

## Internal Circuitry



**Figure 20. Device diode protection diagram**

## Limiting Values

**Table 26. Limiting values**

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V <sub>DD</sub>	supply voltage		-0.5	+6.5	V
I <sub>DD</sub>	supply current		+50	+50	mA
V <sub>I</sub>	input voltage	on pins SCL, SDA, and OSCI	-0.5	+6.5	V
V <sub>O</sub>	output voltage	on pins CLKOUT and INT	-0.5	+6.5	V
I <sub>I</sub>	input current	at any input	-10	+10	mA
I <sub>O</sub>	output current	at any output	-10	+10	mA
P <sub>tot</sub>	total power dissipation		-	300	mW
V <sub>ESD</sub>	electrostatic discharge voltage	HBM			
		MSOP8	-	±2000	V
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>amb</sub>	ambient temperature	operating device	-40	+85	°C

## Static Characteristics

**Table 27. Static characteristics**

$V_{DD} = 1.0 \text{ V to } 5.5 \text{ V}$ ;  $V_{SS} = 0 \text{ V}$ ;  $T_{amb} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ;  $f_{osc} = 32.768 \text{ kHz}$ ; quartz  $R_s = 40 \text{ k}\Omega$ ;  $C_L = 8 \text{ pF}$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
<b>Supplies</b>						
$V_{DD}$	supply voltage	interface inactive; $f_{SCL} = 0 \text{ Hz}$ ; $T_{amb} = 25^\circ\text{C}$ <sup>[1]</sup>	1.0	-	5.5	V
		interface active; $f_{SCL} = 400 \text{ kHz}$ <sup>[1]</sup>	1.8	-	5.5	V
		clock data integrity; $T_{amb} = 25^\circ\text{C}$	$V_{low}$	-	5.5	V
$I_{DD}$	supply current	interface active				
		$f_{SCL} = 400 \text{ kHz}$	-	-	800	$\mu\text{A}$
		$f_{SCL} = 100 \text{ kHz}$	-	-	200	$\mu\text{A}$
		interface inactive ( $f_{SCL}=0\text{Hz}$ ); CLKOUT disabled; $T_{amb} = 25^\circ\text{C}$ <sup>[2]</sup>				
		$V_{DD} = 5.0 \text{ V}$	-	400	600	nA
		$V_{DD} = 3.0 \text{ V}$	-	250	500	nA
		interface inactive ( $f_{SCL}=0 \text{ Hz}$ ); CLKOUT disabled; $T_{amb} = -40^\circ\text{C}$ to $+85^\circ\text{C}$ <sup>[2]</sup>				
		$V_{DD} = 5.0 \text{ V}$	-	500	700	nA
		$V_{DD} = 3.0 \text{ V}$	-	400	600	nA
<b>Inputs</b>						
$V_{IL}$	LOW-level input voltage		$V_{SS}$	-	$0.3V_{DD}$	V
$V_{IH}$	HIGH-level input voltage		$0.7V_{DD}$	-	$V_{DD}$	V
$I_{LI}$	input leakage current	$V_I = V_{DD} \text{ or } V_{SS}$	-1	0	+1	$\mu\text{A}$
$C_i$	input capacitance		-	-	7	pF
<b>Outputs</b>						
$I_{OL}$	LOW-level output current	output sink current; $V_{OL} = 0.4 \text{ V}$ ; $V_{DD} = 5 \text{ V}$				
		on pin SDA	3	-	-	mA
		on pin INT	1	-	-	mA
		on pin CLKOUT	1	-	-	mA
$I_{LO}$	output leakage current	$V_O = V_{DD} \text{ or } V_{SS}$	-1	0	+1	$\mu\text{A}$
<b>Voltage detector</b>						
$V_{low}$	low voltage	$T_{amb} = 25^\circ\text{C}$ ; sets bit VL;	-	0.9	1.0	V

[1] For reliable oscillator start-up at power-up:  $V_{DD(\min)\text{power-up}} = V_{DD(\min)} + 0.3 \text{ V}$ .

[2] Timer source clock = 1/60 Hz, level of pins SCL and SDA is  $V_{DD}$  or  $V_{SS}$ .

## Dynamic Characteristics

**Table 28. Dynamic characteristics**

$V_{DD} = 1.0 \text{ V to } 5.5 \text{ V}$ ;  $V_{SS} = 0 \text{ V}$ ;  $T_{amb} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ;  $f_{osc} = 32.768 \text{ kHz}$ ; quartz  $R_s = 40 \text{ k}\Omega$ ;  $C_L = 8 \text{ pF}$ ; unless otherwise specified.

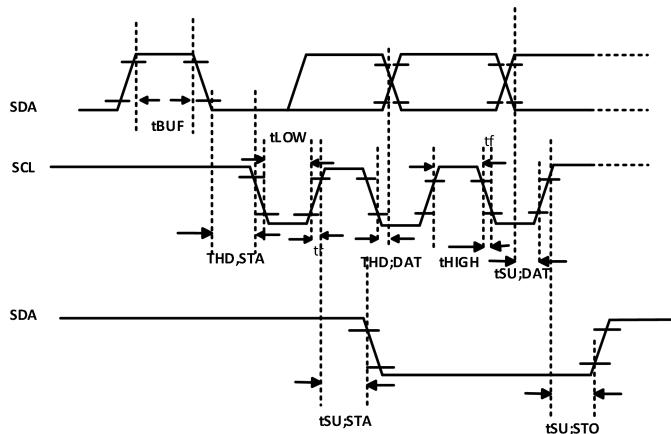
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
<b>Oscillator</b>						
$C_{osco}$	capacitance on pin OSCO		15	25	35	pF
$\Delta f_{osc}/f_{osc}$		$\Delta V_{DD} = 200 \text{ mV}$ ; $T_{amb} = 25^\circ\text{C}$	-	0.2	-	ppm
<b>Quartz crystal parameters (<math>f = 32.768 \text{ kHz}</math>)</b>						
$R_s$	series resistance		-	-	100	
$C_L$	load capacitance	parallel	7 <sup>[1]</sup>	-	12.5	
$C_{trim}$	trimmer capacitance	external; on pin OSC1	5	-	25	
<b>CLKOUT output</b>						
$\delta_{CLKOUT}$	duty cycle on pin CLKOUT		-	50	-	%
<b>I<sup>2</sup>C-bus timing characteristics</b>						
$f_{SCL}$	SCL clock frequency		-	-	400	kHz
$t_{HD:STA}$	hold time (repeated) START condition		0.6	-	-	$\mu\text{s}$
$t_{SU:STA}$	set-up time for a repeated START condition		0.6	-	-	$\mu\text{s}$
$t_{LOW}$	LOW period of the SCL clock		1.3	-	-	$\mu\text{s}$
$t_{HIGH}$	HIGH period of the SCL clock		0.6	-	-	$\mu\text{s}$
$t_r$	rise time of both SDA and SCL signals					
		standard-mode	-	-	1	$\mu\text{s}$
		fast-mode	-	-	0.3	$\mu\text{s}$
$t_f$	fall time of both SDA and SCL signals		-	-	0.3	$\mu\text{s}$
$t_{BUF}$	bus free time between a STOP and START condition		1.3	-	-	$\mu\text{s}$
$C_b$	capacitive load for each bus line		-	-	400	pF
$t_{SU:DAT}$	data set-up time		100	-	-	ns
$t_{HD:DAT}$	data hold time		0	-	-	ns
$t_{SU:STO}$	set-up time for STOP condition		0.6	-	-	$\mu\text{s}$
$t_w(\text{spike})$	spike pulse width	on bus	-	-	50	ns

[1]  $C_L$  is a calculation of  $C_{trim}$  and  $C_{osco}$  in series:  $C_L = \frac{C_{trim} \cdot C_{osco}}{C_{trim} + C_{osco}}$

[2] Unspecified for  $f_{CLKOUT} = 32.768$  kHz.

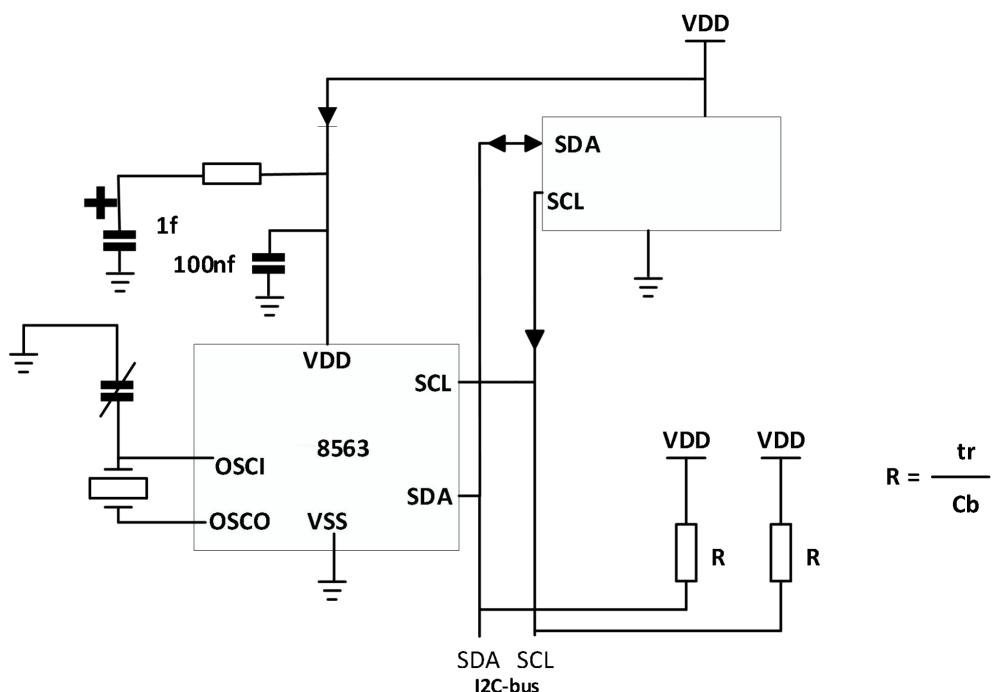
[3] All timing values are valid within the operating supply voltage at ambient temperature and referenced to  $V_{IL}$  and  $V_{IH}$  with an input voltage swing of  $V_{SS}$  to  $V_{DD}$ .

[4] I<sup>2</sup>C-bus access time between two STARTs or between a START and a STOP condition to this device must be less than one second.



**Figure 21. I<sup>2</sup>C-bus timing waveforms**

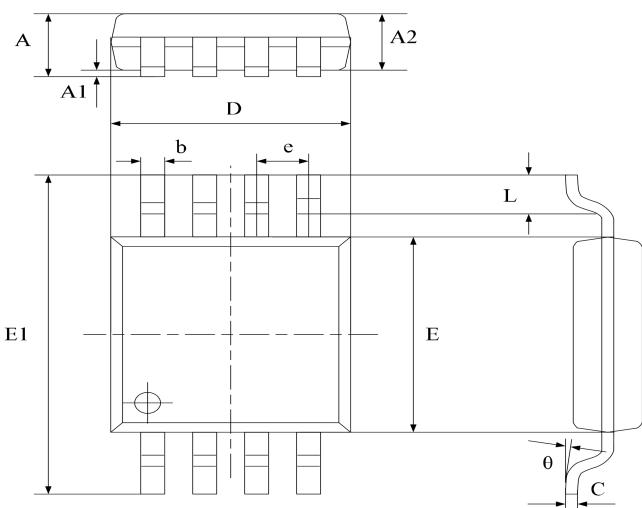
## 12 situation of application



**Figure 22. Application diagram**

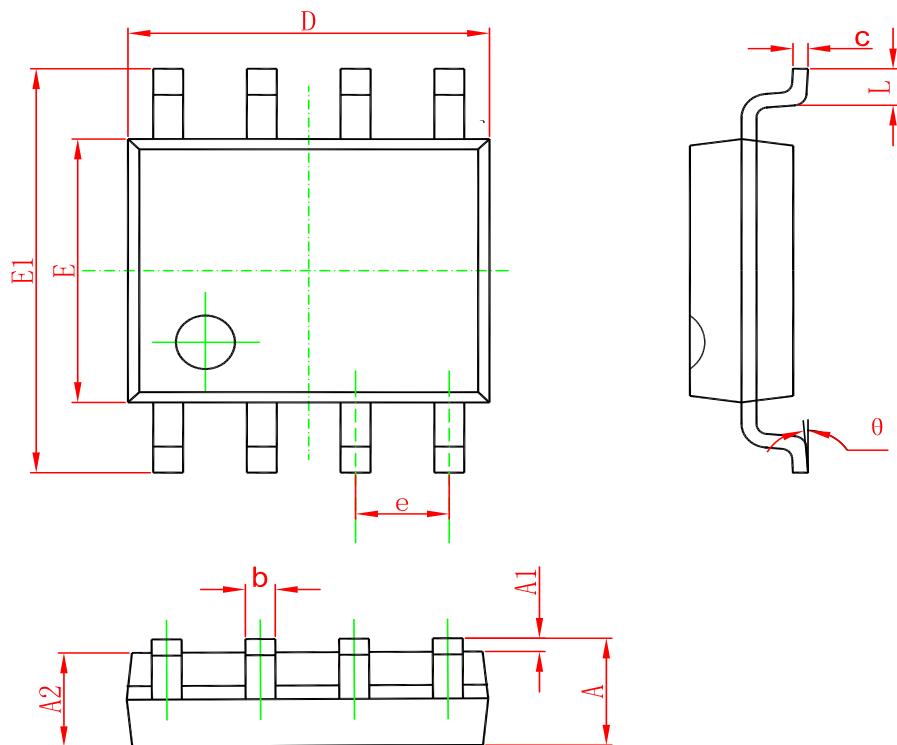
## Package Outline

**MSOP-8**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.033	0.045
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.031	0.039
b	0.290	0.380	0.012	0.016
C	0.150	0.200	0.006	0.008
D	2.900	3.100	0.118	0.127
E	2.900	3.100	0.118	0.127
E1	4.700	5.100	0.192	0.208
e	0.650typ.		0.026typ.	
L	0.400	0.700	0.016	0.029
θ	0°	8°	0°	8°

## SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

## Ordering information

Order code	Package	Baseqty	Deliverymode	Marking
UMW PCF8563T	SOP-8	3000	Tape and reel	PCF8563
UMW PCF8563TS	MSOP-8	3000	Tape and reel	P8563