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XINBOLE

Product Specification

XBLW DS1302

Trickle-Charge Timekeeping Chip

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RoHS

Descriptions

The DS1302 trickle-charge timekeeping chip contains a real-time clock/calendar and 31bytes of static RAM. It communicates with a microprocessor via a simple serial interface.The real-time clock/calendar provides seconds, minutes, hours, day, date, month, and year information.The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator.

Interfacing the DS1302 with a microprocessor is simplified by using synchronous serial communication. Only three wires are required to communicate with the clock/RAM: CE,I/O (data line), and SCLK (serial clock). Data can be transferred to and from the clock/RAM 1 byte at a time or in a burst of up to 31 bytes. The DS1302 is designed to operate on very low power and retain data and clock information on less than 10μW.

Feature

- Real-Time Clock Counts Seconds, Minutes, Hours, Date of the Month, Month, Day of the Week, and Year with Leap-Year Compensation Valid Up to 2100
- 31 x 8 Battery-Backed General-Purpose RAM
- Serial I/O for Minimum Pin Count
- 2.0V to 5.5V Full Operation
- Uses Less than 1uA at 2.0V
- Single-Byte or Multiple-Byte (Burst Mode) Data Transfer for Read or Write of Clock or RAM Data
- Simple 3-Wire Interface
- TTL-Compatible (VCC = 5V)
- Optional Industrial Temperature Range: -40°C to +85°C
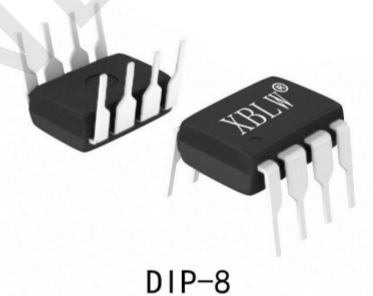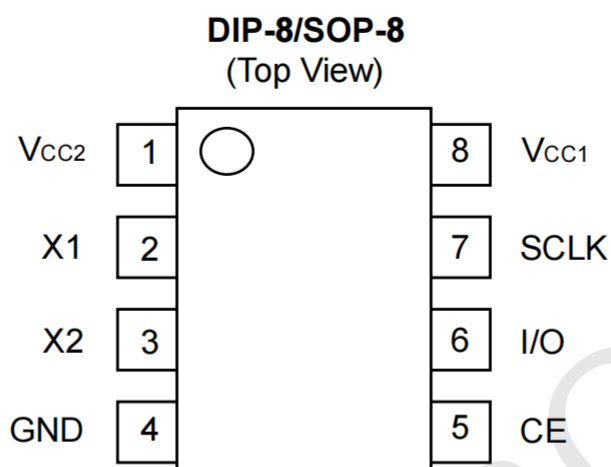
DIP-8

SOP-8

Applications

- Multi-tariff electricity meter
- IC card water meter
- IC card gas meter
- Fax machine
- Portable instrument
- Mobile phone, Perpetual clock

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW DS1302N	DIP-8	DS1302N	Tube	1000Pcs /Box
XBLW DS1302DTR	SOP-8	DS1302	Tape	2500Pcs /Reel

Pin Configurations

DIP-8/SOP-8
(Top View)

V_{CC2}	1	8	V_{CC1}
X1	2	7	SCLK
X2	3	6	I/O
GND	4	5	CE

Pin Description

| NO.	NAME	FUNCTION
1	V_{CC2}	Primary Power-Supply Pin in Dual Supply Configuration. V_{CC1} is connected to a backup source to maintain the time and date in the absence of primary power. The DS1302operates from the larger of V_{CC1} or V_{CC2}. When V_{CC2} is greater than V_{CC1} + 0.2V, V_{CC2} powers the DS1302. When V_{CC2} is less than V_{CC1}, V_{CC1} powers the DS1302.
2	X1	Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator is designed for operation with a crystal having a specified load capacitance of 6pF. The DS1302 can also be driven by an external 32.768kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.
3	X2	
4	GND	Ground
5	CE	Input. CE signal must be asserted high during a read or a write. This pin has an internal 40kΩ (typ) pulldown resistor to ground. Note: Previous data sheet revisions referred to CE as RST. The functionality of the pin has not changed.
6	I/O	Input/Push-Pull Output. The I/O pin is the bidirectional data pin for the 3-wire interface. This pin has an internal 40kΩ (typ) pulldown resistor to ground.
7	SCLK	Input. SCLK is used to synchronize data movement on the serial interface. This pin has an internal 40kΩ (typ) pulldown resistor to ground.
8	V_{CC1}	Low-Power Operation in Single Supply and Battery-Operated Systems and Low-Power Battery Backup. In systems using the trickle charger, the rechargeable energy source is connected to this pin. UL recognized to ensure against reverse charging current when used with a lithium battery.

Typical Operating Circuit
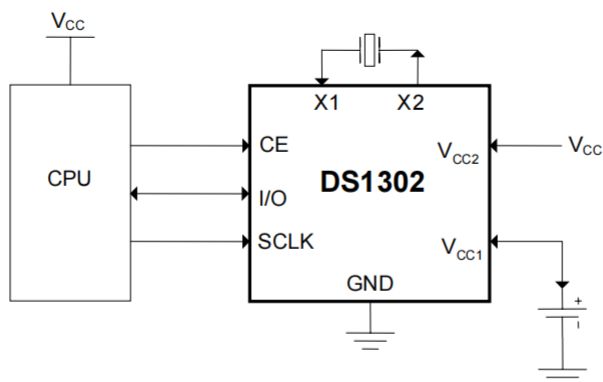
Block Diagram
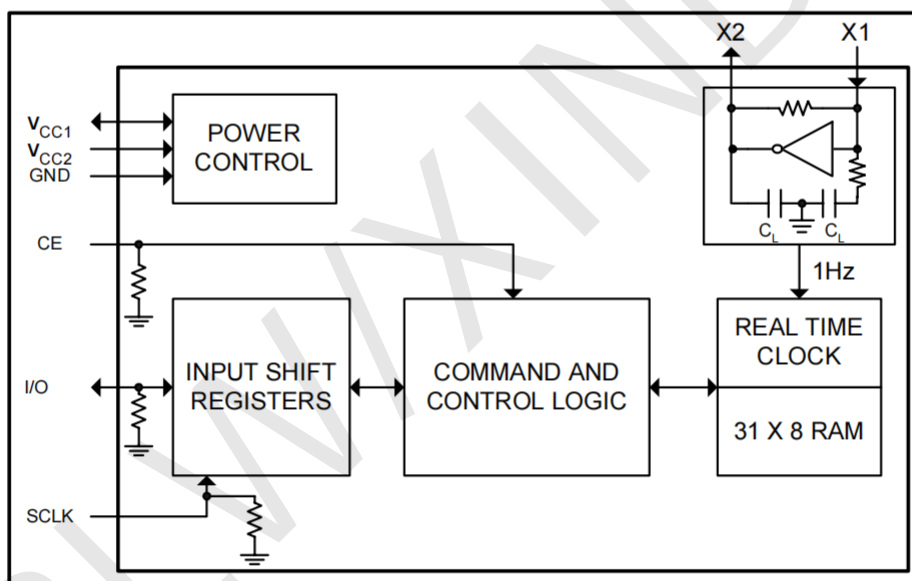
Figure 1. Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage Rangeon Any Pin Relative to Ground	V_{CC1}, V_{CC2}	-0.5 ~ +7.0	V
Operating Temperature Range	Toper	-40 ~ +85	°C
Storage Temperature Range	T_S	-55 ~ 125	°C
SolderingTemperature(leads,10seconds)	T_H	260	°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Dc Operating Conditions

(TA=0℃ to +70℃ or TA=-40℃ to +85℃.)(Note 1)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Supply Voltage V_{CC1},V_{CC2}	V_{CC1} V_{CC2}	(Notes 2,10)	2.0	3.3	5.5	V
Logic 1 Input	V_{IH}	(Note 2)	2.0		Vcc+0.3	V
Logic 0 Input	V_{IL}	Vcc=2.0V	-0.3		+0.3	V
		Vcc=5.0V	-0.3		+0.8	

Electrical Characteristics

DC Characteristics

(TA = 0°C to +70°C or TA = -40°C to +85°C.) (Note 1)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input Leakage	I_{LI}	(Notes 5, 13)			85	500	μA
I/O Leakage	I_{LO}	(Notes 5, 13)			85	500	μA
Logic 1 Output (I_{OH} = -0.4mA)	V_{OH}	Vcc = 2.0V	(Note 2)	1.6			V
Logic 1 Output (I_{OH} = -1.0mA)		Vcc = 5.0V		2.4			
Logic 0 Output (I_{OL} = 1.5mA)	V_{OL}	Vcc = 2.0V	(Note 2)			0.4	V
Logic 0 Output (I_{OL} = 4.0mA)		Vcc = 5.0V				0.4	
Active Supply Curren (Oscillator Enabled)	I_{CC1A}	V_{CC1} = 2.0V	CH = 0			0.6	mA
		V_{CC1} = 5.0V	(Notes 4, 11)			1.28	
Timekeeping Current (Oscillator Enabled)	I_{CC1T}	V_{CC1} = 2.0V	CH = 0		0.5	2	μA
		V_{CC1} = 5.0V	(Notes 3, 11,13)		1	5	
Active Supply Current (Oscillator Enabled)	I_{CC2A}	V_{CC2} = 2.0V	CH = 0			0.6	mA
		V_{CC2} = 5.0V	(Notes 4, 12)			1.28	
Timekeeping Current (Oscillator Enabled)	I_{CC2T}	V_{CC2} = 2.0V	CH = 0			100	μA
		V_{CC2} = 5.0V	(Notes 3, 12)			140	
Trickle-Charge Resistors	R1				2		kΩ
	R2				4		
	R3				8		
Trickle-Charge Diode Voltage Drop	V_{TD}				0.7		V

Capacitance

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Input Capacitance	CI		10		pF
I/O Capacitance	CI/ O		15		pF

AC Characteristics

(TA = 0°C to +70°C or TA = -40°C to +85°C.) (Note 1)

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
Data to CLK Setup	t_{DC}	Vcc = 2.0V	(Note 6)	200			ns
		Vcc = 5V		50			
CLK to Data Hold	t_{CDH}	Vcc = 2.0V	(Note 6)	280			ns
		Vcc = 5V		70			
CLK to Data Delay	t_{CDD}	Vcc = 2.0V	(Notes 6, 7, 8)			800	ns
		Vcc = 5V				200	
CLK Low Time	t_{CL}	Vcc = 2.0V	(Note 6)	1000			ns
		Vcc = 5V		250			
CLK High Time	t_{CH}	Vcc = 2.0V	(Note 6)	1000			ns
		Vcc = 5V		250			
CLK Frequency	t_{CLK}	Vcc = 2.0V	(Note 6)			0.5	MHz
		Vcc = 5V		DC		2.0	
CLK Rise and Fall	t_R, t_F	Vcc = 2.0V				2000	ns
		Vcc = 5V				500	
CE to CLK Setup	t_{CC}	Vcc = 2.0V	(Note 6)	4			μs
		Vcc = 5V		1			
CLK to CE Hold	t_{CCH}	Vcc = 2.0V	(Note 6)	240			ns
		Vcc = 5V		60			
CE Inactive Time	t_{CWH}	Vcc = 2.0V	(Note 6)	4			μs
		Vcc = 5V		1			
CE to I/O High Impedance	t_{CDZ}	Vcc = 2.0V	(Note 6)			280	ns
		Vcc = 5V				70	
SCLK to I/O High Impedance	t_{CCZ}	Vcc = 2.0V	(Note 6)			280	ns
		Vcc = 5V				70	

Note 1 : Limits at -40°C are guaranteed by design and are not production tested.

Note 2 : All voltages are referenced to ground.

Note 3 : Icc1T and Icc2T are specified with I/O open, CE and SCLK set to a logic 0.

Note 4 : Icc1A and Icc2A are specified with the I/O pin open, CE high, SCLK = 2MHz at Vcc = 5V; SCLK = 500kHz, Vcc = 2.0V.

Note 5 : CE, SCLK, and I/O all have 40kΩ pulldown resistors to ground.

Note 6 : Measured at VIH = 2.0V or VIL = 0.8V and 10ns maximum rise and fall time.

Note 7 : Measured at VOH = 2.4V or VOL = 0.4V.

Note 8 : Load capacitance = 50pF.

Note 9 : Icc1S and Icc2S are specified with CE, I/O, and SCLK open.

Note 10 : Vcc = Vcc2, when Vcc2 > Vcc1 + 0.2V; Vcc = Vcc1, when Vcc1 > Vcc2.

Note 11 : Vcc2 = 0V.

Note 12 : Vcc1 = 0V.

Note 13 : Typical values are at +25°C.

Oscillator Circuit

The DS1302 uses an external 32.768kHz crystal.The oscillator circuit does not require any external resistors or capacitors to operate.Table 1 specifies several crystal parameters for the external crystal.Figure 1 shows a functional schematic of the oscillator circuit.If using a crystal with the specified characteristics,the startup time is usually less than one second.

Table 1.Crystal Specifications

Parameter	Symbol	Min.	Typ.	Max.	Units
Nominal Frequency	f0		32.768		KHz
Series Resistance	ESR			45	KΩ
Load Capacitance	CL		6		pF

Clock Accuracy

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed.In order to improve the accuracy of high running, a set of 0pF-33pF negative load compensation capacitors should be placed outside the crystal end. The specific capacity is determined by the application layout and crystal vibration. Additional will be added by crystal frequency drift caused by temperature shifts.External circuit noise coupled into the oscillator circuit may result in the clock running fast.Figure 2 shows a typical PC board layout for isolating the crystal and oscillator from noise.
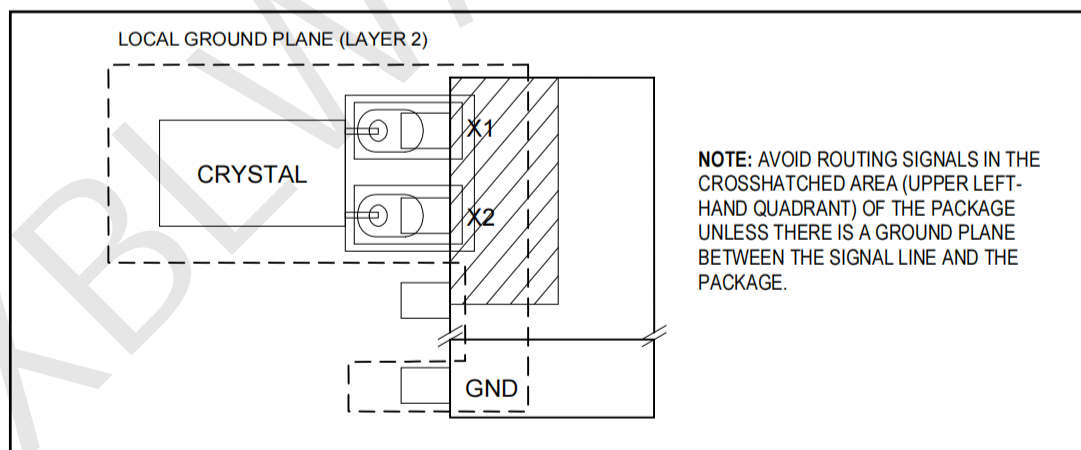

Figure 2. Typical PC Board Layout for Crystal

Command Byte

Figure 3 shows the command byte.A command byte initiates each data transfer.The MSB (bit 7)must be a logic 1.If it is 0, writes to the DS1302 will be disabled.Bit 6 specifies clock/calendar data if logic 0 or RAM data if logic 1. Bits 1 to 5 specify the designated registers to be input or output,and the LSB (bit 0)specifies a write operation (input)if logic 0 or read operation (output)if logic 1.The command byte is always input starting with the LSB (bit0).
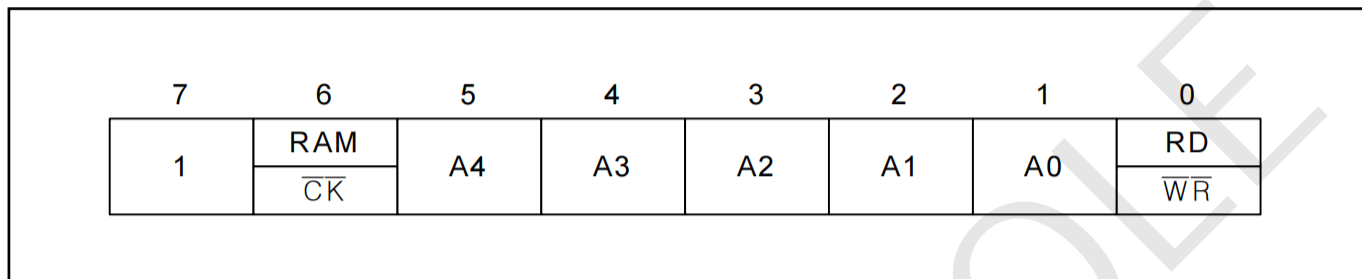
7	6	5	4	3	2	1	0
1	RAM $\overline{CK}$	A4	A3	A2	A1	A0	RD $\overline{WR}$

Figure 3. Address/Command Byte

Ce And Clock Control

Driving the CE input high initiates all data transfers.The CE input serves two functions.First,CE turns on the control logic that allows access to the shift register for the address/command sequence.Second,the CE signal provides a method of terminating either single-byte or multiple-byte CE data transfer.

A clock cycle is a sequence of a rising edge followed by a falling edge.For data inputs,data must be valid during the rising edge of the clock and data bits are output on the falling edge of clock.If the CE input is low,all data transfer terminates and the I/O pin goes to a high-impedance state.Figure 4 shows data transfer.At power-up,CE must be a logic 0 until Vcc>2.0V.Also,SCLK must be at a logic 0 when CE is driven to a logic 1 state.

Data Input

Following the eight SCLK cycles that input a write command byte,a data byte is input on the rising edge of the next eight SCLK cycles.Additional SCLK cycles are ignored should they inadvertently occur.Data is input starting with bit 0.

Data Output

Following the eight SCLK cycles that input a read command byte,a data byte is output on the falling edge of the next eight SCLK cycles.Note that the first data bit to be transmitted occurs on the first falling edge after the last bit of the command byte is written.Additional SCLK cycles retransmit the data bytes should they inadvertently occur so long as CE remains high.This operation permits continuous burst mode read capability.Also,the I/O pin is tri-stated upon each rising edge of SCLK.Data is output starting with bit 0.

Burst Mode

Burst mode can be specified for either the clock/calendar or the RAM registers by addressing location 31 decimal (address/command bits 1 through 5=logic 1).As before,bit 6 specifies clock or RAM and bit 0 specifies read or write.There is no data storage capacity at locations 9 through 31 in the Clock/Calendar Registers or location 31 in the RAM registers.Reads or writes in burst mode start with bit 0 of address 0.

When writing to the clock registers in the burst mode,the first eight registers must be written in order for the data to be transferred.However,when writing to RAM in burst mode it is not necessary to write all 31 bytes for the data to transfer.Each byte that is written to will be transferred to RAM regardless of whether all 31 bytes are written or not.

Clock/Calendar

The time and calendar information is obtained by reading the appropriate register bytes.Table 3 illustrates the RTC registers.The time and calendar are set or initialized by writing the appropriate register bytes.The contents of the time and calendar registers are in the binary-coded decimal (BCD)format.

The day-of-week register increments at midnight.Values that correspond to the day of week are user-defined but must be sequential (i.e.,if 1 equals Sunday,then 2 equals Monday,and so on.).Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers,secondary (user)buffers are used to prevent errors when the internal registers update.When reading the time and date registers,the user buffers are synchronized to the internal registers the rising edge of CE.

The countdown chain is reset whenever the seconds register is written.Write transfers occur on the falling edge of CE.To avoid rollover issues,once the countdown chain is reset,the remaining time and date registers must be written within 1 second.

The DS1302 can be run in either 12-hour or 24-hour mode.Bit 7 of the hours register is defined as the 12-or 24-hour mode-select bit.When high,the 12-hour mode is selected.In the 12-hour mode,bit 5 is the AM/PM bit with logic high being PM.In the 24-hour mode,bit 5 is the second 10-hour bit(20-23 hours).The hours data must be re-initialized whenever the 12/24 bit is changed.

Clock Halt Flag

Bit 7 of the seconds register is defined as the clock halt (CH)flag.When this bit is set to logic 1,the clock oscillator is stopped and the DS1302 is placed into a low-power standby mode with a current drain of less than 100nA.When this bit is written to logic 0,the clock will start.The initial power-on state is not defined.

Write-Protect Bit

Bit 7 of the control register is the write-protect bit.The first seven bits (bits 0 to 6)are forced to 0 and always read 0 when read.Before any write operation to the clock or RAM,bit 7 must be 0.When high,the write-protect bit prevents a write operation to any other register.The initial power-on state is not defined.Therefore,the WP bit should be cleared before attempting to write to the device.

Trickle-Charge Register

This register controls the trickle-charge characteristics of the DS1302.The simplified schematic of Figure 5 shows the basic components of the trickle charger.The trickle-charge select (TCS)bits (bits 4 to 7)control the selection of the trickle charger.To prevent accidental enabling,only a pattern of 1010 enables the trickle charger.All other patterns will disable the trickle charger.The DS1302 powers up with the trickle charger disabled.The diode select (DS)bits (bits 2 and 3)select whether one diode or two diodes are connected between Vcc_2 and Vcc_1.If DS is 01, one diode is selected or if DS is 10,two diodes are selected.If DS is 00 or 11,the trickle charger is disabled independently of TCS. The RS bits (bits 0 and 1)select the resistor that is connected between Vcc_2 and Vcc_1.The resistor and diodes are selected by the RS and DS bits as shown in Table 2.

Table 2.Trickle Charger Resistor and Diode Select

TCS BIT7	TCS BIT6	TCS BIT5	TCS BIT4	TCS BIT3	TCS BIT2	TCS BIT1	TCS BIT0	FUNCTION
×	×	×	×	×	×	0	0	D disabled
×	×	×	×	0	0	×	×	D disabled
×	×	×	×	1	1	×	×	D disabled
1	0	1	0	0	1	0	1	1 Diode，2KΩ
1	0	1	0	0	1	1	0	1 Diode，4KΩ
1	0	1	0	0	1	1	1	1 Diode，8KΩ
1	0	1	0	1	0	0	1	2 Diodes，2KΩ
1	0	1	0	1	0	1	0	2 Diodes，4KΩ
1	0	1	0	1	0	1	1	2 Diodes，8KΩ
0	1	0	1	1	1	0	0	Initial power-on state

Diode and resistor selection is determined by the user according to the maximum current desired for battery or super cap charging.The maximum charging current can be calculated as illustrated in the following example. Assume that a system power supply of 5V is applied to Vcc2 and a super cap is connected to Vcc1.Also assume that the trickle charger has been enabled with one diode and resistor R1 between Vcc2 and Vcc1.The maximum current IMAx would therefore be calculated as follows:

$$I_{MAX} = (5.0V - diode\ drop) / R1 \approx (5.0V - 0.7V) / 2k\Omega \approx 2.2mA$$

As the super cap charges,the voltage drop between Vcc2 and Vcc1 decreases and therefore the charge current decreases.

Clock/Calendar Burst Mode

The clock/calendar command byte specifies burst mode operation.In this mode,the first eight clock/calendar registers can be consecutively read or written (see Table 3)starting with bit 0 of address 0.

If the write-protect bit is set high when a write clock/calendar burst mode is specified,no data transfer will occur to any of the eight clock/calendar registers (this includes the control register).The trickle charger is not accessible in burst mode.At the beginning of a clock burst read,the current time is transferred to a second set of registers.The time information is read from these secondary registers,while the clock may continue to run.This eliminates the need to re-read the registers in case of an update of the main registers during a read

Ram

The static RAM is 31x8 bytes addressed consecutively in the RAM address space.

Ram Burst Mode

The RAM command byte specifies burst mode operation.In this mode,the 31 RAM registers can be consecutively read or written (see Table 3)starting with bit 0 of address 0.

Register Summary
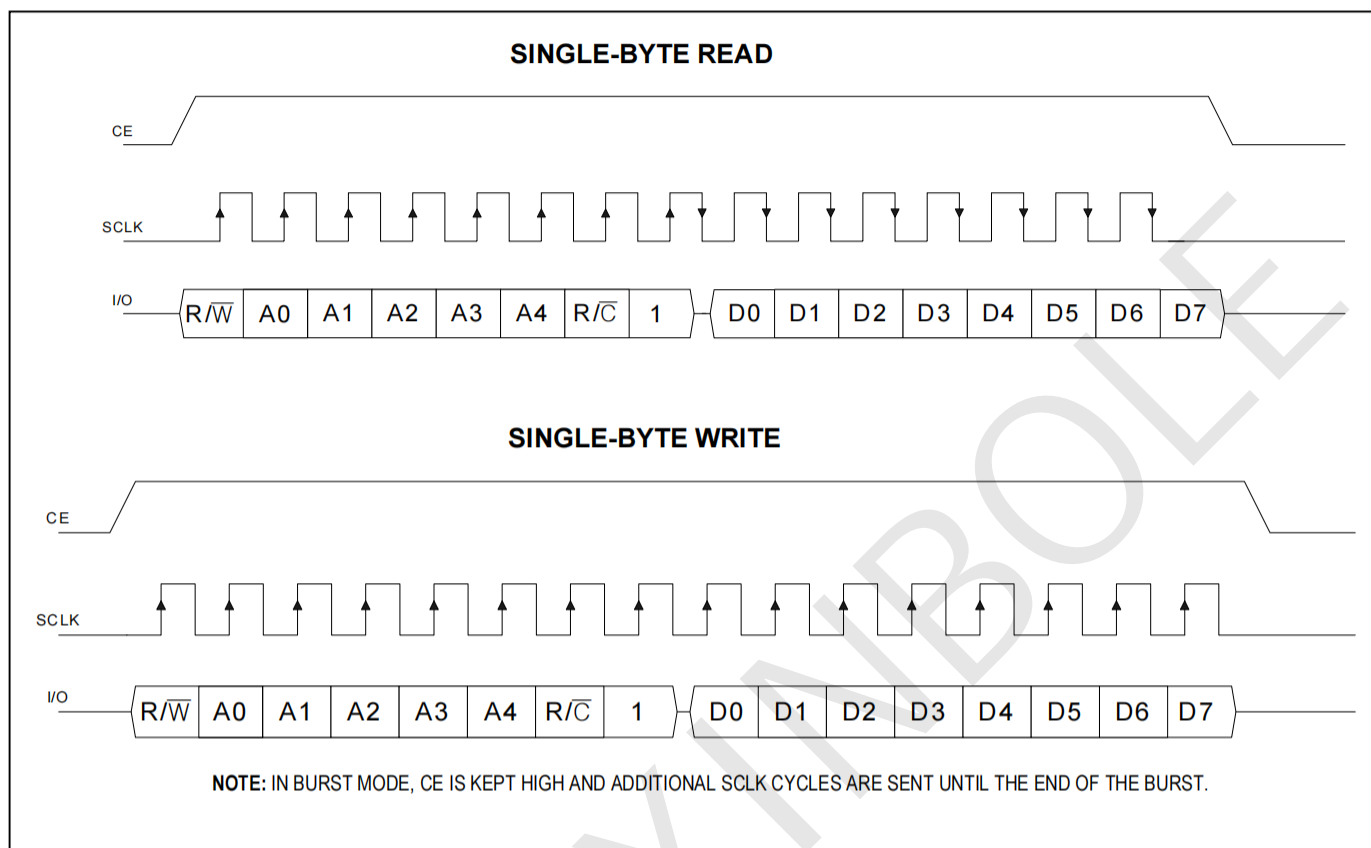
A register data format summary is shown in Table 3.

Table 3 . RTC

READ	WRITE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RANGE
81h	80h	CH	10 Seconds			Seconds				00–59
83h	82h		10 Minutes			Minutes				00–59
85h	84h	$12/\overline{24}$	0	$\dfrac{10}{\overline{AM/PM}}$ Hour	Hour	Hour				1–12/0–23
87h	86h	0	0	10 Date		Date				1–31
89h	88h	0	0	0	10 Month	Month				1–12
8Bh	8Ah	0	0	0	0	0	Day			1–7
8Dh	8Ch	10 Year				Year				00–99
8Fh	8Eh	WP	0	0	0	0	0	0	0	—
91h	90h	TCS	TCS	TCS	TCS	DS	DS	RS	RS	—

Crystal Selection

A 32.768kHz crystal can be directly connected to the DS1302 via pins 2 and 3(X1,X2).In order to improve the accuracy of high running, a set of 6pF-30pF negative load compensation capacitors should be placed outside the crystal end. The specific capacity is determined by the application layout and crystal burst.

Figure 4.Data Transfer Summary

SINGLE-BYTE READ

CE	SCLK	I/O

I/O: R/$\overline{W}$ | A0 | A1 | A2 | A3 | A4 | R/$\overline{C}$ | 1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7

SINGLE-BYTE WRITE

CE	SCLK	I/O

I/O: R/$\overline{W}$ | A0 | A1 | A2 | A3 | A4 | R/$\overline{C}$ | 1 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7

NOTE: IN BURST MODE, CE IS KEPT HIGH AND ADDITIONAL SCLK CYCLES ARE SENT UNTIL THE END OF THE BURST.

Clock Burst

BFh	BEh

Ram Burst

FFh	FEh

Ram

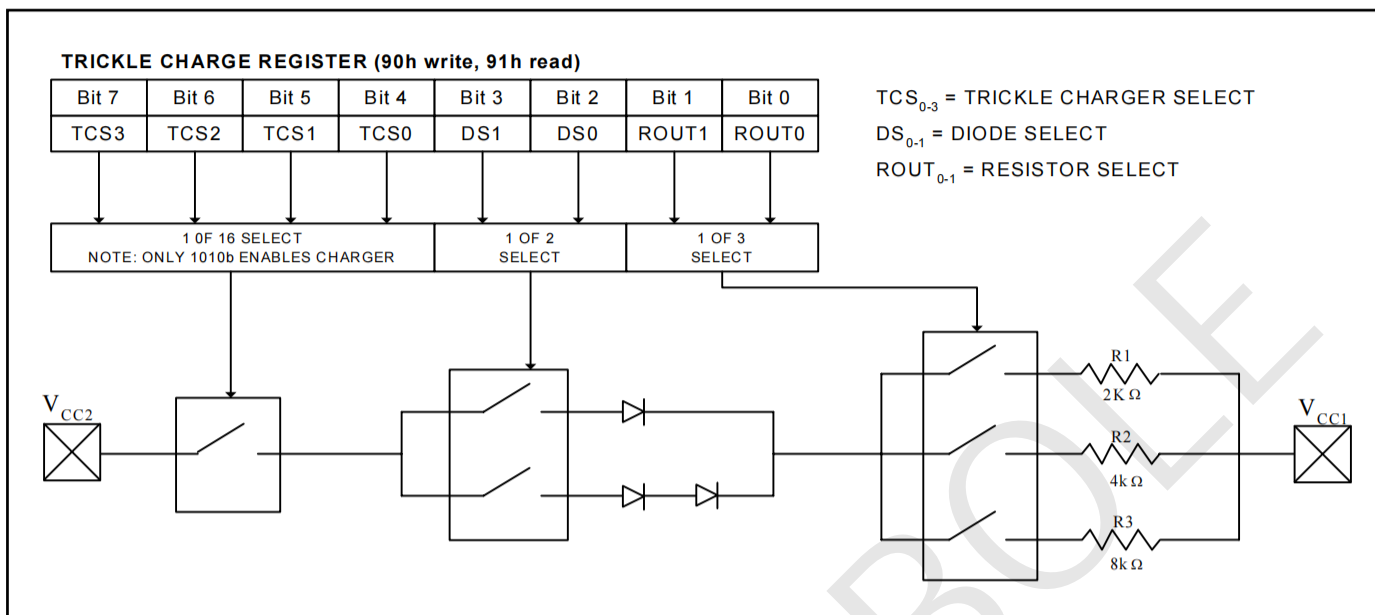| C1h	C0h		00-FFh
C3h	C2h		00-FFh
C5h	C4h		00-FFh
.	.		.
.	.		.
.	.		.
FDh	FCh		00-FFh

Figure 5.Programmable Trickle Charger

Figure 6.Timing Diagram:Read Data Transfer

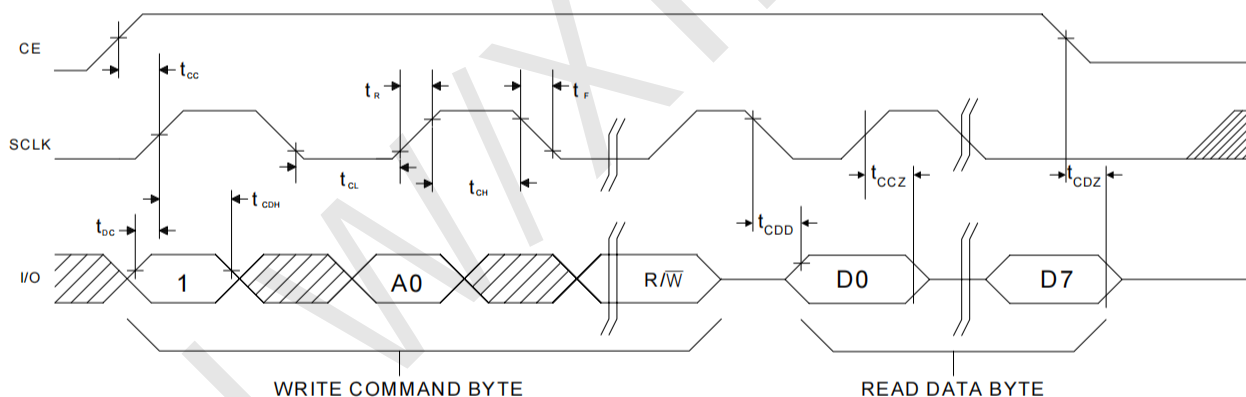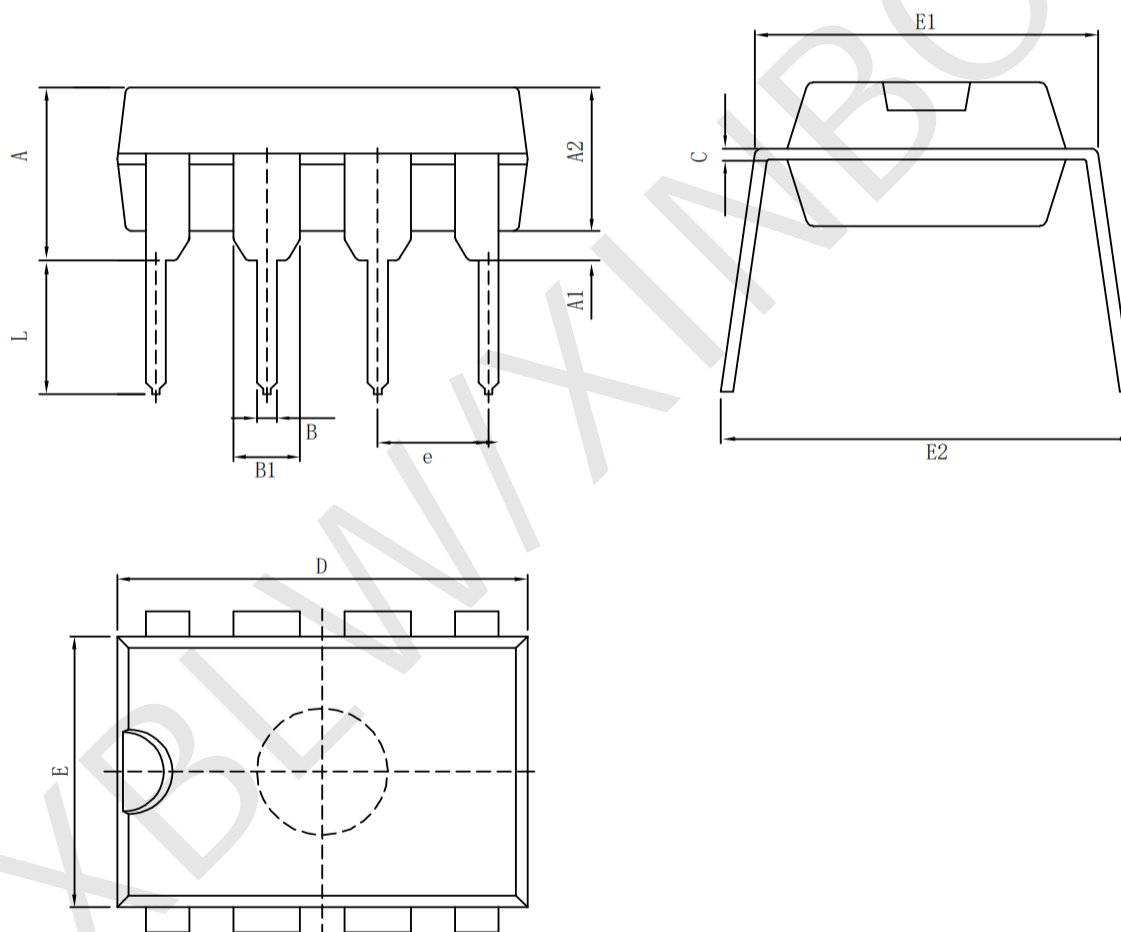**Figure 7.Timing Diagram:Write Data Transfer**
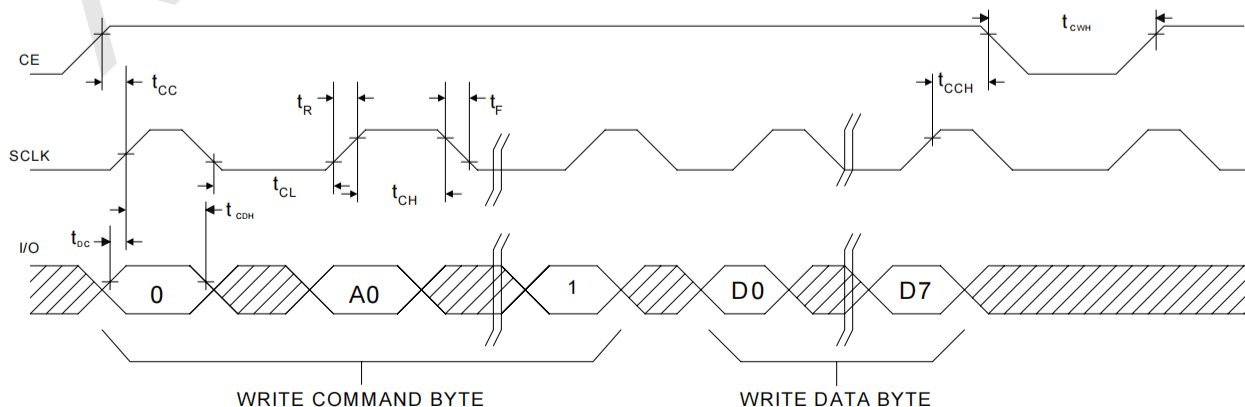
Package Information

· DIP-8

Size Symbol	Dimensions In Millimeters		Size Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	3.710	4.310	A	0.146	0.170
A1	0.510		A1	0.020	
A2	3.200	3.600	A2	0.126	0.142
B	0.380	0.570	B	0.015	0.022
B1	1.524(BSC)		B1	0.060(BSC)	
C	0.204	0.360	C	0.008	0.014
D	9.000	9.400	D	0.354	0.370
E	6.200	6.600	E	0.244	0.260
E1	7.320	7.920	E1	0.288	0.312
e	2.540(BSC)		e	0.100(BSC)	
L	3.000	3.600	L	0.118	0.142
E2	8.400	9.000	E2	0.331	0.354

• SOP-8

Size Symbol	Dimensions In Millimeters		Size Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	1.350	1.750	A	0.053	0.069
A1	0.100	0.250	A1	0.004	0.010
A2	1.350	1.550	A2	0.053	0.061
b	0.330	0.510	b	0.013	0.020
c	0.170	0.250	c	0.006	0.010
D	4.700	5.100	D	0.185	0.200
E	3.800	4.000	E	0.150	0.157
E1	5.800	6.200	E1	0.228	0.224
e	1.270 (BSC)		e	0.050 (BSC)	
L	0.400	1.270	L	0.016	0.050
θ	0°	8°	θ	0°	8°
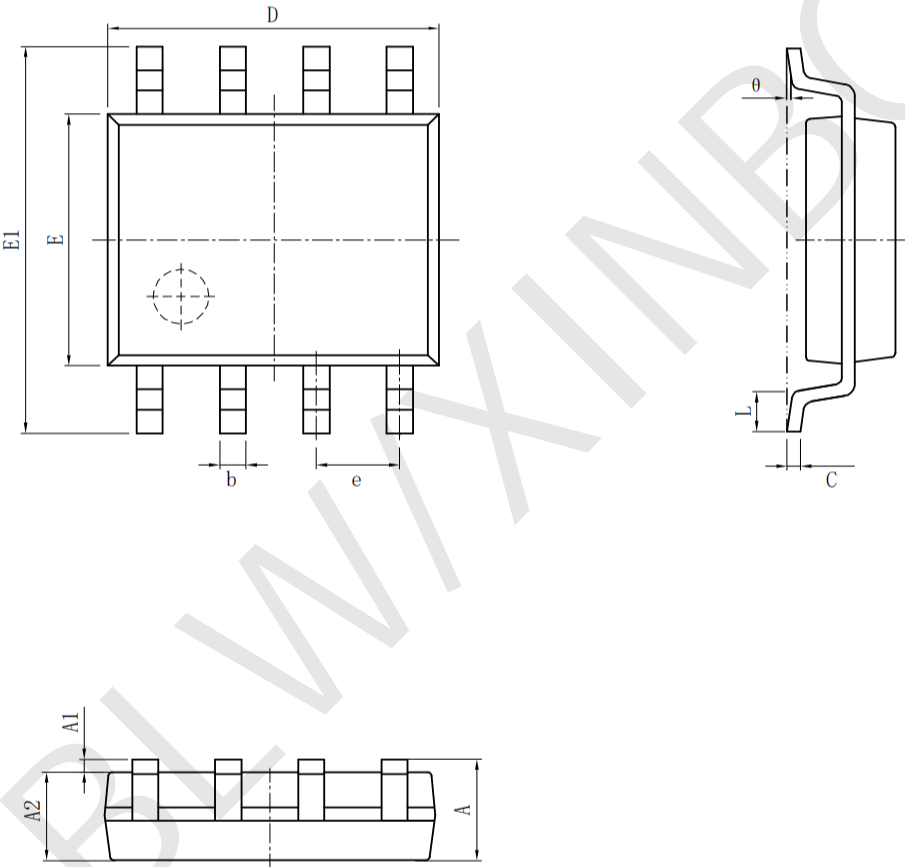
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