

Power Amplifier

5.9 - 9.5 GHz



XP1035-QH

Rev. V3

Features

- 26 dB Small Signal Gain
- 39 dBm Third Order Intercept Point (OIP3)
- Integrated Power Detector
- Lead-Free 4 mm 24-lead QFN Package
- 100% RF Testing
- RoHS* Compliant

Applications

- Point to Point
- SATCOM
- VSAT

Description

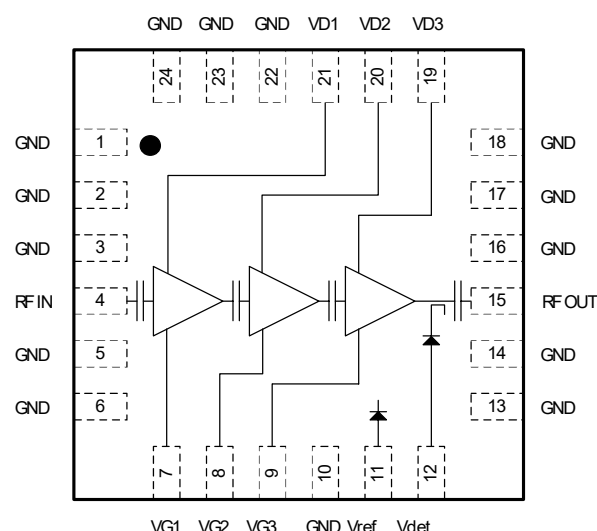
The XP1035-QH is a packaged linear power amplifier that operates over the 5.9-9.5 GHz frequency band. The device provides 26 dB gain and 39 dBm Output Third Order Intercept Point (OIP3) across the band and is offered in an industry standard, fully molded 4 mm QFN package. The packaged amplifier is comprised of a three stage power amplifier with an integrated, temperature compensated on-chip power detector. The device includes on-chip ESD protection structures and DC by-pass capacitors to ease the implementation and volume assembly of the packaged part. The device is manufactured in GaAs PHEMT device technology with BCB wafer coating to enhance ruggedness and repeatability of performance. The XP1035-QH is specifically designed for Point to Point radio applications and is well suited for other telecom applications such as SATCOM and VSAT.

Ordering Information¹

Part Number	Package
XP1035-QH-0G00	bulk quantity
XP1035-QH-0G0T	tape and reel
XP1035-QH-EV1	evaluation module

1. Reference Application Note M513 for reel size information.

Functional Schematic



Pin Configuration ²

Pin #	Function
1-3, 5-6, 10, 13-14, 16-18, 22-24	Ground
4	RF Input
7	Gate 1 Bias
8	Gate 2 Bias
9	Gate 3 Bias
11	Pwr Det Ref.
12	Pwr Det
15	RF Output
19	Drain 3 Bias
20	Drain 2 Bias
21	Drain 1 Bias

2. The exposed pad centered on the package bottom must be connected to RF and DC ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: 5.9 - 9.5 GHz, T_A = 25°C

Parameter	Units	Min.	Typ.	Max.
Small Signal Gain (S21)	dB	-	26	-
Input Return Loss (S11)	dB	-	13	-
Output Return Loss (S22)	dB	-	10	-
Reverse Isolation (S12)	dB	-	45	-
Psat	dBm	-	29	-
P1dB	dBm	-	27.5	-
OIP3	dBm	-	39	-
Drain Bias Voltage (Vd1,2,3)	VDC	-	6	-
Detector Bias Voltage (Vdet,ref)	VDC	-	5	-
Gate Bias Voltage (Vg1,2,3)	VDC	-2	-1	-
Supply Current (Id1)	mA	-	70	-
Supply Current (Id2)	mA	-	140	-
Supply Current (Id3)	mA	-	280	-

Absolute Maximum Ratings^{3,4}

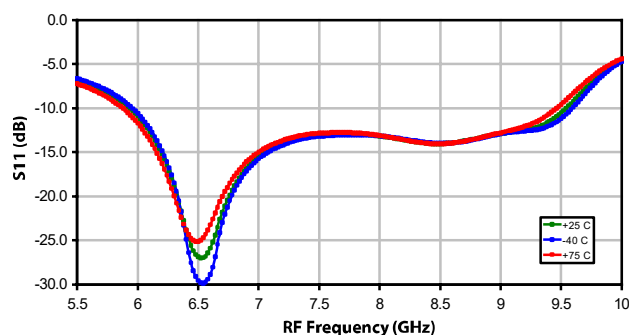
Parameter	Absolute Maximum
Supply Voltage (Vd1,2,3)	+7.2 V
Supply Current (Id1,2,3)	600 mA
Gate Bias Voltage (Vg1,2,3)	-3 V
Power Dissipation (P _{diss})	4.2 W
RF Input Power	+15 dBm
Operating Temperature (T _a)	-55°C to +85°C
Storage Temperature (T _{stg})	-65°C to +165°C
Channel Temperature (T _{ch}) ²	150°C
MSL Level (MSL)	MSL1

3. Operation of this device above any one of these parameters may cause permanent damage.

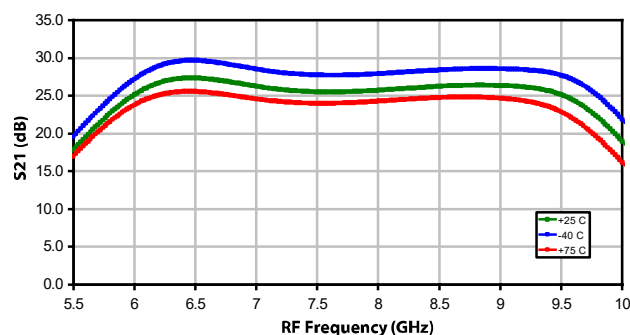
4. Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.

Typical Performance Curves

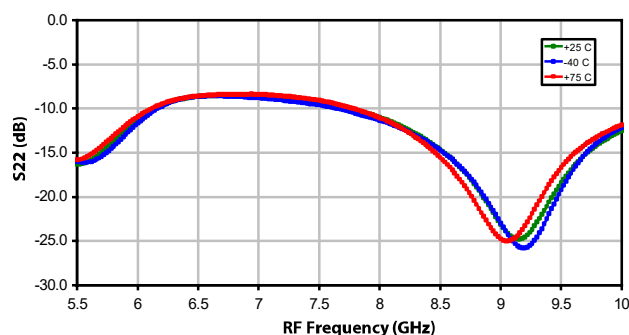
XP1035-QH: S₁₁ (dB) at V_d=6V, I_d=500mA



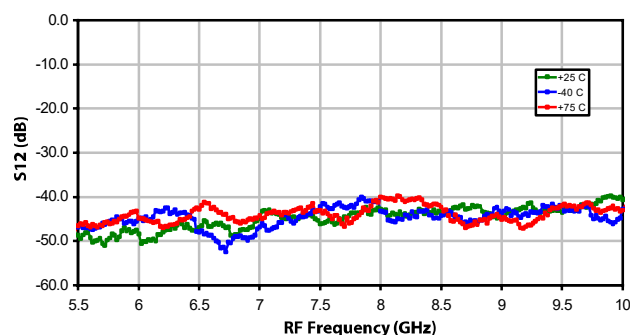
XP1035-QH: S₂₁ (dB) at V_d=6V, I_d=500mA



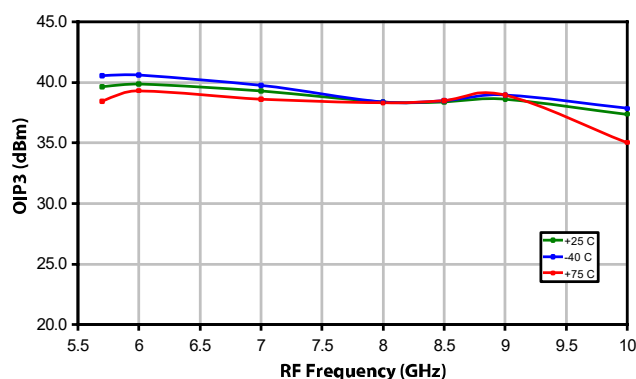
XP1035-QH: S₂₂ (dB) at V_d=6V, I_d=500mA



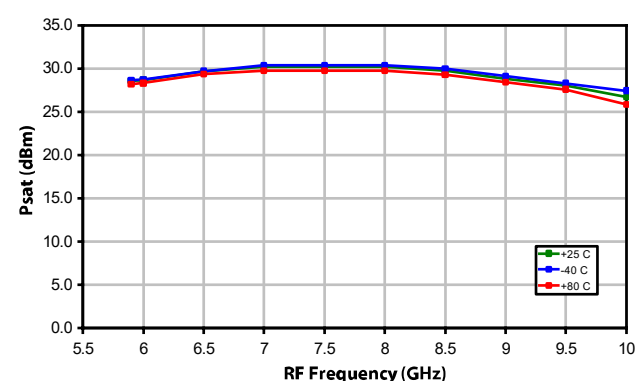
XP1035-QH: S₁₂ (dB) at V_d=6V, I_d=500mA



XP1035-QH: OIP₃ (dBm) at V_d=6V, I_d=500mA

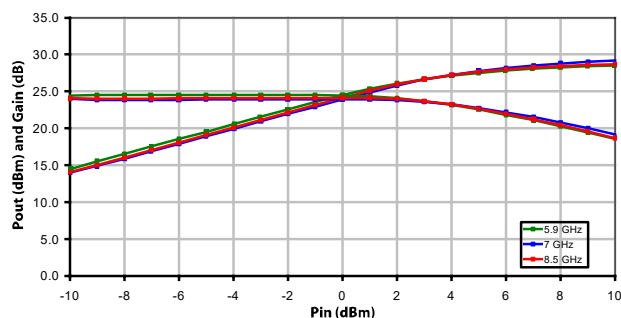


XP1035-QH: P_{sat} (dBm) at I_d=500mA, V_d=6V

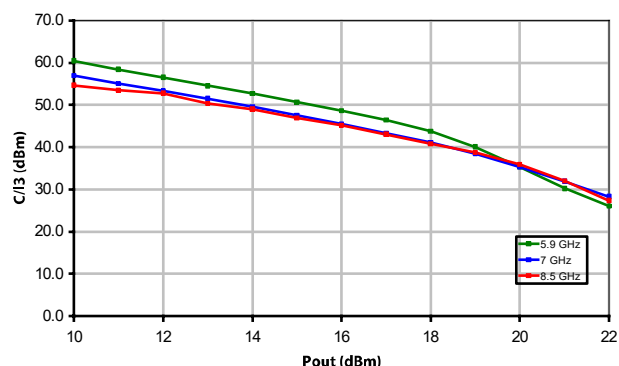


Typical Performance Curves

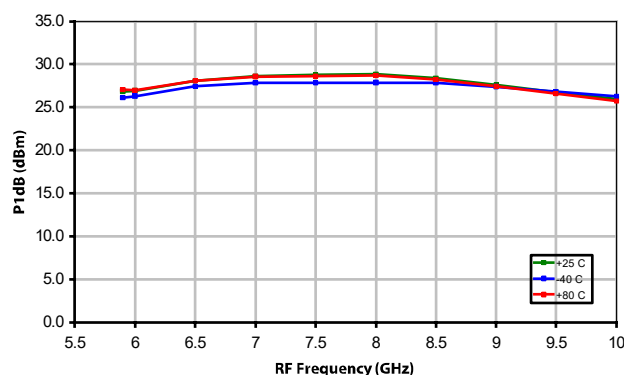
XP1035-QH: Pout (dBm) and Gain (dB) vs Pin (dBm)
Id=500mA, Vd=6V, +25 C



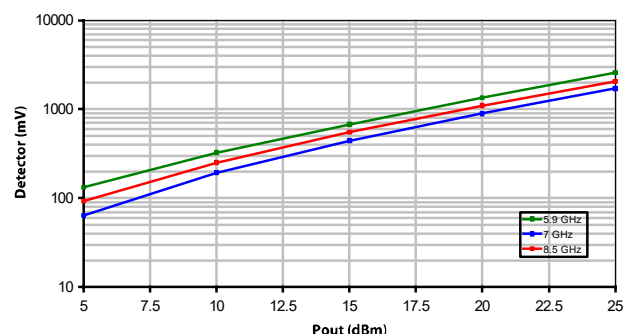
XP1035-QH: C/I3 vs Pout at Id=500mA, Vd=6V, +25 C, 10 MHz Span



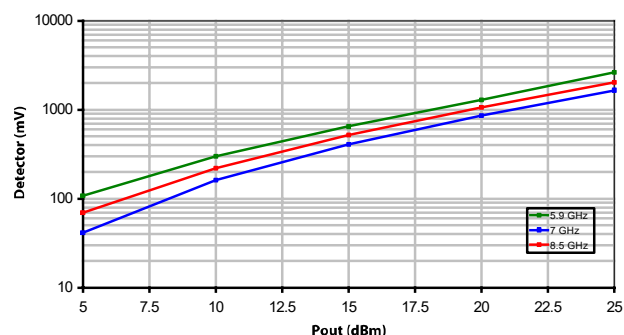
XP1035-QH: P1dB (dBm) at Id=500mA, Vd=6V



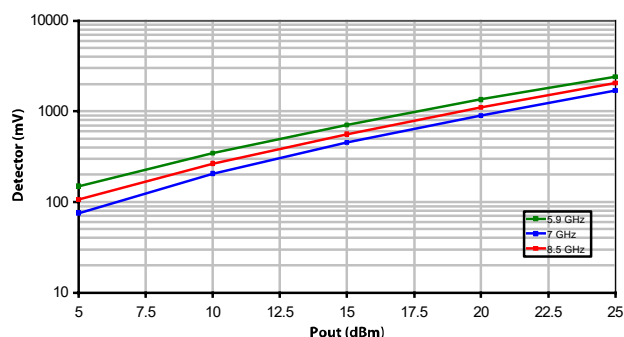
XP1035-QH: Detector (mV) vs Pout (dBm) at Id=500mA, Vd=6V, +25 C



XP1035-QH: Detector (mV) vs Pout (dBm) at Id=500mA, Vd=6V, -40 C

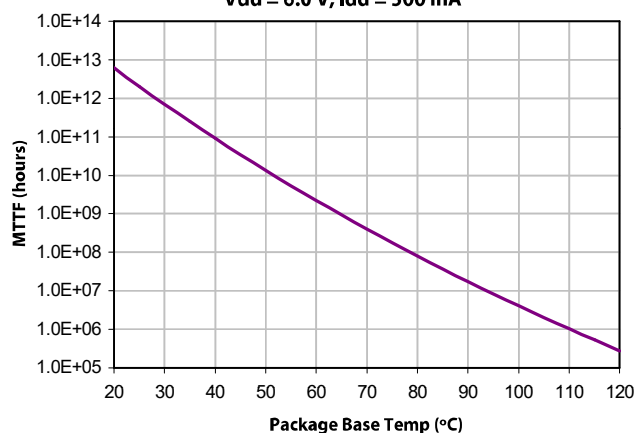


XP1035-QH: Detector (mV) vs Pout (dBm) at Id=500mA, Vd=6V, +80 C

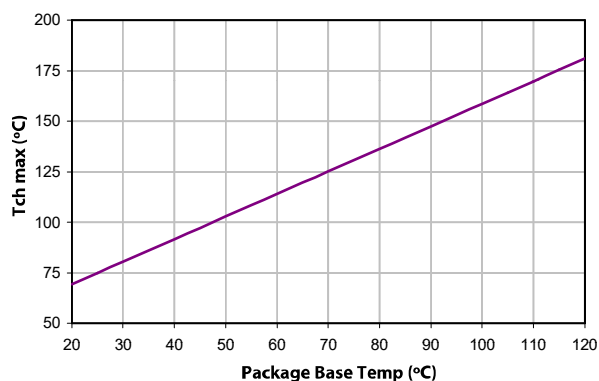


MTTF

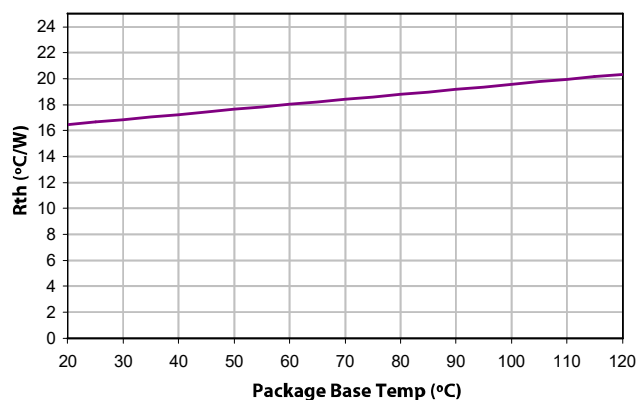
XP1035-QH-0G00: MTTF (hours) vs. Package Base Temperature
Vdd = 6.0 V, Idd = 500 mA



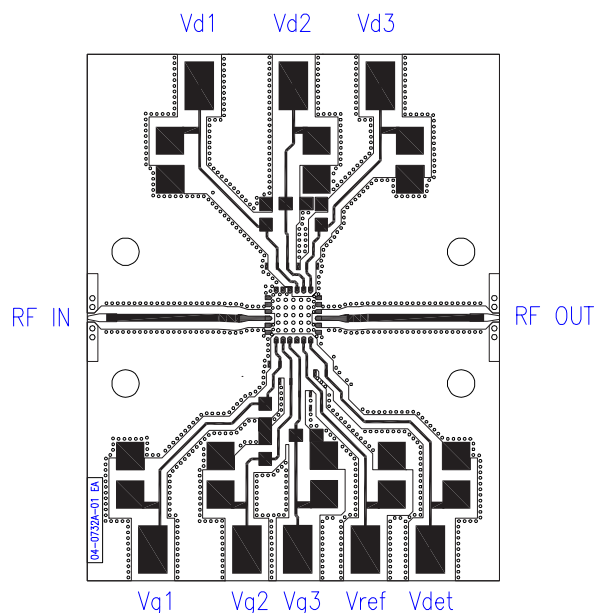
XP1035-QH-0G00: MTTF (hours) vs. Package Base Temperature
Vdd = 6.0 V, Idd = 500 mA



XP1035-QH-0G00: Rth vs. Package Base Temperature
Vdd = 6.0 V, Idd = 500 mA



Recommended Layout



Recommended Decoupling Capacitors: 100pF 0402, 10 μ F 0805

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

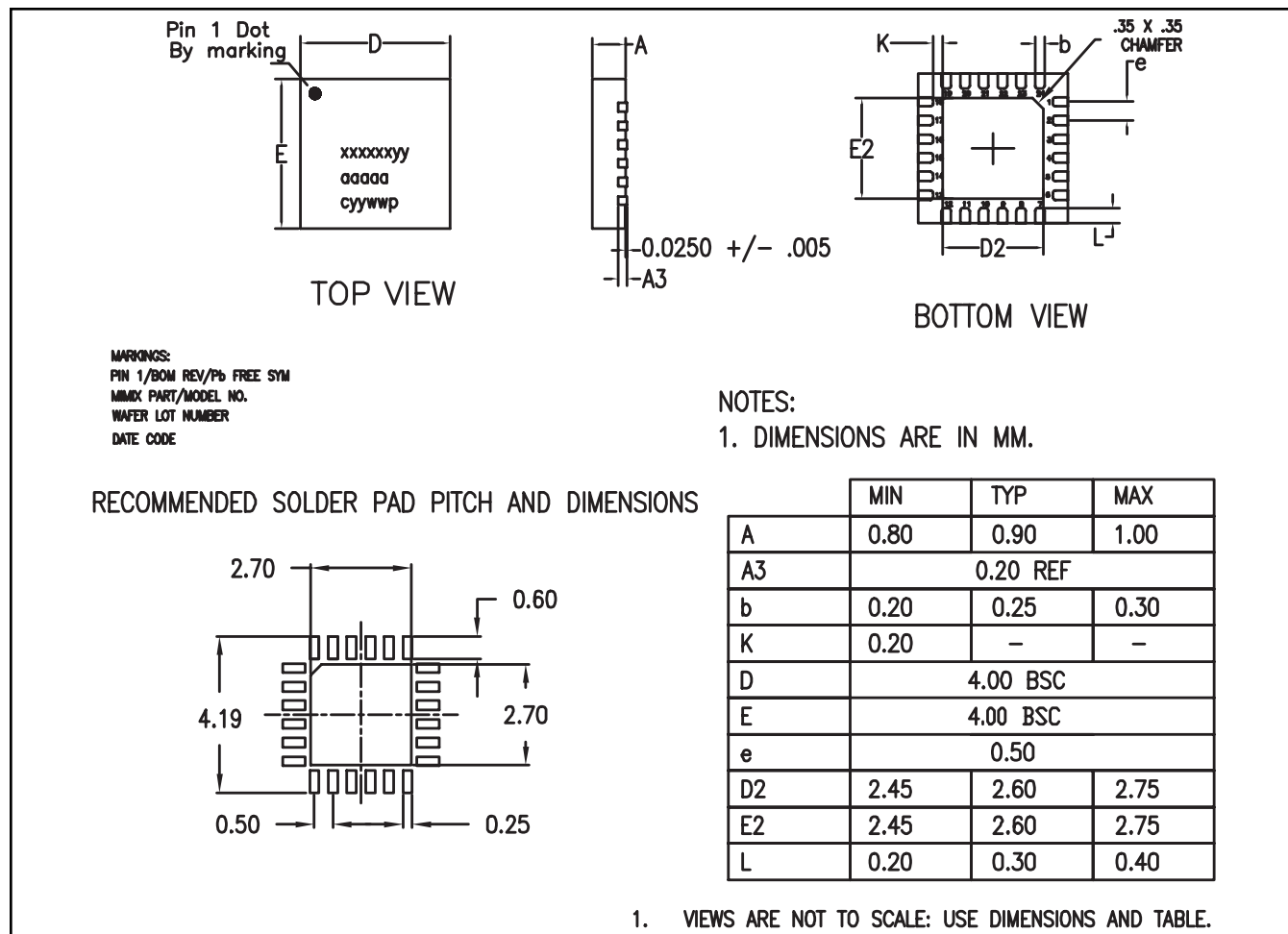
App Note [1] Biasing -

As shown in the Pin Designations table, the device is operated by biasing VD1,2,3 at 5 V with 70, 140, 280 mA respectively. It is recommended to use active bias to keep the currents constant in order to maintain the best performance over temperature. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is -1 V. Make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

App Note [2] Board Layout -

As shown in the board layout, it is recommended to provide 100 pF decoupling caps as close to the bias pins as possible, with additional 10 μ F decoupling caps.

Lead-Free 4 mm 24-Lead PQFN[†]



[†] Reference Application Note S2083 for lead-free solder reflow recommendations.
Plating is 100% matte tin over copper.

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