

## 40 V, 3 A, Synchronous Buck Regulator Module with Low EMI and 6 $\mu$ A Quiescent Current

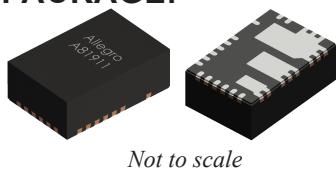
### FEATURES AND BENEFITS

- AEC-Q100 Grade 1 qualified
- ClearPower module DC/DC converter with internal passive components
- **V<sub>IN</sub> Range:** 3.5 to 36 V operating, 40 V transient
- **V<sub>OUT</sub>:** 0.8 to 24 V,  $\pm 1.5\%$  accuracy,  $-40^\circ\text{C}$  to  $150^\circ\text{C}$
- **Up to 3 A** of continuous output current
- **Ultra-Low EMI** design and selectable spread spectrum to easily pass CISPR25 Class 5
- **Low-Power (LP) mode:** 6  $\mu$ A I<sub>Q</sub> from V<sub>IN</sub> at no load, automatic transition from LP to PWM mode
- **Fixed Frequency PWM (f<sub>OSC</sub>):** 1 MHz to 2.4 MHz, programmable
- **Synchronization (1 MHz to 2.4 MHz):** PLL-based, f<sub>SYNC</sub> can be above or below f<sub>OSC</sub>
- CLK<sub>OUT</sub>: Phase-shifted clock output for reduced EMI in multi-converter systems
- Accurate enable input threshold
- Overvoltage, pulse-by-pulse current limit, hiccup mode short-circuit, and thermal protections
- Robust FMEA: pin open/short and component faults

### APPLICATIONS:

- Infotainment
- Navigation systems
- ADAS
- Industrial systems

### PACKAGE:



32-pin QFN  
4 mm × 6 mm × 2.1 mm  
with wettable flank  
(suffix NB)

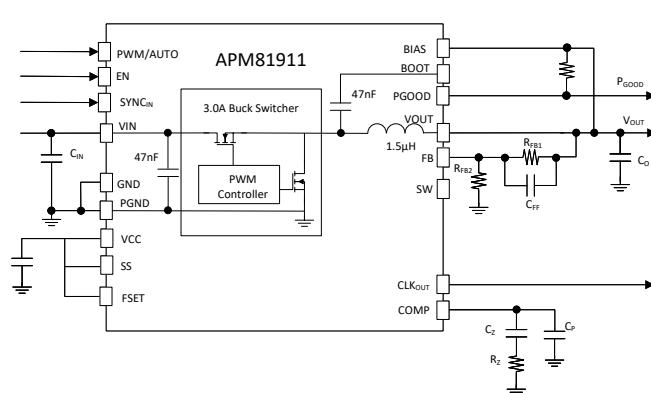


Figure 1: APM81911 Typical Application Circuit

### DESCRIPTION

The APM81911 is a highly integrated, 3 A, low EMI, DC-DC buck regulator module that satisfies demanding power delivery requirements. The APM81911 includes a high-performance DC-DC regulator IC, two capacitors, and an inductor in a compact 4 mm × 6 mm QFN package. The module includes all the control and protection circuitry necessary to produce a robust and scalable DC-DC regulator solution with  $\pm 1.5\%$  output voltage accuracy over the full operating temperature range.

The fixed frequency, peak current mode control is programmable from 1 MHz to 2.4 MHz, ensuring rapid response to load and line transients. A 2.15 MHz PWM switching frequency is programmed by connecting the FSET pin to VCC. The VIN and BOOT pin bypass capacitors are integrated into the module to greatly reduce noise-generating hot loops which significantly improves radiated EMI. Spread spectrum operation (dithering) is available to further reduce EMI. The APM81911-1 part variant is available for applications where dithering is not desired.

The Low Power (LP) mode maintains the output voltage at no-load or very light load conditions while drawing only microamps from V<sub>IN</sub>. At no-load, the APM81911 draws only 6  $\mu$ A. The transition between PWM and LP modes is automatic in response to the load demand. PWM-only operation is available to prevent pulse skipping at light load conditions.

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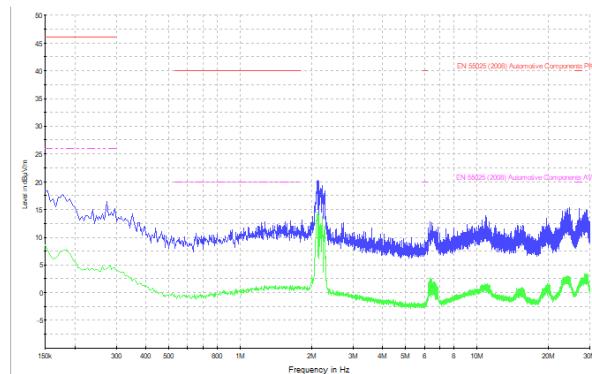


Figure 2: APM81911 Radiated Emissions from 150 kHz to 30 MHz (Monopole Antenna)

**DESCRIPTION (continued)**

The APM81911 can synchronize to an external clock signal with frequency ranging from 1 MHz to 2.4 MHz applied to the SYNC\_IN pin. The APM81911 provides a CLK<sub>OUT</sub> pin so “downstream” regulators can easily be interleaved and dithered via their synchronization inputs.

The APM81911 includes adjustable soft-start, an open-drain power good output, and a low shutdown current of 1  $\mu$ A. The accurate enable input allows for programmable turn-on and turn-off thresholds.

Extensive protection features of the APM81911 include pulse-by-pulse current limit, hiccup mode short-circuit protection, BOOT open/short voltage protection, V<sub>IN</sub> undervoltage lockout, V<sub>OUT</sub> overvoltage protection, and thermal shutdown. The APM81911 is offered in a thermally enhanced, 4 mm  $\times$  6 mm  $\times$  2.1 mm 32-pin wettable flank QFN package (suffix “NB”) with exposed power pads.

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**SELECTION GUIDE**

Part Number	Dither	Description	Packing <sup>[1]</sup>	Lead Finish
APM81911KNBATOR	Enabled	32-pin wettable flank QFN package with thermal pad	3000 pieces per 13-inch reel	Matte Tin
APM81911KNBATOR-1	Disabled			

<sup>[1]</sup> Contact Allegro for additional packing options.

**ABSOLUTE MAXIMUM RATINGS<sup>[1]</sup>**

Characteristic	Symbol	Notes	Rating	Unit
V <sub>IN</sub> , EN, PGOOD, BIAS	V <sub>IN</sub> , V <sub>EN</sub> , V <sub>PGOOD</sub> , V <sub>BIAS</sub>		−0.3 to 40	V
V <sub>OUT</sub>	V <sub>OUT</sub>		−0.3 to 24	V
SW	V <sub>SW</sub>	Continuous	−0.3 <sup>[2]</sup> to V <sub>IN</sub> + 0.3	V
		V <sub>IN</sub> ≤ 36 V, t < 50 ns	−1.0 to V <sub>IN</sub> + 2	V
BOOT	V <sub>BOOT</sub>	Continuous	V <sub>SW</sub> − 0.3 to V <sub>SW</sub> + 3.5	V
		t < 1 ms	V <sub>SW</sub> − 0.3 to V <sub>SW</sub> + 7.0	V
All other pins			−0.3 to 5.5	V
Operating Junction Temperature	T <sub>J(max)</sub>		−40 to 150	°C
Storage Temperature	T <sub>STG</sub>		−55 to 150	°C

<sup>[1]</sup> Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>[2]</sup> This voltage is a function of temperature.

**THERMAL CHARACTERISTICS<sup>[1]</sup>**: May require derating at maximum conditions; see application section

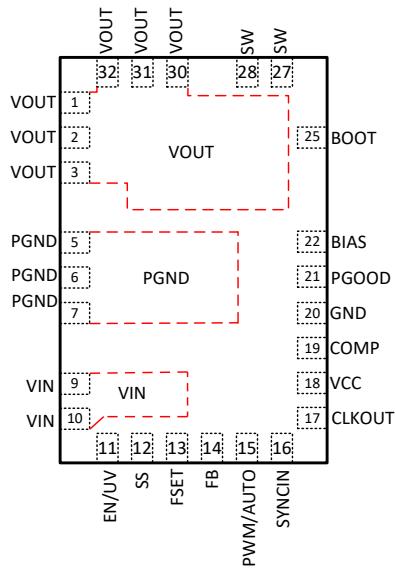
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	R <sub>θJA</sub>	On 4-layer PCB based on JEDEC standard	48	°C/W

<sup>[1]</sup> Additional thermal information available on the Allegro website.

## PINOUT DIAGRAM AND TERMINAL LIST

## QFN-32 Pinout Diagram

PCB schematic and layout library files available for download on the [APM81911 product page](#)



## Terminal List

Number	Name	Function
1, 2, 3, 30, 31, 32	VOUT	Power output of buck regulator. Connect output filter capacitor from this pin to GND.
5, 6, 7	PGND	Power ground pins for the lower MOSFET, gate driver, and BOOT charge circuit.
9, 10	VIN	Power input for the control circuits and the drain of the internal high-side N-channel MOSFET. A high-quality ceramic capacitor should be connected directly between VIN and PGND with short and wide PCB traces to minimize EMI. The package pinout is designed with this consideration.
11	EN/UV	EN/UV is an input to a hysteretic comparator with an accurate 1.2 V (typical) threshold. A voltage on EN/UV above the nominal 1.2 V threshold enables the APM81911. Once enabled, the EN/UV comparator has a typical hysteresis of 300 mV. Once enabled, if EN/UV is lowered below 0.9 V (typical), the APM81911 will enter the shutdown state, stop switching and draw only 1 $\mu$ A (typical) from Vin. Connect EN/UV directly to VIN for "always-on" applications. When EN is not connected directly to VIN, the rising edge of EN must be compatible to a digital signal.
12	SS	Soft-start pin. Connect a capacitor, $C_{SS}$ , from this pin to GND to set the startup time. This capacitor also determines the hiccup period during overcurrent. Connect SS directly to VCC to program a fixed 880 $\mu$ s (typical) startup time.
13	FSET	Frequency setting pin. A resistor, $R_{FSET}$ , from this pin to GND sets the base oscillator frequency, $f_{OSC}$ . Connect FSET directly to VCC to program a fixed 2.15 MHz (typical) frequency.
14	FB	Feedback, negative input to the error amplifier. Connect a resistor divider from the regulators output, VOUT, to this pin to program the output voltage.
15	PWM/AUTO	Dual function pin: <b>High/Low</b> . Setting this pin <b>high</b> forces PWM mode. Setting this pin <b>low</b> allows AUTO changeover between PWM and LP mode based on the load current.
16	SYNC <sub>IN</sub>	Triple function pin: <b>High/Low/ExtClock</b> . Setting this pin <b>high</b> sets CLK <sub>OUT</sub> to the internal oscillator frequency ( $f_{OSC}$ ) but with 180-degree phase shift. Setting this pin <b>low</b> disables the CLK <sub>OUT</sub> pin. Applying an <b>external clock</b> forces PWM mode, synchronizes the PWM switching frequency to the external clock, adds dithering, and sets CLK <sub>OUT</sub> to the same dithered frequency but with 180-degree phase shift. See Table 3 for details.
17	CLK <sub>OUT</sub>	Clock output pin. Frequency dithering is added to this pin. The exact functionality of this pin is dependent on the status of the SYNC <sub>IN</sub> pin, see Table 1 and the description for SYNC <sub>IN</sub> for additional details.
18	VCC	Internal voltage regulator bypass capacitor pin. Connect a 4.7 $\mu$ F capacitor from this pin to PGND and place it very close to the APM81911.
19	COMP	Output of the error amplifier and compensation node for the current-mode control loop. Connect a series RC network from this pin to GND for loop compensation.
20	GND	Analog ground pin.
21	PGOOD	Power good output signal. This pin is an open-drain output that transitions from low to high impedance after the output has maintained regulation for $t_{dPG(SU)}$ . If the output voltage is out of range (undervoltage or overvoltage), this pin will be low impedance. Connect a resistor from PGOOD to VCC for PGOOD to report a logic low when out of regulation.
22	BIAS	Output voltage sense pin. This pin should be connected to the output of the regulator. Voltage at this pin sets the internal slope compensation. It also supplies the internal circuitry when output voltage is high enough.
25	BOOT	This pin supplies the gate drive for the buck converter's high-side N-channel MOSFET. An internal 47 nF ceramic capacitor connects this pin to SW. Leave this pin open.
27, 28	SW	Switching node of the buck converter. Leave this pin open.
–	Exposed PADS	VIN, VOUT, and PGND exposed pads should be soldered to their respective traces for enhanced thermal dissipation.

## FUNCTIONAL BLOCK DIAGRAM

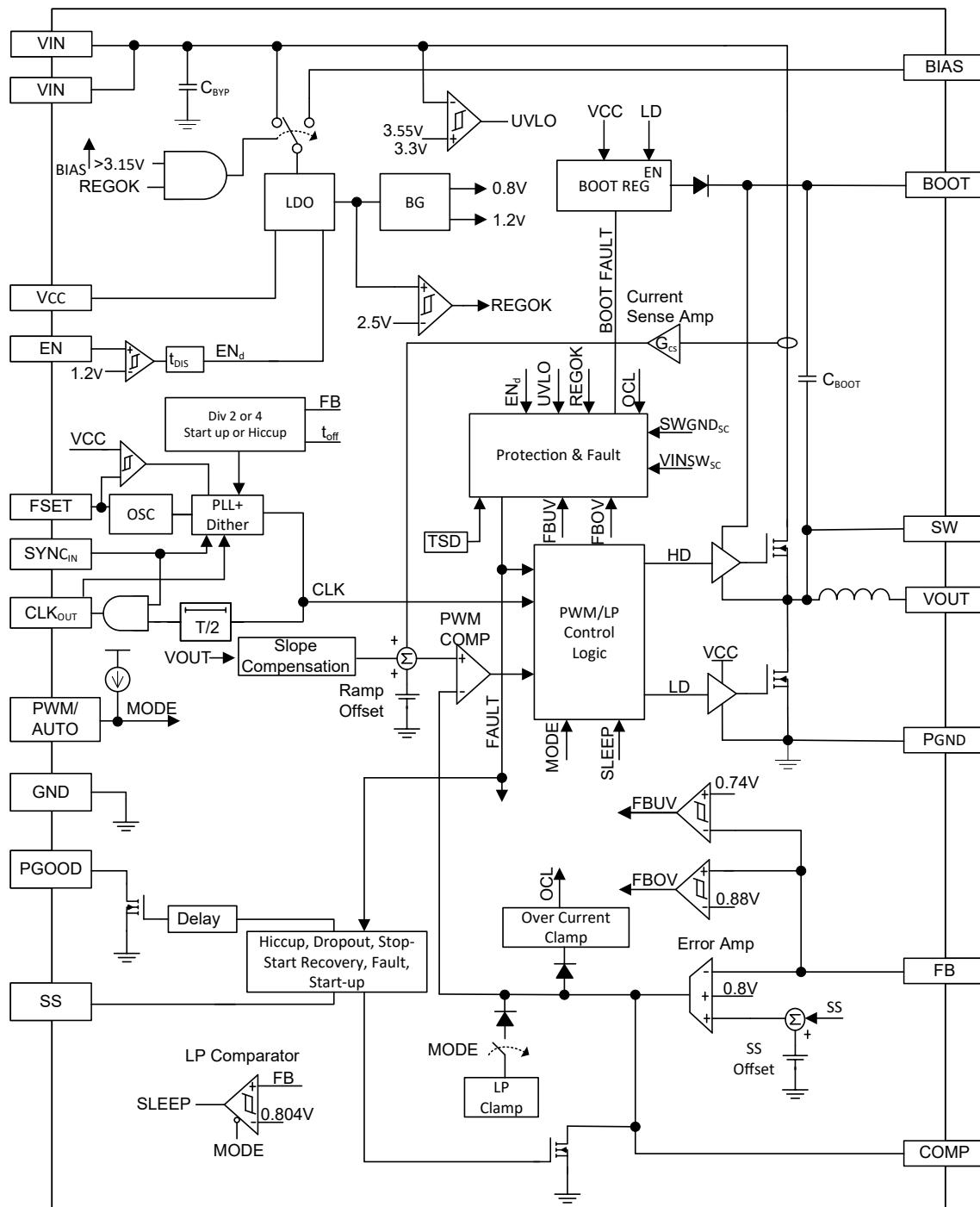


Figure 3: Functional Block Diagram

ELECTRICAL CHARACTERISTICS: Valid at  $3.5 \text{ V} \leq V_{IN} \leq 36 \text{ V}$ ,  $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$ , unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>INPUT VOLTAGE SPECIFICATIONS</b>						
Input Voltage Range [2]	$V_{IN}$	$V_{IN}$ must first rise above $V_{UVLO(ON,MAX)}$	3.5	-	36	V
UVLO Start	$V_{UVLO(ON)}$	$V_{IN}$ rising	3.35	3.55	3.8	V
UVLO Stop	$V_{UVLO(OFF)}$	$V_{IN}$ falling	3.1	3.3	3.5	V
UVLO Hysteresis	$V_{UVLO(HYS)}$		-	250	-	mV
<b>INPUT SUPPLY CURRENT</b>						
Input Shutdown Current [1]	$I_{IN(SD)}$	$V_{IN} = 12 \text{ V}$ , $V_{EN} = 0 \text{ V}$ , $V_{SW} = V_{IN}$ , $T_J = 25^\circ\text{C}$ [3]	-	1	2.9	$\mu\text{A}$
Input Current, PWM Mode [1]	$I_{IN(PWM)}$	$V_{IN} = 12 \text{ V}$ , $V_{EN} = 2 \text{ V}$ , no load, no switching	-	5	6.5	mA
3.3 $V_{OUT}$ LP Input Current [3][4]	$I_{LP(3.3V)}$	$V_{IN} = 12 \text{ V}$ , $I_{OUT} = 0 \mu\text{A}$ , $T_J = 25^\circ\text{C}$ , BIAS connected to $V_{OUT}$	-	6	-	$\mu\text{A}$
		$V_{IN} = 12 \text{ V}$ , $I_{OUT} = 50 \mu\text{A}$ , $T_J = 25^\circ\text{C}$ , BIAS connected to $V_{OUT}$	-	24.3	-	$\mu\text{A}$
5.0 $V_{OUT}$ LP Input Current [3][4]	$I_{LP(5.0V)}$	$V_{IN} = 12 \text{ V}$ , $I_{OUT} = 0 \mu\text{A}$ , $T_J = 25^\circ\text{C}$ , BIAS connected to $V_{OUT}$	-	7.5	-	$\mu\text{A}$
		$V_{IN} = 12 \text{ V}$ , $I_{OUT} = 50 \mu\text{A}$ , $T_J = 25^\circ\text{C}$ , BIAS connected to $V_{OUT}$	-	40	-	$\mu\text{A}$
<b>REGULATION ACCURACY (FB PIN)</b>						
Feedback Voltage Accuracy	$V_{FB}$	$-40^\circ\text{C} < T_J < 150^\circ\text{C}$ , $V_{IN} \geq 3.5 \text{ V}$	788	800	812	mV
<b>SWITCHING FREQUENCY AND DITHERING (FSET PIN)</b>						
PWM Switching Frequency	$f_{OSC}$	FSET connected to VCC	1.98	2.15	2.42	MHz
		$R_{FSET} = 34 \text{ k}\Omega$	0.90	1.00	1.10	MHz
		$R_{FSET} = 71.5 \text{ k}\Omega$	450	500	550	kHz
		$R_{FSET} = 86.6 \text{ k}\Omega$	360	410	460	kHz
		External clock on $SYNC_{IN}$ pin at $f_{SW(SYNC)}$	-	$f_{SW(SYNC)}$	-	kHz
Dropout Switching Frequency [3]	$f_{SW(DO)}$		-	$f_{OSC} / 2$	-	kHz
PWM Frequency Dither Range	$f_{DITH(RNG)}$	APM81911KNJSR	-	$\pm 5$	$\pm 6.5$	$\% f_{OSC}$
		APM81911KNJSR-1	-	0	-	$\% f_{OSC}$
PWM Dither Modulation Frequency	$f_{DITH(FREQ)}$		-	$\pm 0.5$	-	$\% f_{OSC}$
<b>PULSE-WIDTH MODULATION (PWM) TIMING AND CONTROL</b>						
Minimum SW On-Time	$t_{ON(MIN)}$	$V_{IN} = 12 \text{ V}$ , $I_{OUT} = 0.7 \text{ A}$ , $V_{BOOT} - V_{SW} = 3.3 \text{ V}$	-	60	90	ns
Minimum SW Off-Time	$t_{OFF(MIN)}$	$V_{IN} = 12 \text{ V}$ , $I_{OUT} = 0.7 \text{ A}$	-	55	75	ns
COMP to SW Current Gain	$gm_{POWER}$		-	5.0	-	A/V
PWM Ramp Offset	$V_{PWM(OFFS)}$		-	650	-	mV
<b>LOW POWER (LP) MODE</b>						
LP Output Voltage Ripple [3][4]	$\Delta V_{OUT(LP)}$	LP Mode, $8 \text{ V} < V_{IN} < 16 \text{ V}$ , $C_{OUT} = 47 \mu\text{F}$	-	65	-	mV

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ELECTRICAL CHARACTERISTICS (continued): Valid at  $3.5 \text{ V} \leq V_{IN} \leq 36 \text{ V}$ ,  $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$ , unless otherwise noted

INTERNAL MOSFET PARAMETERS							
High-Side On Resistance	$R_{DS(ON)HS}$	$T_J = 25^\circ\text{C}$ [3], $V_{BOOT} - V_{SW} = 3.3 \text{ V}$ , $I_{DS} = 1 \text{ A}$	–	115	140	–	$\text{m}\Omega$
		$T_J = 150^\circ\text{C}$ , $V_{BOOT} - V_{SW} = 3.3 \text{ V}$ , $I_{DS} = 1 \text{ A}$	–	–	230	–	$\text{m}\Omega$
Low-Side On Resistance	$R_{DS(ON)LS}$	$T_J = 25^\circ\text{C}$ [3], $V_{IN} \geq 4.5 \text{ V}$ , $I_{DS} = 1 \text{ A}$	–	85	115	–	$\text{m}\Omega$
		$T_J = 150^\circ\text{C}$ , $V_{IN} \geq 4.5 \text{ V}$ , $I_{DS} = 1 \text{ A}$	–	–	195	–	$\text{m}\Omega$
High-Side Leakage Current [3]	$I_{LKG(HS)}$	$T_J = 25^\circ\text{C}$ , $V_{IN} = 12 \text{ V}$ , $V_{EN} = 0 \text{ V}$ , $V_{SW} = 0 \text{ V}$	–	–	3.5	–	$\mu\text{A}$
Low-Side Leakage Current [3]	$I_{LKG(LS)}$	$T_J = 25^\circ\text{C}$ , $V_{IN} = 12 \text{ V}$ , $V_{EN} = 0 \text{ V}$ , $V_{SW} = 12 \text{ V}$	–	–	1.5	–	$\mu\text{A}$
Gate Drive Non-Overlap Time [3]	$t_{NO}$	$V_{BOOT} - V_{SW} = 3.3 \text{ V}$	–	1.5	4	–	$\text{ns}$
Switch Node Rising Slew Rate	$SR_{HS}$	$12 \text{ V} < V_{IN} < 16 \text{ V}$ , $V_{BOOT} - V_{SW} = 3.3 \text{ V}$	–	7	–	–	$\text{V/ns}$
MOSFET CURRENT PROTECTION THRESHOLDS							
High-Side Current Limit	$I_{LIM(HS)}$	$t_{ON} = t_{ON(MIN)}$	4.0	4.5	5.0	–	A
Low-Side Negative Current Limit	$I_{LIM(LS)}$		–	2.0	–	–	A
SYNCHRONIZATION INPUT (SYNC <sub>IN</sub> PIN)							
Synchronization Frequency Range	$f_{SW(SYNC)}$		1	–	2.5	–	MHz
SYNC <sub>IN</sub> Duty Cycle	$DC_{SYNC}$		20	50	70	–	%
SYNC <sub>IN</sub> Pulse-Width	$t_{PW(SYNC)}$		80	–	–	–	$\text{ns}$
SYNC <sub>IN</sub> Voltage Thresholds	$V_{SYNC(HI)}$	$V_{SYNC(IN)}$ rising	–	1.35	1.5	–	V
	$V_{SYNC(LO)}$	$V_{SYNC(IN)}$ falling	0.8	1.2	–	–	V
SYNC <sub>IN</sub> Hysteresis	$V_{SYNC(HYS)}$	$V_{SYNC(HI)} - V_{SYNC(LO)}$	–	150	–	–	$\text{mV}$
SYNC <sub>IN</sub> Pin Current	$I_{SYNC}$	$V_{SYNC(IN)} = 5 \text{ V}$	–	1	–	–	$\mu\text{A}$
CLOCK OUTPUT (CLK <sub>OUT</sub> PIN)							
SYNC <sub>IN</sub> to CLK <sub>OUT</sub> Delay	$\Phi_{SYNC(CLK)}$	$R_{FSET} = 14.3 \text{ k}\Omega$ , $V_{SYNC(HI)} = 3.3 \text{ V}$	–	$1/(2f_{OSC}) \pm 70$	–	–	$\text{ns}$
CLK <sub>OUT</sub> Output Voltage	$V_{CLK(OUT,H)}$	$V_{CC} = 3.3 \text{ V}$	2.2	–	–	–	V
	$V_{CLK(OUT,L)}$	$V_{CC} = 3.3 \text{ V}$	–	–	0.6	–	V
ERROR AMPLIFIER (COMP PIN)							
Feedback Input Bias Current [1]	$I_{FB}$	$V_{FB} = 800 \text{ mV}$	–50	–	–10	–	$\text{nA}$
Open Loop Voltage Gain	$AV_{OL}$		–	60	–	–	$\text{dB}$
Transconductance	$g_m$	$V_{FB} > 400 \text{ mV}$	500	750	1000	–	$\mu\text{A/V}$
		$0 \text{ V} < V_{FB} < 400 \text{ mV}$	270	400	540	–	$\mu\text{A/V}$
Output Current	$I_{EA}$		–	$\pm 75$	–	–	$\mu\text{A}$
COMP Pull-Down Resistance	$R_{COMP}$	FAULT = 1 or HICCUP = 1	–	1	–	–	$\text{k}\Omega$

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ELECTRICAL CHARACTERISTICS (continued): Valid at  $3.5 \text{ V} \leq V_{IN} \leq 36 \text{ V}$ ,  $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$ , unless otherwise noted

SOFT-START (SS PIN)						
Startup (Source) Current	$I_{SS}$	$HICCUP = FAULT = 0$	-30	-20	-10	$\mu\text{A}$
Hiccup (Sink) Current	$I_{HIC}$	$HICCUP = 1$	1	2.2	5	$\mu\text{A}$
Soft-Start Delay Time [3]	$t_{dSS}$	$C_{SS} = 22 \text{ nF}$	-	440	-	$\mu\text{s}$
Soft-Start Ramp Time [3]	$t_{SS}$	$C_{SS} = 22 \text{ nF}$	-	880	-	$\mu\text{s}$
FAULT/HICCUP Reset Voltage	$V_{SS(RST)}$	$V_{SS}$ falling due to HICCUP or FAULT	-	200	275	$\text{mV}$
Hiccup OCP (and LP) Counter Enable Threshold	$V_{HIC/LP(EN)}$	$V_{SS}$ rising	-	2.3	-	$\text{V}$
Soft-Start Frequency Foldback	$f_{SW(ss)}$	0 V < $V_{FB}$ < 100 mV	-	$f_{OSC}/8$	-	$\text{kHz}$
		100 mV < $V_{FB}$ < 200 mV	-	$f_{OSC}/4$	-	$\text{kHz}$
		200 mV < $V_{FB}$ < 400 mV	-	$f_{OSC}/2$	-	$\text{kHz}$
		400 mV < $V_{FB}$	-	$f_{OSC}$	-	$\text{kHz}$
Maximum Voltage	$V_{SS(MAX)}$	$V_{EN} = 0 \text{ V}$ or FAULT without HICCUP	-	$V_{CC}$	-	$\text{V}$
Pull-Down Resistance	$R_{SS(FLT)}$		-	2	-	$\text{k}\Omega$
HICCUP MODE COUNTS						
High-Side Overcurrent Count	$HIC_{OC}$	After $V_{SS} > V_{HIC/LP(EN)}$	-	120	-	$f_{OSC}$ counts
SW Short-to-Ground Count	$HIC_{SW(GND)}$		-	3	-	$f_{OSC}$ counts
BOOT Short-Circuit Count	$HIC_{BOOT(SC)}$		-	120	-	$f_{OSC}$ counts
BOOT Open-Circuit Count [3]	$HIC_{BOOT(OC)}$		-	7	-	$f_{OSC}$ counts
OUTPUT VOLTAGE PROTECTION THRESHOLDS ( $V_{FB}$ , OV, UV)						
VFB OV PWM Threshold	$V_{FB(OV)}$	$V_{FB}$ rising	840	860	880	$\text{mV}$
VFB OV PWM Hysteresis	$V_{FB(OV,HYS)}$	$V_{FB}$ falling, relative to $V_{FB(OV)}$	-	10	-	$\text{mV}$
VFB UV PWM Threshold	$V_{FB(UV)}$	$V_{FB}$ falling	710	740	770	$\text{mV}$
VFB UV PWM Hysteresis	$V_{FB(UV,HYS)}$	$V_{FB}$ rising, relative to $V_{FB(UV)}$	-	10	-	$\text{mV}$
VFB UV LP Mode Threshold [3]	$V_{FB(UV,LP)}$	$V_{FB}$ falling	665	700	735	$\text{mV}$
POWER GOOD OUTPUT (PGOOD PIN)						
PGOOD Startup (SU) Delay	$t_{dPG(SU)}$	Increasing $V_{FB}$ due to startup	-	30	-	$\mu\text{s}$
PGOOD Undervoltage (UV) Delay	$t_{dPG(UV)}$	Decreasing $V_{FB}$	80	120	-	$\mu\text{s}$
PGOOD Overvoltage (OV) Delay	$t_{dPG(OV)}$	After overvoltage event	-	240	-	$f_{OSC}$ cycles
PGOOD Low Output Voltage	$V_{PG(L)}$	$I_{PGOOD} = 5 \text{ mA}$	-	200	400	$\text{mV}$
PGOOD Leakage [1]	$I_{PG(LKG)}$	$V_{PGOOD} = 5.5 \text{ V}$	-	-	2	$\mu\text{A}$
PWM/AUTO INPUT						
PWM/AUTO High Threshold	$V_{HI(PWM)}$	$V_{PWM/AUTO}$ rising	1.8	2.0	2.5	$\text{V}$
PWM/AUTO Low Threshold	$V_{LO(PWM)}$	$V_{PWM/AUTO}$ falling	0.6	0.8	1.0	$\text{V}$
PWM to LP Transition Delay [3]	$t_{dPWM(LP)}$	PWM/AUTO low, $V_{SS} > V_{HIC/LP(EN)}$ , PGOOD high	-	7.5	-	$\text{ms}$

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ELECTRICAL CHARACTERISTICS (continued): Valid at  $3.5 \text{ V} \leq V_{IN} \leq 36 \text{ V}$ ,  $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$ , unless otherwise noted

ENABLE VOLTAGE INPUT (EN PIN)						
EN High Threshold	$V_{EN(HI)}$	$V_{EN}$ rising	1.15	-	1.35	V
EN Input Hysteresis	$V_{EN(HYS)}$	$V_{EN(HI)} - V_{EN(LO)}$	200	300	400	mV
Disable Delay	DISDLY	$V_{EN}$ transitions low to when SW stops switching	-	120	-	$f_{OSC}$ cycles
EN Pin Input Current	$I_{EN}$	$V_{EN} = 5 \text{ V}$	-	2	-	$\mu\text{A}$
BOOT REGULATOR (BOOT PIN)						
BOOT Charging Frequency	$f_{BOOT}$		-	$f_{OSC}$	-	kHz
BOOT Voltage	$V_{BOOT}$	$V_{IN} = 12 \text{ V}$ , $V_{BIAS} = 0 \text{ V}$ , $V_{BOOT} - V_{SW}$	-	3.3	3.6	V
INTERNAL REGULATOR (VCC PIN)						
BIAS Disconnected	$V_{CC1}$	$6 \text{ V} < V_{IN} < 36 \text{ V}$ , $V_{BIAS} = 0 \text{ V}$	3.25	3.45	3.65	V
BIAS Connected	$V_{CC2}$	$V_{BIAS} = 3.3 \text{ V}$	2.85	3.2	3.29	V
		$6 \text{ V} < V_{BIAS} < 36 \text{ V}$	3	3.35	3.75	V
BIAS Input Voltage Range	$V_{BIAS}$		3.15	-	36	V
BIAS OVERVOLTAGE PROTECTION (BIAS PIN)						
BIAS Overvoltage Protection	$V_{BIASOV(FBLO)}$	$V_{FB} \leq 200 \text{ mV}$	-	-	7.5	V
	$V_{BIASOV(FBHI)}$	$V_{FB} = 800 \text{ mV}$	24.6	-	27.5	V
THERMAL SHUTDOWN						
Thermal Shutdown Threshold <sup>[3]</sup>	$T_{SD}$	$T_J$ rising, PWM stops immediately and COMP and SS are pulled low	155	170	-	$^\circ\text{C}$
Thermal Shutdown Hysteresis <sup>[3]</sup>	$T_{SD(HYS)}$	$T_J$ falling, relative to $T_{SD}$	-	20	-	$^\circ\text{C}$

[1] Negative current is defined as coming out of the node or pin, positive current is defined as going into the node or pin.

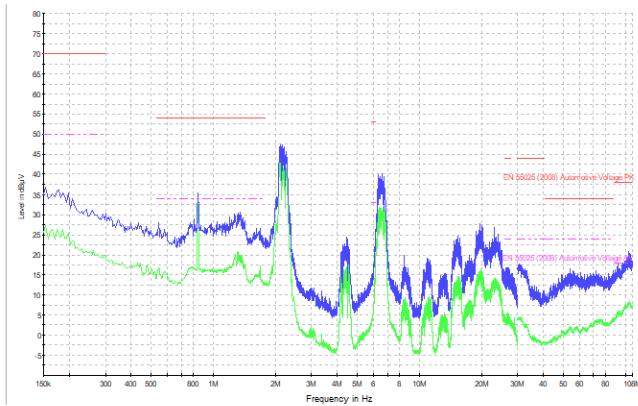
[2] Thermally limited depending on input voltage, duty cycle, regulator load currents, PCB layout, and airflow.

[3] Ensured by design and characterization, not production tested.

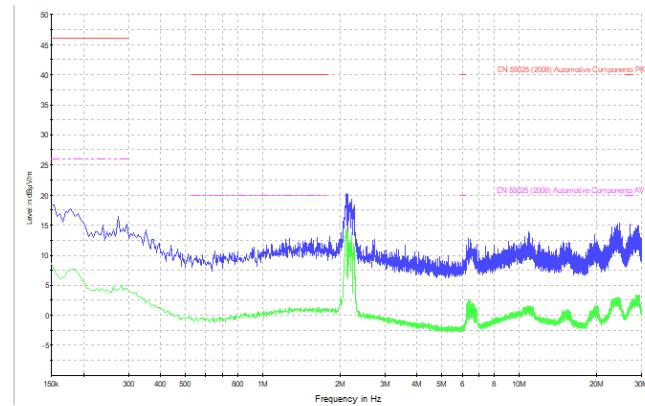
[4] Must use component values shown in Table 3, Recommended External Component Values.

### EMI/EMC PERFORMANCE CHARACTERISTICS

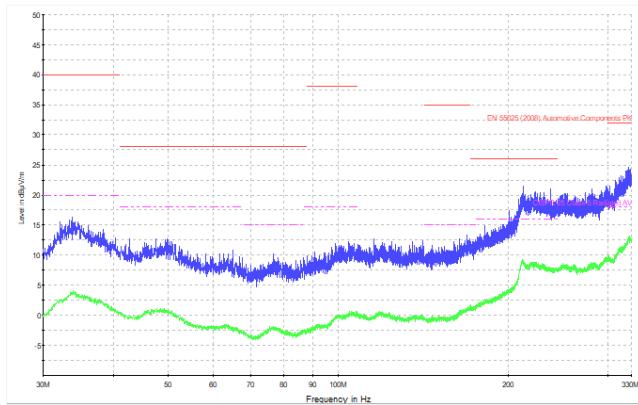
$V_{IN} = 12$  V,  $V_{OUT} = 5$  V,  $f_{SW} = 2.15$  MHz



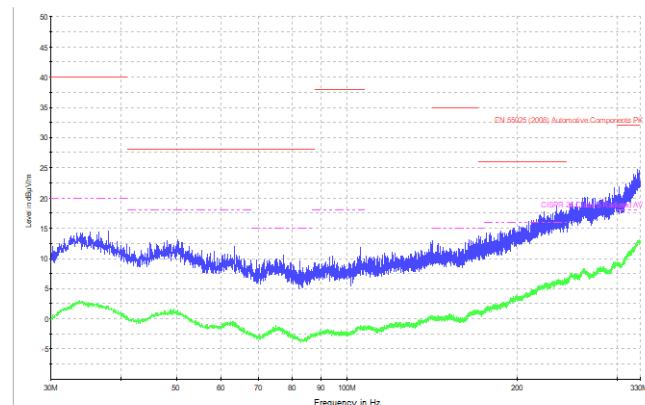
Conducted Emissions (150 kHz to 30 MHz)



Radiated Emissions (150 kHz to 30 MHz) (Monopole)



Radiated Emissions (30 MHz to 330 MHz)  
(Horizontal Biconical)



Radiated Emissions (30 MHz to 330 MHz)  
(Vertical Biconical)

NOTE: Allegro is not an accredited EMC laboratory. The information presented here is for reference only.

## FUNCTIONAL DESCRIPTION

## Overview

The APM81911 is a wide input voltage (3.5 to 36 V) synchronous PWM buck regulator that integrates low  $R_{DS(on)}$  high-side and low-side N-channel MOSFETs. A low DCR inductor and two capacitors (VIN capacitor and BOOT capacitor) are also integrated in the APM81911's compact 4 mm × 6 mm × 2.1 mm package. The APM81911 employs peak current mode control to provide superior line and load regulation, cycle-by-cycle current limit, fast transient response, and simple compensation. The features of the APM81911 include ultra-low  $I_Q$  LP mode, extremely low minimum on-time, maximized duty cycle for low dropout operation, and pre-bias startup capability.

Protection features of the APM81911 include  $V_{IN}$  undervoltage lockout, cycle-by-cycle overcurrent protection, BOOT overvoltage and undervoltage protection, hiccup mode short-circuit protection, overvoltage protection, and thermal shutdown. In addition, the APM81911 provides open-circuit, adjacent pin short-circuit, and pin-to-ground short-circuit protection.

## Reference Voltage

The APM81911 incorporates an internal precision reference that allows output voltages as low as 0.8 V. The accuracy of the internal reference is  $\pm 1.5\%$  across  $-40^\circ\text{C}$  to  $150^\circ\text{C}$ . The output voltage of the regulator is programmed with a resistor divider between  $V_{OUT}$  and the FB pin of the APM81911.

Internal  $V_{CC}$  Regulator

$V_{CC}$  is used as power supply for internal control circuitry and low-side MOSFET driver. APM81911 consists of two internal low dropout regulators,  $V_{IN}$  LDO and  $V_{BIAS}$  LDO, to generate  $V_{CC}$  voltage.  $V_{IN}$  LDO is powered from the input voltage to generate 3.5 V for  $V_{CC}$  supply during power up, soft-start and PWM mode.  $V_{BIAS}$  LDO uses the  $V_{BIAS}$  pin, connected to  $V_{OUT}$ , as a supply to generate  $V_{CC}$  voltage in LP mode to reduce current consumption from  $V_{IN}$ .

## Oscillator/Switching Frequency

The PWM switching frequency of the APM81911 is adjustable from 1 MHz to 2.4 MHz by programming the internal clock frequency of the oscillator by connecting an FSET resistor from the FSET pin to GND. The internal clock has an accuracy of about  $\pm 10\%$  over the operating temperature range. Usually, an FSET resistor with  $\pm 1\%$  tolerance is recommended. A graph of switching frequency versus FSET resistor value is shown in the PWM Switching Frequency ( $R_{FSET}$ ) section. The APM81911 will suspend operation if the FSET pin is shorted to GND or left open.

Synchronization ( $SYNC_{IN}$ ) and Clock Output ( $CLK_{OUT}$ )

The Phase-Locked Loop (PLL) in the APM81911 allows its internal oscillator to be synchronized to an external clock applied on the  $SYNC_{IN}$  pin. If the  $SYNC_{IN}$  pin is driven by an external clock, the APM81911 will be forced to operate in PWM mode, with synchronized switching frequency, overriding the mode selection on the PWM/AUTO pin. The external clock must satisfy the pulse-width, duty cycle, and rise/fall time requirements shown in the Electrical Characteristics table. If the  $SYNC_{IN}$  pin is continuously pulled high, the APM81911 outputs a 180-degree phase-shifted internal oscillator clock on the  $CLK_{OUT}$  pin, so “downstream” APM81911 devices can be easily interleaved via their synchronization inputs. Figure 5 shows the usage of multiple APM81911 devices in master-follower configuration. If the  $SYNC_{IN}$  pin is continuously pulled low, the device disables the  $CLK_{OUT}$  pin. The internal switching frequency dithering can be disabled by pulling the  $CLK_{OUT}$  pin high on APM81911 devices or by using the APM81911-1.

## Transconductance Error Amplifier

The transconductance error amplifier's primary function is to control the regulator's output voltage. The error amplifier is a three-terminal input device with two positive inputs and one negative input, as shown in Figure 4. The negative input is simply connected to the FB pin and is used to sense the feedback voltage for regulation. The error amplifier performs an “analog OR” selection between its positive inputs and operates according to the positive input with the lowest potential. The two positive inputs are used for soft-start and steady-state regulation. The error amplifier regulates to the soft-start pin voltage minus 400 mV during startup and to the internal reference ( $V_{REF}$ ) during normal operation.

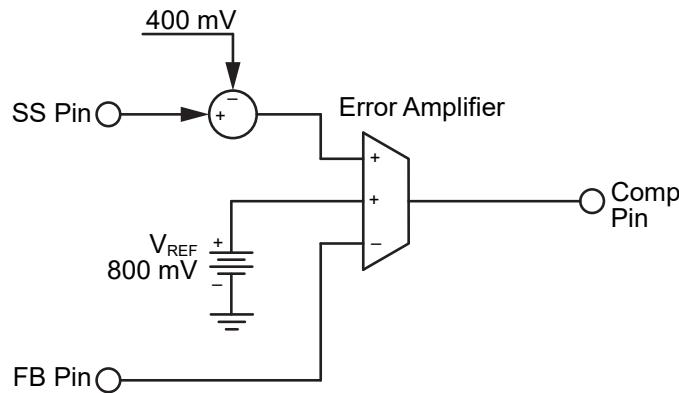


Figure 4: APM81911 Error Amplifier

### Ultra-Low Quiescent Current Low Power (LP) Mode

The APM81911 operates in ultra-low  $I_Q$  LP mode when PWM/AUTO pin is pulled to logic low. If the PWM/AUTO pin transitions from logic high to logic low while output is in regulation, the device waits for 7 clock cycles before entering the LP mode. This delay provides adequate filtering to ensure no noise transients forces the device to erroneously enter LP mode.

When LP mode is selected, the APM81911 operates in continuous conduction PWM Mode until peak inductor current decreases to  $I_{PEAK(LP)}$ . When peak inductor current falls below  $I_{PEAK(LP)}$ , the LP comparator monitors FB node and regulates the output voltage in hysteretic manner. The reference for the LP comparator is calibrated approximately 0.5% above the PWM regulation point. The transition point from PWM to LP mode is defined by the input voltage, output voltage and inductor value.

When voltage on the COMP pin falls to the voltage corresponding to the ultra-low  $I_Q$  peak current threshold value, an internal clamp prevents the COMP voltage from falling further. This results in a momentary rise in the FB voltage beyond the LP comparator upper threshold which causes the LP comparator to trip. Once the LP comparator trips, the device enters a coast period during which MOSFET switching is terminated and the associated control circuitry is also shut down. This ensures a very low quiescent current is drawn from the input.

The coast period terminates once the FB voltage falls below the LP comparator lower threshold. The device will fully power-up after approximately a 2.5  $\mu$ s delay and the high-side MOSFET is repeatedly turned on, operating at the PWM switching frequency until the voltage at the FB pin rises again above the LP comparator threshold. The rate of rise of output voltage is determined by the input voltage, output voltage, inductor value, output capacitance, and load.

### Dropout

The APM81911 is designed to operate at extremely wide duty cycles to minimize any reduction in output voltage during dropout conditions such as cold crank (where the input voltage drops to a certain value).

### Power MOSFETs

The APM81911 includes a 115 m $\Omega$  (typ), high-side N-channel MOSFET and a 85 m $\Omega$  (typ), low-side N-channel MOSFET to provide synchronous rectification. When the APM81911 is disabled via the EN input being low or a fault condition, its output stage is tri-stated by turning off both the high-side and low-side MOSFETs.

### Integrated Passive Components

The APM81911 module integrates a high-performance DC-DC regulator IC, a low DCR inductor, and two ceramic capacitors in a compact 4 mm  $\times$  6 mm  $\times$  2.1 mm package:

- Inductor = 1.5  $\mu$ H  $\pm$ 20% at 1 MHz, DCR= 52 m $\Omega$
- VIN capacitor ( $C_{VIN}$ ) = 47 nF
- BOOT capacitor ( $C_{BOOT}$ ) = 47 nF

The bootstrap capacitor is connected between the BOOT and SW pins to provide floating gate drive to the high-side MOSFET, while the VIN capacitor is used to bypass high di/dt input ripple current, minimizing the EMI.

### Soft-Start (Startup) and Inrush Current Control

The soft-start function controls the inrush current at startup. The soft-start pin (SS) is connected to GND via a capacitor. When the APM81911 is enabled and all faults are cleared, the SS pin sources the charging current  $I_{SS}$  and the voltage on the soft-start capacitor  $C_{SS}$  starts ramping upward from 0 V. When the voltage at the soft-start pin exceeds the soft-start offset voltage (SS Offset), typically 400 mV, the error amplifier will ramp up its output voltage above the PWM Ramp Offset. At this instant, the top and bottom MOSFETs will begin switching. There is a small delay ( $t_{dSS}$ ) from the moment EN pin transitions high to the moment soft-start voltage reaches 400 mV to initiate PWM switching.

Immediately after the start of PWM switching, the error amplifier will regulate the voltage at the FB pin to the soft-start pin voltage minus approximately 400 mV. During the active portion of soft-start, the voltage at the SS pin will rise from 400 mV to 1.2 V (a difference of 800 mV), the voltage at the FB pin will rise from 0 V to 800 mV, and the regulator output voltage will rise from 0 V to the set voltage determined by the feedback resistor divider.

During startup, PWM switching frequency is reduced to 25% of  $f_{SW}$  while FB is below 200 mV. If FB voltage is above 200 mV but below 400 mV, the switching frequency is 50% of  $f_{SW}$ . At the same time, the transconductance of the error amplifier,  $g_m$ , is reduced to half of nominal value when FB is below 400 mV. When FB is above 400 mV, the switching frequency will be  $f_{SW}$  and the error amplifier gain will be the nominal value. The reduced switching frequency and error amplifier gain are necessary to help improve output regulation and stability when  $V_{OUT}$  is very low. During low  $V_{OUT}$ , the PWM control loop requires on-time near the minimum controllable on-time and very low duty cycles that are not possible at the nominal switching frequency.

When the voltage at the soft-start pin reaches approximately 1.2 V, the error amplifier will switch over and begin regulating

the voltage at the FB pin to the fixed internal bandgap reference voltage of 800 mV. The voltage at the soft-start pin will continue to rise to the internal LDO regulator output voltage. If the APM81911 is disabled or a fault occurs, the internal fault latch is set and the capacitor at the SS pin is discharged to ground very quickly through a 2 k $\Omega$  pull-down resistor. The device will clear the internal fault latch when the voltage at the SS pin decays to approximately 200 mV. However, if the device enters hiccup mode, the capacitor at the SS pin is slowly discharged through a current sink,  $I_{HIC}$ . Therefore, the soft-start capacitor  $C_{SS}$  not only controls the startup time but also the time between soft-start attempts in hiccup mode.

### Pre-Biased Startup

If the output of the buck regulator is pre-biased at a certain output voltage level, the APM81911 will modify the normal startup routine to prevent discharging the output capacitors. As described in the Soft-Start (Startup) and Inrush Current Control section, the error amplifier usually becomes active when the voltage at the soft-start pin exceeds 400 mV. If the output is pre-biased, the voltage at the FB pin will be non-zero. The device will not start switching until the voltage at SS pin rises to approximately  $V_{FB} + 400$  mV. From then on, the error amplifier becomes active, the voltage at the COMP pin rises, PWM switching starts, and  $V_{OUT}$  will ramp upward from the pre-bias level.

### PGOOD Output

The APM81911 provides a Power Good (PGOOD) status signal to indicate if the output voltage is within the regulation limits. Since the PGOOD output is an open-drain output, an external pull-up resistor must be used as shown in the applications schematic. PGOOD transitions high when the output voltage, sensed at the FB pin, is within regulation.

During startup, the PGOOD signal exhibits an additional delay of  $t_{dPG(SU)}$  after FB pin voltage reaches the regulation voltage. This delay helps to filter out any glitches on the FB pin voltage.

The PGOOD output is pulled low if either an undervoltage or overvoltage condition occurs or the APM81911 junction temperature exceeds thermal shutdown threshold ( $T_{SD}$ ). The PGOOD overvoltage and undervoltage comparators incorporate a small amount of hysteresis ( $V_{FB(OV,HYS)}$ ),  $V_{FB(UV,HYS)}$ ) to prevent chattering and deglitch filtering ( $t_{dPG(UV)}$ ,  $t_{dPG(OV)}$ ) to eliminate false triggering. For other faults, PGOOD depends on the output voltage.

It is important that the correct status of PGOOD is reported during either the input supply ramp up or ramp down. During a supply ramp up, the PGOOD is designed to operate in the correct state from a very low input voltage. Also, during supply ramp

down, the PGOOD is designed to operate in the correct state down to a very low input voltage.

### Current Sense Amplifier

The APM81911 incorporates a high-bandwidth current sense amplifier to monitor the current through the top MOSFET. This current signal is used to regulate the peak current when the top MOSFET is turned on. The current signal is also used by the protection circuitry for the cycle-by-cycle current limit and hiccup mode short-circuit protection.

### Pulse-Width Modulation (PWM)

The APM81911 employs fixed-frequency, peak current mode control to provide excellent load and line regulation, fast transient response, and simple compensation. A high-speed comparator and control logic are included in the APM81911. The inverting input of the PWM comparator is connected to the output of the error amplifier. The non-inverting input is connected to the sum of the current sense signal, the slope compensation signal, and a DC PWM Ramp offset voltage (Ramp Offset).

At the beginning of each PWM cycle, the CLK signal sets the PWM flip flop, the bottom MOSFET is turned off, the top MOSFET is turned on, and the inductor current increases. When the voltage at the non-inverting input of the PWM comparator rises above the error amplifier output COMP, the PWM flip flop is reset, the top MOSFET is turned off, the bottom MOSFET is turned on, and the inductor current decreases. Since the PWM flip flop is reset, the dominant error amplifier may override the CLK signal in certain situations.

### Frequency Dither

In addition to EMI-aware PCB layout, extensive filtering, controlled switch node transitions, and shielding, switching frequency dithering is an effective way to mitigate EMI concerns in switching power supplies. Frequency dither helps to minimize peak emissions by spreading the emissions across a wide range of frequencies. The APM81911 provides frequency dither by spreading the switching frequency  $\pm 5\%$  using a triangular modulated wave of 0.5% switching frequency (see Table 1: PWM Frequency, CLK<sub>OUT</sub>, and Dithering Settings)

The APM81911 can add dither to the external clock applied on the SYNC pin. This unique feature allows the minimizing of electromagnetic emissions even when the device is using external clock.

With a factory trim option, there is the possibility to disable the frequency dither scheme. This option could be used in master-follower configuration to avoid double-dithering.

Table 1: PWM Frequency,  $CLK_{OUT}$ , and Dithering Settings

Device	SYNC <sub>IN</sub>	PWM Frequency and Dithering			CLK <sub>OUT</sub> Frequency and Dithering		
		SW Frequency	Dither Frequency Range	Dither Modulation Frequency	Frequency	Dither Frequency Range	Dither Modulation Frequency
APM81911KNBATTR	Low	$f_{OSC}$	$\pm 0.05 \times f_{OSC}$	$\pm 0.005 \times f_{OSC}$	Disabled/Off	None	None
	High	$f_{OSC}$			$f_{OSC} + 180^\circ$	$\pm 0.05 \times f_{OSC}$	$\pm 0.005 \times f_{OSC}$
	$f_{SYNC}$	$f_{SYNC}$			$f_{SYNC} + 180^\circ$	$\pm 0.05 \times f_{OSC}$	$\pm 0.005 \times f_{OSC}$
APM81911KNBATTR-1	Low	$f_{OSC}$	Dither Disabled	$\pm 0.05 \times f_{OSC}$	Disabled/Off	Dither Disabled	$\pm 0.005 \times f_{OSC}$
	High	$f_{OSC}$			$f_{OSC} + 180^\circ$		
	$f_{SYNC}$	$f_{SYNC}$			$f_{SYNC} + 180^\circ$		
APM81911KNBATTR with CLKOUT pulled to VCC	Low	$f_{OSC}$	Dither Disabled	$\pm 0.05 \times f_{OSC}$	None	None	None
	High	$f_{OSC}$					
	$f_{SYNC}$	$f_{SYNC}$					

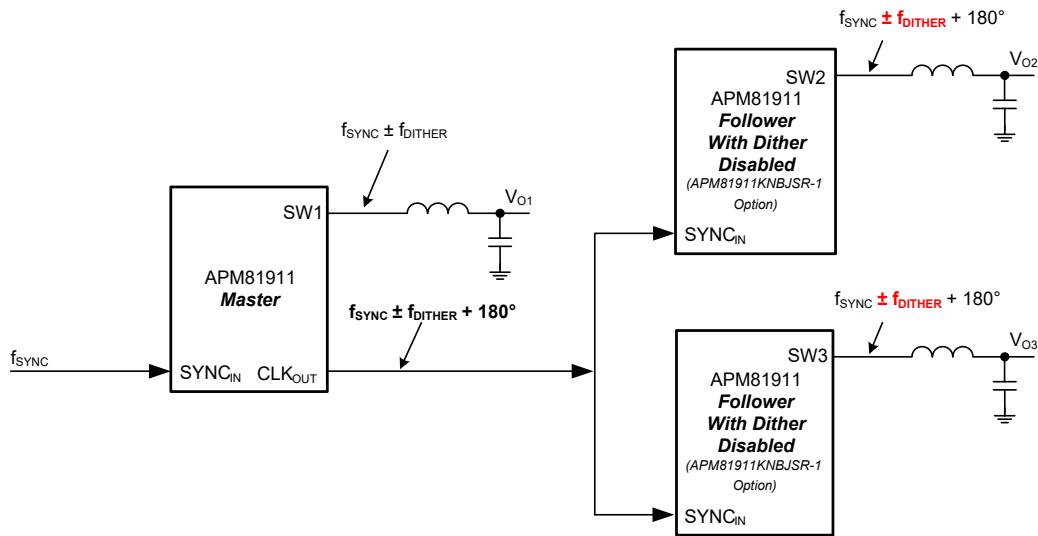


Figure 5: Master-Follower Configuration with APM81911KNBATTR-1 Option

Follower devices can be APM81911-1, or APM81911 with CLKOUT tied to VCC

## PROTECTION FEATURES

The APM81911 was designed to satisfy the most demanding automotive and non-automotive applications. In this section, a description of each protection feature is described and Table 2 summarizes the protections and their operation.

**Undervoltage Lockout (UVLO)**

An undervoltage lockout (UVLO) comparator in the APM81911 monitors the voltage at the VIN pin and keeps the regulator disabled if the voltage is below the start threshold ( $V_{UVLO(ON)}$ ,  $V_{IN}$  rising) or the stop threshold ( $V_{UVLO(OFF)}$ ,  $V_{IN}$  falling). The UVLO comparator incorporates some hysteresis ( $V_{UVLO(HYS)}$ ) to help prevent on-off cycling of the regulator due to resistive or inductive drops in the  $V_{IN}$  path during heavy loading or during startup.

**Pulse-by-Pulse Peak Current Protection (PCP)**

The APM81911 monitors the current in the high-side MOSFET, and if the peak MOSFET current exceeds the pulse-by-pulse overcurrent limit  $I_{LIM(HS)}$ , the upper MOSFET is turned off and the bottom MOSFET is turned on until the start of the next clock pulse from the oscillator. The device includes leading edge blanking to prevent false triggering of pulse-by-pulse current protection when the upper MOSFET is turned on.

**Overcurrent Protection (OCP) and Hiccup Mode**

An OCP counter and hiccup mode circuit protect the buck regulator when the output of the regulator is shorted to ground or when the load is too high. When the soft-start ramp is active ( $t < t_{SS}$ ), the OCP hiccup counter is disabled. The following two conditions must be met for the OCP counter to be enabled and begin counting:

- SS pin voltage,  $V_{SS} > V_{HIC/LP(EN)}$  (2.3 V), and
- COMP pin voltage,  $V_{COMP}$  clamped at its maximum voltage.

As long as these two conditions are met, the OCP counter remains enabled and will count pulses from the overcurrent comparator. If the COMP voltage decreases ( $OCP = 0$ ), the OCP counter is cleared. Otherwise, if the OCP counter reaches 120 clock counts, PWM switching ceases, a hiccup latch is set, and the COMP pin is quickly pulled down by a relatively low resistance (1 k $\Omega$ ). The hiccup latch

also enables a small current sink connected to the SS pin ( $I_{HIC}$ ). This causes the voltage at the soft-start pin to slowly ramp downward. When the voltage at the soft-start pin decays to a low enough level ( $V_{SS(RST)}$ , 200 mV), the hiccup latch is cleared, and the current sink is turned off. At this instant, the SS pin will begin to source current ( $I_{SS}$ ) and the voltage at the SS pin will ramp upward.

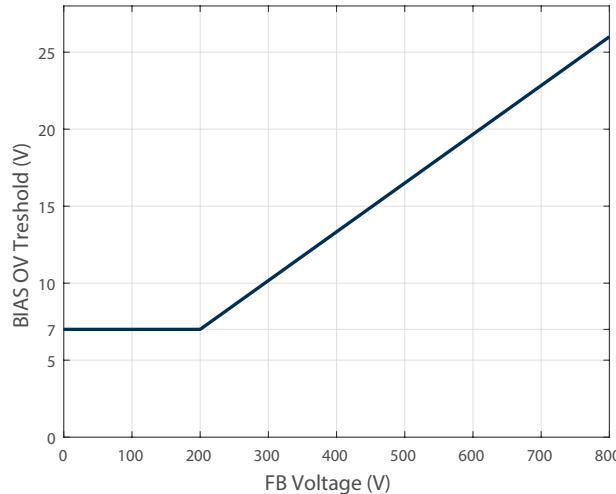
This marks the beginning of a new, normal soft-start cycle as described earlier. When the voltage at the soft-start pin exceeds the error amp voltage by approximately 400 mV, the error amplifier will force the voltage at the COMP pin to quickly slew upward and PWM switching will resume.

If the short circuit/overload at the regulator output persists, another hiccup cycle will occur. Hiccups will repeat until the short circuit/overload is removed or the converter is disabled. If the short circuit/overload is removed, the device will soft-start normally and the output voltage will automatically recover to the desired level. Thus, hiccup mode is a very effective protection for the short-circuit/overload condition. It avoids false trigger during short duration short-circuit/overload. On the other hand, for the extended short-circuit/overload duration, the reduced average power dissipation with hiccup mode of operation helps in lowering the temperature rise of the device and enhancing the system reliability.

Note that OCP is the only fault that results in hiccup mode being ignored while  $V_{SS} < 2.3$  V.

**Bias Overvoltage Monitoring**

The APM81911 includes an always-on overvoltage protection circuit on the BIAS pin that monitors for an output overvoltage condition. This circuit allows for overvoltage protection even when the connection to FB is lost or shorted to ground. The BIAS overvoltage threshold adjusts with the voltage at FB, decreasing the overvoltage threshold in events such as when FB is shorted to ground. During an overvoltage event the controller tries to reduce the output overvoltage by terminating the high-side MOSFET switching and pulsing the low side MOSFET with minimum off-time ( $t_{OFF(min)}$ ) until FB returns to regulation. The APM81911 waits for  $t_{dPG(OV)}$  (240 clock cycles) before pulling the PGOOD low. The device returns to regulation when the fault condition is removed.



**Figure 6: BIAS Overvoltage Threshold vs. FB Pin Voltage**

### SW Pin Protection

Unlike most regulators, the APM81911 protects itself when the SW pin is shorted to ground. If the SW pin is shorted to ground, there will be a very high current in the high-side MOSFET when it is turned on. The APM81911 incorporates an internal secondary current protection to detect this unusually high current and turns off the high-side MOSFET if the high current persists for more than two consecutive switching cycles. After turning off the high-

side MOSFET, the device enables the hiccup latch and attempts to restart after hiccup latch is cleared. If the short to ground is removed, the regulator will automatically recover; otherwise, the device continues hiccupping. Unlike other hiccup mode protections, the SW pin protection is not delayed until soft-start is completed, i.e.,  $V_{SS} > 2.3$  V.

### Pin-to-Ground and Pin-to-Pin Short Protections

The APM81911 is designed to satisfy the most demanding automotive applications. For example, the device has been carefully designed to withstand a short circuit to ground at each pin without causing any damage to the IC.

In addition, care was taken when defining the device pinouts to optimize protection against pin-to-pin adjacent short circuits. For example, logic pins and high-voltage pins are separated as much as possible. Inevitably, some low-voltage pins are located adjacent to high voltage pins, but in these instances, the low-voltage pins are designed to withstand increased voltages, with clamps and/or series input resistance, to prevent damage to the device.

### Thermal Shutdown ( $T_{SD}$ )

The APM81911 monitors internal junction temperature and shuts down the IC by disabling the switching pulses of high- and low-side MOSFETs if the junction temperature exceeds the Thermal Shutdown Threshold  $T_{SD}$ . Also, to prepare for a restart, the internal soft-start voltage ( $V_{SS}$ ) and the voltage at the COMP pin are pulled low until  $V_{SS} < V_{SS(RST)}$ .  $T_{SD}$  is a non-latched fault, so the device automatically recovers.

**Table 2: Summary of APM81911 Fault Modes and Operation**

Fault Mode	Hiccup	High Side MOSFET	Low-Side MOSFET	PGOOD	Reset Condition
$V_{IN}$ Undervoltage	NO	Off	Off	Low	$V_{IN}$ above UVLO
Output Short / Overcurrent	YES after 120 pulses	Off	Turned On if BOOT Voltage is too low	Low	Short / Overcurrent removed
SW short to GND (HS OCP)	YES after 2 pulses	Off	Off	Low	Short removed
Output Overvoltage	NO	Off	Pulsed with Minimum $t_{OFF}$	Low	$V_{OUT}$ within operative range
Output Undervoltage	NO		Switching with Minimum $t_{OFF}$	Low	$V_{OUT}$ within operative range
FSET shorted to GND	NO	Off	Off	Low	FSET short removed
Thermal Shutdown	NO	Off	Off	Low	Part cools down

## APPLICATION INFORMATION

PWM Switching Frequency ( $R_{FSET}$ )

The PWM switching frequency is set by connecting a resistor from the FSET pin to signal ground. Figure 7 shows the relationship between the typical switching frequency (y-axis) and the FSET resistor (x-axis). For a required switching frequency ( $f_{SW}$ ), the FSET resistor value can be calculated as follows:

Equation 1:

$$R_{FSET} = \frac{37037}{f_{SW}} - 2.96$$

where  $f_{SW}$  is in kHz and  $R_{FSET}$  is in k $\Omega$ .

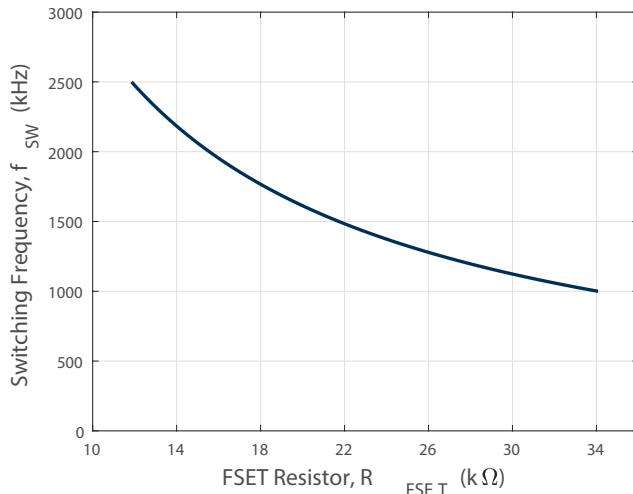


Figure 7: PWM Switching Frequency vs.  $R_{FSET}$

## Power Switch Minimum On-Time

While choosing the PWM switching frequency, the designer should be aware of the minimum controllable on-time,  $t_{ON(MIN)}$ , of the APM81911. If the required on-time of the system is less than the minimum controllable on-time, pulse skipping will occur and the output voltage will have increased ripple. The PWM switching frequency should be calculated using Equation 2, where  $V_{OUT}$  is the output voltage,  $t_{ON(MIN)}$  is the minimum controllable on-time of the device (see Electrical Characteristics table), and  $V_{IN(MAX)}$  is the maximum required operational input voltage (not the peak surge voltage).

Equation 2:

$$f_{SW} < \frac{V_{OUT}}{t_{ON(MIN)} \times V_{IN(MAX)}}$$

If an external clock  $f_{SYNC}$  is used for synchronization, the base switching frequency should be chosen such that pulse skipping will not occur at the maximum synchronized switching frequency (i.e.,  $1.5 \times f_{SYNC}$  should be less than the frequency  $f_{SW}$  in Equation 2).

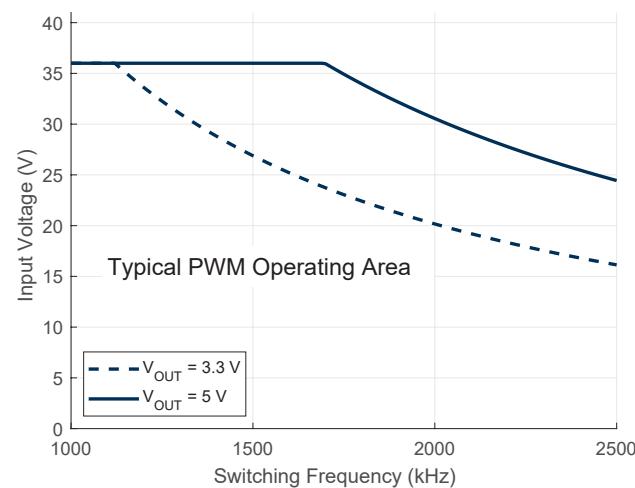


Figure 8: Input Voltage Limit To Prevent Pulse Skipping  
Output Voltage Setting

The output voltage of the APM81911 is determined by connecting a resistive feedback divider ( $R_{FB1}$ ,  $R_{FB2}$ ) from the output node ( $V_{OUT}$ ) to the FB pin as shown in Figure 7. The feedback resistors must satisfy the ratio shown in Equation 3 to produce the desired output voltage ( $V_{OUT}$ ).

Equation 3:

$$\frac{R_{FB1}}{R_{FB2}} = \frac{V_{OUT}}{0.8} - 1.0$$

1% resistors are recommended to maintain the output voltage accuracy. There are tradeoffs while choosing the value of the feedback resistors. If the series combination ( $R_{FB1} + R_{FB2}$ ) is too low, the light load efficiency of the regulator will be reduced. So, to maximize the efficiency, it is best to choose large values for feedback resistors. On the other hand, large values of feedback resistors increase the parallel combination ( $R_{FB1} \parallel R_{FB2}$ ) and makes the regulator more susceptible to noise coupling onto the FB pin.

The FB pin leakage current also has an impact on the output voltage accuracy of the regulator. A small amount of leakage current,

$I_{FB}$ , flowing into the FB pin increases the output voltage beyond the set regulation voltage. The output voltage of the regulator accounting for the FB pin leakage current is given by:

Equation 4:

$$V_{OUT} = V_{FB} \times \left( 1 + \frac{R_{FB1}}{R_{FB2}} \right) + I_{FB} \times R_{FB1}$$

## Output Capacitors ( $C_O$ )

The output capacitor of switching regulators filter the output voltage to provide an acceptable level of ripple on the output voltage, and they also store energy to help maintain voltage regulation during a load transient. The voltage rating of the output capacitors must support the output voltage with sufficient design margin.

The output voltage ripple ( $\Delta V_{OUT}$ ) is a function of the output capacitor parameters:  $C_O$ ,  $ESR_{CO}$ , and  $ESL_{CO}$ :

Equation 5:

$$\Delta V_{OUT} = \Delta I_{LO} \times ESR_{CO} + \frac{V_{IN} - V_{OUT}}{L_0} \times ESL_{CO} + \frac{\Delta I_{LO}}{8 \times f_{SW} \times C_0}$$

The type of output capacitors determines which terms of Equation 5 are dominant. For ceramic output capacitors,  $ESR_{CO}$  and  $ESL_{CO}$  are virtually zero, so the output voltage ripple will be dominated by the third term of Equation 5. The value of  $C_O$  can be calculated as:

Equation 6:

$$C_O \geq \frac{\Delta I_{LO}}{8 \times f_{SW} \times \Delta V_{OUT}}$$

Voltage ripple of a regulator using ceramic output capacitors can be reduced by increasing the total capacitance, reducing the inductor current ripple, or increasing the switching frequency. For electrolytic output capacitors, the value of capacitance will be relatively high, so the third term in Equation 5 will be very small and the output voltage ripple will be determined primarily by the first two terms:

Equation 7:

$$\Delta V_{OUT} = \Delta I_{LO} \times ESR_{CO} + \frac{V_{IN} - V_{OUT}}{L_0} \times ESL_{CO}$$

Voltage ripple of a regulator using electrolytic output capacitors can be reduced by decreasing the equivalent  $ESR_{CO}$  and  $ESL_{CO}$  by using a high-quality capacitor, adding more capacitors in parallel, or reducing the inductor current ripple.

As the ESR of some electrolytic capacitors can be quite high, Allegro recommends choosing a quality capacitor for which

the ESR or the total impedance is clearly documented in the capacitor datasheet. Also, ESR of electrolytic capacitors usually increases significantly at cold ambient temperatures, as much as 10 times, which increases the output voltage ripple and, in most cases, reduces the stability of the system.

The transient response of the regulator depends on the quantity and type of output capacitors. In general, minimizing the ESR of the output capacitance will result in a better transient response. The ESR can be minimized by simply adding more capacitors in parallel or by using higher quality capacitors. At the instant of a fast load transient (high  $di_O/dt$ ), the change in the output voltage, using electrolytic output capacitors, is:

Equation 8:

$$\Delta V_{OUT} = \Delta I_{LO} \times ESR_{CO} + \frac{di_O}{dt} \times ESL_{CO}$$

When ceramic capacitors are used in the output, the output voltage deviation during load transients depends on the bulk output capacitance along with various other factors. To calculate the bulk ceramic capacitance required, the entire load transient duration can be divided into two stages: large signal and small signal. During large signal load transients, immediately after the transient event, the output voltage deviates from the nominal value due to large mismatch in the load current requirement and the inductor current. The output voltage deviation during this interval is maximum and depends on output inductor, bulk output capacitance, and closed-loop crossover frequency. For designs with higher crossover frequency, the controller typically saturates the duty cycle, i.e., either minimum or maximum. For a chosen output inductor and crossover frequency values, the output voltage deviation can be minimized by increasing the output bulk capacitance. In the case of a buck converter, operating with a low duty cycle, the step-down load transient is more severe and hence the output capacitance should be determined for this scenario. The bulk ceramic output capacitance required is given by:

Equation 9:

$$C_{O(\text{bulk})} = \frac{\Delta I_O^2 \times L_0}{2 \times V_{OUT} \times \Delta V_{OUT(\text{spec})}}$$

where  $\Delta I_O$  is the magnitude of the change in the load current,  $\Delta V_{OUT(\text{spec})}$  is the maximum allowed output voltage deviation during load transient event. Gradually, as the mismatch between the load current and the inductor current becomes small, the output voltage deviation also reduces, resembling a small signal transient event. Eventually, during small signal transient interval, the error amplifier brings the output voltage back to its nominal value. The speed with which the error amplifier brings the output voltage back into regulation depends mainly on the loop cross-

over frequency. A higher crossover frequency usually results in a shorter time to return to the nominal set voltage.

### Output Voltage Ripple – Ultra-Low $I_Q$ LP Mode

After choosing output capacitor(s), it is important to calculate the output voltage ripple ( $V_{PP(LP)}$ ) during ultra-low  $I_Q$  LP mode. With ceramic output capacitors, the output voltage ripple in PWM mode is usually negligible, but this is not the case during LP mode.

In LP mode, the peak inductor current during on-time of the high-side switch is limited to  $I_{PEAK(LP)}$ . Also, in LP mode, the low-side switch is constantly turned off thereby forcing the regulator to operate in Discontinuous Conduction Mode (DCM) in order to reduce switching losses. A LP comparator monitors the output voltage on the internal feedback node and allows the regulator to switch until the internal feedback voltage is 0.5% greater than its nominal value (0.8 V). When internal feedback voltage is greater than 0.804 V, the APM81911 coasts by terminating the switching pulses.

During coasting, device shuts down most of its internal control circuitry to ensure very low quiescent current is drawn from the input. The number of switching pulses, in LP mode, required to coast the device depends on various factors including input voltage, output voltage, load current, output inductor and output capacitor. If APM81911 starts coasting after a single switching pulse, then the output voltage ripple would be dictated by this single pulse. The peak inductor current ( $I_{PEAK_L}$ ) is given by:

Equation 10:

$$I_{PEAK_L} = \frac{I_{PEAK(LP)}}{1 + \frac{S_E \times L_0}{V_{IN} - V_{OUT}}}$$

where  $I_{PEAK(LP)}$  is the peak inductor current, specified in the Electrical Characteristics table, at which device enters LP mode. Referring to Figure 49, on-time and off-time calculations are given as:

Equation 11:

$$t_{ON} = \frac{I_{PEAK_L} \times L_0}{V_{IN} - V_{OUT} - I_{PEAK_L} \times (R_{DS(ON)HS} + L_{O(DCR)})}$$

Equation 12:

$$t_{OFF} = \frac{I_{PEAK_L} \times L_0}{V_{OUT}}$$

where  $R_{DS(ON)HS}$  is the on-resistance of internal high-side MOSFET and  $L_{O(DCR)}$  is the DC resistance of the output inductor,  $L_0$ .

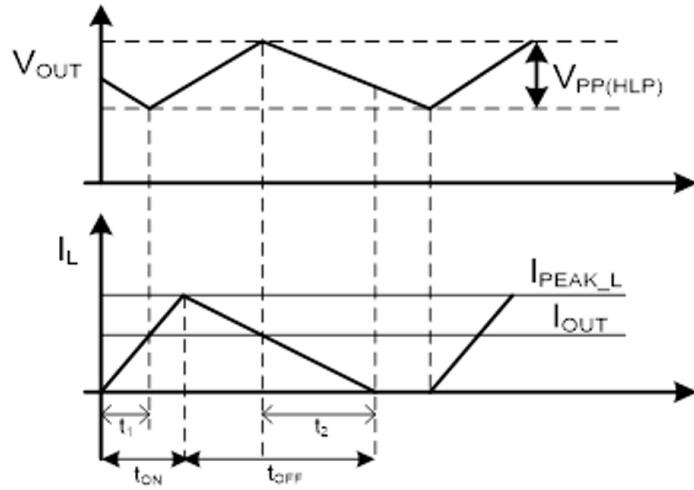


Figure 9: Output Voltage Ripple in LP Mode

During on-time interval, the length of the time for the inductor current to rise from 0 A to  $I_{OUT}$  is:

Equation 13:

$$t_1 = \frac{I_{OUT} \times L_0}{V_{IN} - V_{OUT} - I_{PEAK_L} \times (R_{DS(ON)HS} + L_{O(DCR)})}$$

During off-time interval, the length of the time for the inductor current to fall from  $I_{OUT}$  to 0 A is:

Equation 14:

$$t_2 = \frac{I_{OUT} \times L_0}{V_{OUT}}$$

Given the peak inductor current ( $I_{PEAK_L}$ ) and the rise and fall times ( $t_{ON}$  and  $t_{OFF}$ ) for the inductor current, the output voltage ripple for a single switching pulse can be calculated as follows:

Equation 15:

$$V_{PP(LP)} = \frac{I_{PEAK_L} - I_{OUT}}{2 \times C_{OUT}} \times (t_{ON} + t_{OFF} - t_1 - t_2)$$

### Input Capacitors

Three factors should be considered when choosing the input capacitors. First, the capacitors must be chosen to support the maximum expected input surge voltage with adequate design margin. Second, the capacitor RMS current rating must be higher than the expected RMS input current to the regulator. Third, the capacitors must have enough capacitance and a low enough ESR to limit the input voltage  $dV/dt$  to much less than the hysteresis of the UVLO circuitry (250 mV nominal) at maximum loading

and minimum input voltage. The input capacitors must deliver an RMS current ( $I_{RMS}$ ) given by:

Equation 16:

$$I_{RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

where D is the duty cycle

Equation 17:

$$D \approx \frac{V_{OUT}}{V_{IN}}$$

Figure 1010 shows the normalized input capacitor RMS current versus duty cycle. To use this graph, simply find the operational duty cycle (D) on the x-axis and determine the input/output current multiplier on the y-axis. For example, at a 20% duty cycle, the input/output current multiplier is 0.40. Therefore, if the regulator is delivering 1.0 A of steady-state load current, the input capacitor(s) must support  $0.40 \times 1.0$  A or 0.4 A RMS.

The input capacitor(s) must limit the voltage deviations at the  $V_{IN}$  pin to significantly less than the device UVLO hysteresis during maximum load and minimum input voltage condition. The following equation allows to calculate the minimum input capacitance required:

Equation 18:

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1 - D)}{0.85 \times f_{SW} \times \Delta V_{IN(MIN)}}$$

where  $\Delta V_{IN(MIN)}$  is chosen to be much less than the hysteresis of the  $V_{IN}$  UVLO comparator ( $\Delta V_{IN(MIN)} \leq 150$  mV is recommended), and  $f_{SW}$  is the nominal PWM frequency. The  $D \times (1 - D)$  term in Equation 18 has an absolute maximum value of 0.25 at 50% duty cycle.

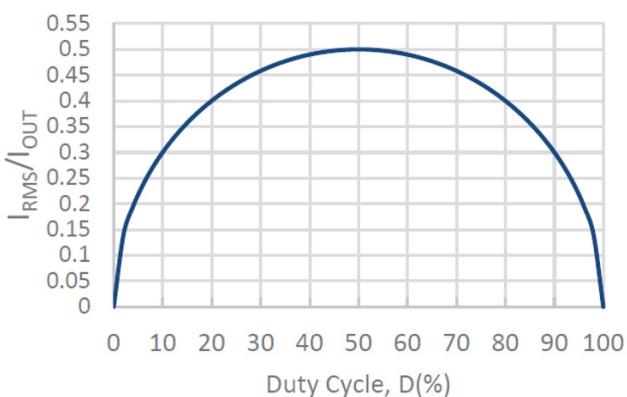


Figure 10: Normalized Input Capacitor Ripple versus Duty Cycle

A good design should consider the DC bias effect on a ceramic capacitor: as the applied voltage approaches the rated value, the capacitance value decreases. This effect is very pronounced with the Y5V and Z5U temperature characteristic devices (as much as 90% reduction), so these types should be avoided. The X5R, X7R, and X8R type capacitors should be the primary choices due to their stability versus both DC bias and temperature.

The APM81911 integrates a 47 nF X8R input capacitor. In addition to the recommended ceramic input capacitance and 47 nF integrated ceramic capacitor, an aluminum electrolytic capacitor of at least 47  $\mu$ F is recommended at the input to help dampen transient events. The electrolytic capacitor is used to meet load-transient response requirements and to avoid input voltage oscillation due to the negative input impedance of the DC-DC regulator. While the integrated ceramic capacitor is used to bypass high di/dt input ripple current.

### Soft-Start and Hiccup Mode Timing ( $C_{SS}$ )

The soft-start time of the APM81911 is determined by the value of the capacitance ( $C_{SS}$ ) at the soft-start pin. When the APM81911 is enabled, the SS pin sources the charging current  $I_{SS}$ , and the voltage across the soft-start capacitor  $C_{SS}$  starts ramping upward from 0 V. PWM switching will begin after the voltage across  $C_{SS}$  exceeds 400 mV. The soft-start delay ( $t_{dSS}$ ) can be calculated using the following equation:

Equation 19:

$$t_{dSS} = 0.4 \times \left( \frac{C_{SS}}{I_{SS}} \right)$$

If the device is starting with a very heavy load, a very fast soft-start time may cause the regulator to exceed the pulse-by-pulse overcurrent threshold. This occurs because the sum of the full load current, the inductor ripple current, and the additional current required to charge the output capacitors,

Equation 20:

$$I_{CO} = C_0 \times \frac{V_{OUT}}{t_{SS}},$$

is higher than the pulse-by-pulse current threshold. This phenomenon is more pronounced when using high value electrolytic-type output capacitors. To avoid prematurely triggering hiccup mode, the soft-start capacitor ( $C_{SS}$ ) should be calculated according to equation below:

Equation 21:

$$C_{SS} \geq \frac{I_{SS} \times V_{OUT} \times C_0}{0.8 \times I_{CO}}$$

where  $V_{OUT}$  is the output voltage,  $C_0$  is the output capacitance,

$I_{CO}$  is the amount of current allowed to charge the output capacitance during soft-start ( $0.1 \text{ A} < I_{CO} < 0.3 \text{ A}$  is recommended). The soft-start time ( $t_{SS}$ ) can be calculated as below:

Equation 22:

$$t_{SS} = 0.8 \times \left( \frac{C_{SS}}{I_{SS}} \right)$$

Higher values of  $I_{CO}$  result in faster soft-start times. However, lower values of  $I_{CO}$  ensure that hiccup mode is not falsely triggered. Allegro recommends starting the design with an  $I_{CO}$  of 0.1 A and increasing it only if the soft-start time is too slow. If a non-standard capacitor value for  $C_{SS}$  is calculated, the next larger value should be used.

When the device is in hiccup mode, the soft-start capacitor is used as a timing capacitor and sets the hiccup period. The soft-start pin charges the soft-start capacitor with  $I_{SS}$  during a startup attempt and discharges the same capacitor with  $I_{HIC}$  between startup attempts. Because the ratio of  $I_{SS}/I_{HIC}$  is approximately 4:1, the time between hiccups will be about four times as long as the startup time. Therefore, the effective duty cycle will be very low, and the junction temperature will be kept low.

## Output Current Derating

The APM81911 output maximum current derates with increased ambient temperature. The figures below show the maximum output current over temperature using the APEK81911KNB-01-T evaluation board, with a large copper area for VOUT, 2 oz copper on the outer layers, and 1oz copper on the inner layers. Refer to the evaluation board user manual for more information about the evaluation board layout and performance.

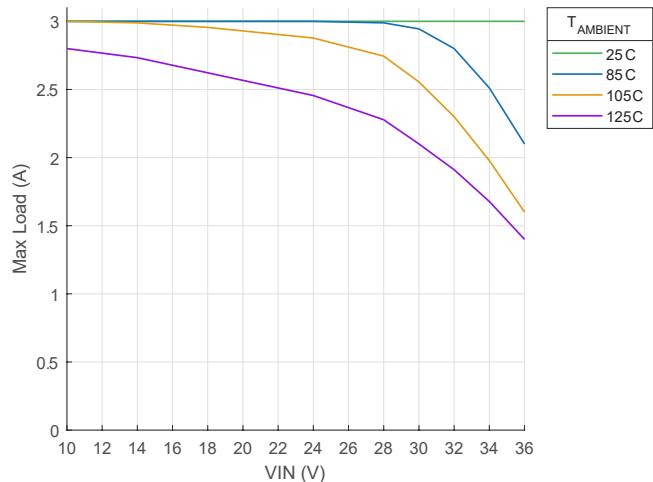


Figure 11: APM81911 Maximum Output Current Derating with  $V_{OUT} = 3.3 \text{ V}$ ,  $f_{sw} = 2.15 \text{ MHz}$

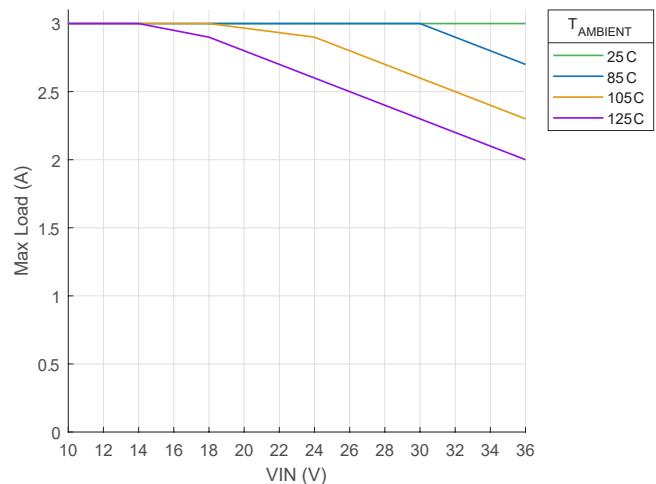


Figure 12: APM81911 Maximum Output Current Derating with  $V_{OUT} = 5 \text{ V}$ ,  $f_{sw} = 2.15 \text{ MHz}$

## Compensation Components ( $R_Z$ , $C_Z$ , $C_P$ , and $C_{FF}$ )

The objective of the selection of the compensation components is to ensure adequate stability margins to avoid instability issues, to maintain a high loop gain at DC to achieve excellent output voltage regulation, and to obtain a high loop bandwidth for superior transient response. To a first order, the closed-loop model of a peak current mode-controlled regulator can be broken into two blocks as shown in Figure 133.

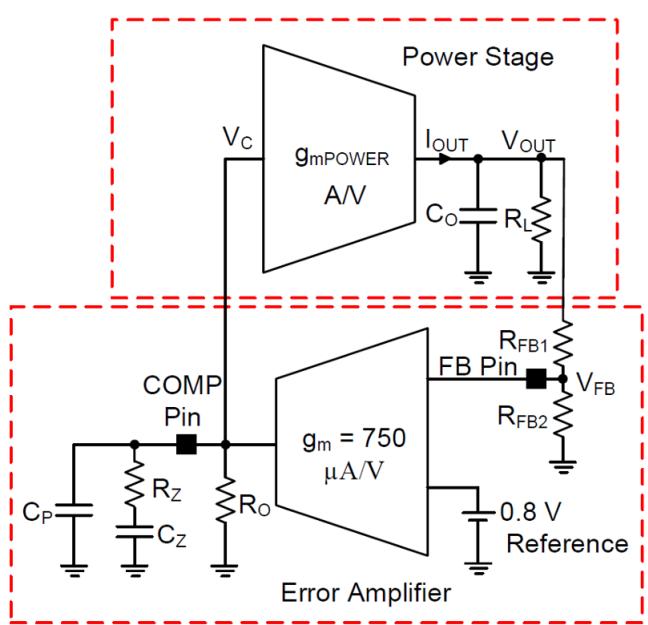


Figure 13: Power Stage and Error Amplifier

The power stage includes the output filter capacitor(s),  $C_O$ , the equivalent load,  $R_L$  and the inner current loop which consists of the PWM modulator and the integrated output inductor,  $L_O$ . The inner current loop, with a first-order approximation, can be effectively modelled as a trans-conductance amplifier which converts the control voltage ( $V_C$ ) from the error amplifier to a peak output inductor current with an equivalent gain  $g_{mPOWER}$ . Although, the peak current through the inductor is being controlled, neglecting the inductor ripple current, it is acceptable to replace it with output current  $I_{OUT}$ .

From a small-signal point of view, the current mode control loop behaves like a current source and therefore the power inductor can be ignored. The output capacitor integrates the ripple current through the inductor, effectively forming a single pole with the output load. A control-to-output transfer function between the control voltage ( $V_C$ ), output of the error amplifier in the feedback loop, and the regulator output voltage ( $V_{OUT}$ ) describes the dynamics of the power stage. The DC gain of the power stage, i.e., control-to-output transfer function, is given by

Equation 23:

$$G_{DC(CO)} = g_{mPOWER} \times R_L$$

where  $g_{mPOWER}$  is the equivalent gain of the inner current loop (specified in the Electrical Characteristics table) and  $R_L$  is the load resistance.

The control-to-output transfer function has a pole  $f_{P(CO)}$ , formed by the output capacitance ( $C_O$ ) and load resistance ( $R_L$ ), located at:

Equation 24:

$$f_{P(CO)} = \frac{1}{2 \times \pi \times R_L \times C_O}$$

The control-to-output transfer function has a zero  $f_{Z(CO)}$ , formed by the output capacitance ( $C_O$ ) and its associated ESR, located at:

Equation 25:

$$f_{Z(CO)} = \frac{1}{2 \times \pi \times ESR \times C_O}$$

For a design with very low-ESR type output capacitors (such as ceramic or OSCON output capacitors), the ESR zero,  $f_{Z(CO)}$ , is usually at a very high frequency so it can be ignored. On the other hand, with high-ESR electrolytic output capacitors, the ESR zero falls below or near the 0 dB crossover frequency of the closed loop, hence it should be cancelled by the pole formed by the  $C_P$  capacitor and the  $R_Z$  resistor discussed and identified later as  $f_{P2(EA)}$ .

A feedforward capacitor ( $C_{FF}$ ) can be connected in parallel with  $R_{FB1}$  to increase phase margin and loop crossover frequency for improving transient response of the regulator. The addition of  $C_{FF}$  results in an additional zero and pole in the compensation network and boosts the loop phase at the crossover frequency. In general,  $C_{FF}$  should be less than 25 pF. While large value of  $C_{FF}$  increases the loop crossover frequency and reduces the phase margin, very small value of  $C_{FF}$  will not have any effect. Optimal value of  $C_{FF}$  can be calculated from the following equation.

Equation 26:

$$C_{FF} = \frac{1}{2 \times \pi \times R_{FB1} \times f_C}$$

Figure 14: Feedback Divider with Feedforward Capacitor  
Error Amplifier

The error amplifier, as a part of the output voltage feedback loop, comprises a transconductance amplifier with an external Type-II compensation formed by  $R_Z$ - $C_Z$ - $C_P$  network. A Type-II compensated error amplifier introduces two poles and a zero. The placement of these poles and zero should be such that the closed-loop system has sufficient stability margins and high bandwidth (loop crossover frequency) and provides optimal transient response.

The DC gain of the feedback loop, including the error amplifier and the feedback resistor divider is given by:

Equation 27:

$$G_{DC(FB)} = A_{VOL} \times \frac{R_{FB2}}{R_{FB1} + R_{FB2}} = A_{VOL} \times \frac{V_{FB}}{V_{OUT}}$$

where  $A_{VOL}$  is the open-loop DC gain of the error amplifier (specified in the Electrical Characteristics table).

The DC gain of the error amplifier is 65 dB (equivalent to 1778) and with a gm value of 750  $\mu$ A/V, the effective output impedance,  $R_O$ , of the amplifier is:

Equation 28:

$$R_O = \frac{1778}{750 \times 10^{-6}} = 2.37 \text{ M}\Omega$$

Typically,  $R_O \gg R_Z$  and  $C_Z \gg C_P$ , which simplifies the derivation of the transfer function of the Type-II compensated error amplifier. The transfer function has a (very) low frequency pole  $f_{P1(EA)}$  dominated by the error amplifier output impedance  $R_O$  and the compensation capacitor  $C_Z$ :

Equation 29:

$$f_{P1(EA)} = \frac{1}{2 \times \pi \times R_O \times C_Z}$$

The transfer function of the Type-II compensated error amplifier also has a zero at frequency  $f_{Z(EA)}$  caused by the resistor  $R_Z$  and the capacitor  $C_Z$ :

Equation 30:

$$f_{Z(EA)} = \frac{1}{2 \times \pi \times R_Z \times C_Z}$$

Lastly, the transfer function of the Type-II compensated error amplifier has a (very) high frequency pole  $f_{P2(EA)}$  dominated by the resistor  $R_Z$  resistor and the capacitor  $C_P$ :

Equation 31:

$$f_{P2(EA)} = \frac{1}{2 \times \pi \times R_Z \times C_P}$$

Although there are many different approaches for designing the feedback loop, a good design approach attempts to maximize the closed-loop system stability, while providing a high bandwidth and optimized transient response. A generalized tuning procedure is presented below to systematically determine the values of compensation components ( $R_Z$ ,  $C_Z$ , and  $C_P$ ) in the feedback loop.

## A Generalized Tuning Procedure

**1. Choose the system bandwidth ( $f_C$ ).** This is the frequency at which the magnitude of the gain crosses 0 dB. Recommended values for  $f_C$ , based on the PWM switching frequency, are in

the range  $f_{SW}/20 < f_C < f_{SW}/10$ . A higher value of  $f_C$  generally provides a better transient response, while a lower value of  $f_C$  generally makes it easier to obtain higher gain and phase margins.

**2. Calculate the  $R_Z$  resistor value.** This sets the system bandwidth ( $f_C$ ):

Equation 32:

$$R_Z = f_C \times \frac{V_{OUT}}{V_{FB}} \times \frac{2 \times \pi \times C_0}{g_{mPOWER} \times g_m}$$

**3. Calculate the range of values for the  $C_Z$  capacitor.** Use the following:

Equation 33:

$$\frac{4}{2 \times \pi \times R_Z \times f_C} < C_Z < \frac{14}{2 \times \pi \times R_Z \times 1.5 \times f_{P(CO)}}$$

To maximize system stability, i.e., high gain and phase margins, use a higher value of  $C_Z$ . To optimize transient recovery time, although at the expense of low stability margins, use a lower value of  $C_Z$ .

**4. Calculate the frequency of the ESR zero  $f_{Z(CO)}$  formed by the output capacitor(s) by using Equation 25 (repeated here):**

$$f_{Z(CO)} = \frac{1}{2 \times \pi \times ESR \times C_0}$$

If  $f_{Z(CO)}$  is at least one decade higher than the target crossover frequency  $f_C$ , then  $f_{Z(CO)}$  can be ignored. This is usually the case for a design using ceramic output capacitors. Use Equation 31 to calculate the value of  $C_P$  by setting  $f_{P2(EA)}$  to either  $5 \times f_C$  or  $f_{SW}/2$ , whichever is higher.

Alternatively, if  $f_{Z(CO)}$  is near or below the target crossover frequency  $f_C$ , then use Equation 31 to calculate the value of  $C_P$  by setting  $f_{P2(EA)}$  equal to  $f_{Z(CO)}$ . This is usually the case for a design using high ESR electrolytic output capacitors.

## APPLICATION SCHEMATIC AND RECOMMENDED EXTERNAL COMPONENTS

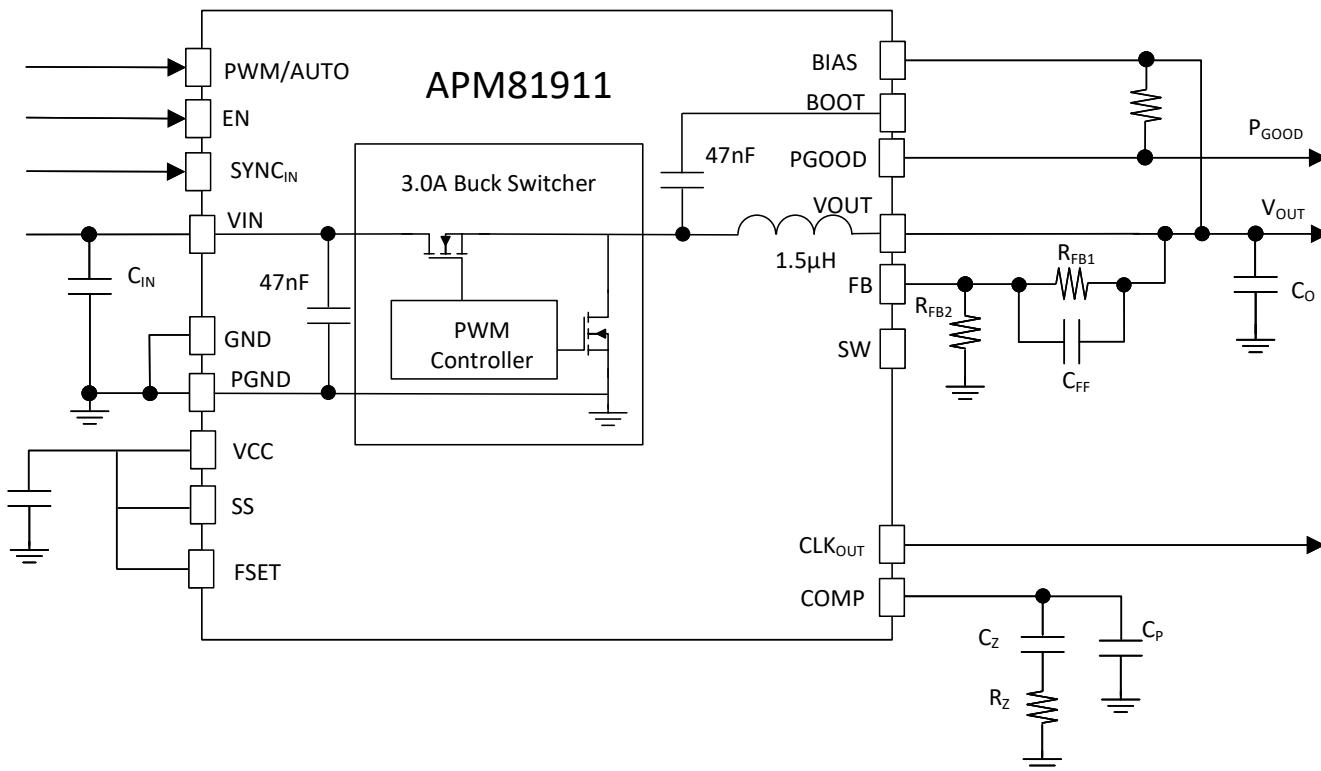


Figure 15: Applications Schematic showing component locations

Table 3: Recommended External Components Value

V <sub>OUT</sub>	f <sub>osc</sub>	C <sub>IN(MIN)</sub> <sup>[1]</sup>	C <sub>O</sub> <sup>[1]</sup>	COMP Components				FB Components	
				R <sub>Z</sub>	C <sub>Z</sub>	C <sub>P</sub>	C <sub>FF</sub>	R <sub>FB1</sub>	R <sub>FB2</sub>
5.0 V	2.15 MHz	7 $\mu$ F	24 $\mu$ F	13.3 k $\Omega$	1 nF	Not Mounted	10 pF	732 k $\Omega$	137 k $\Omega$
3.3 V	2.15 MHz	7 $\mu$ F	24 $\mu$ F	13.3 k $\Omega$	1 nF	Not Mounted	10 pF	301 k $\Omega$	95.3 k $\Omega$

<sup>[1]</sup> Input and output minimum capacitance values reflect total effective capacitance requirement over temperature and DC bias. Use high quality ceramic capacitors with an appropriate voltage and temperature rating to ensure sufficient total effective capacitance.

Note: These values are provided for reference. It is the responsibility of the customer to verify proper performance across all operating corners in the final application.

## POWER DISSIPATION AND THERMAL CALCULATIONS

The total power dissipated in the APM81911 is the sum of the power dissipated from the  $V_{IN}$  supply current ( $P_{IN}$ ), the power dissipated due to the switching of the high-side power MOSFET ( $P_{SWH}$ ), the power dissipated due to the conduction of rms current in the high-side MOSFET ( $P_{CH}$ ) and low-side MOSFET ( $P_{CL}$ ), power dissipated due to the low-side MOSFET body diode conduction during the non-overlap time ( $P_{NO}$ ) and the power dissipated by both high-side and low-side gate drivers ( $P_{DRIVER}$ ).

The power dissipated from the  $V_{IN}$  supply current (with BIAS pin open) can be calculated using Equation 34:

Equation 34:

$$P_{IN} = V_{IN} \times I_{IN(PWM)} + (V_{IN} - V_{GS}) \times f_{SW}$$

where  $V_{IN}$  is the input voltage,  $I_{IN(PWM)}$  is the input quiescent current drawn by the APM81911 in PWM mode (see Electrical Characteristics table),  $V_{GS}$  is the MOSFET gate drive voltage, and  $f_{SW}$  is the PWM switching frequency.

The power dissipated by the high-side MOSFET during PWM switching can be calculated using Equation 35:

Equation 35:

$$P_{SWH} = (V_{IN} \times I_{OUT} \times (t_r + t_f) \times f_{SW}) / 2$$

where  $V_{IN}$  is the input voltage,  $I_{OUT}$  is the regulator output current,  $f_{SW}$  is the PWM switching frequency,  $t_r$  and  $t_f$  are the rise and fall times measured at the switch node.

The exact rise and fall times at the SW node will depend on the external components and PCB layout, so each design should be measured at full load.

The power dissipated in the high-side MOSFET while it is conducting can be calculated using Equation 36:

Equation 36:

$$P_{CH} = I_{RMS(H)}^2 \times R_{DS(ON)H} = \left( \frac{V_{OUT}}{V_{IN}} \right) \times \left( I_{OUT}^2 \times \frac{\Delta I_{LO}^2}{12} \right) \times R_{DS(ON)H}$$

Similarly, the conduction losses dissipated in the low-side MOSFET while it is conducting can be calculated by the following equation:

Equation 37:

$$P_{CL} = I_{RMS(L)}^2 \times R_{DS(ON)L} = \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \times \left( I_{OUT}^2 \times \frac{\Delta I_{LO}^2}{12} \right) \times R_{DS(ON)L}$$

where  $I_{OUT}$  is the regulator output current,  $\Delta I_{LO}$  is the peak-to-peak inductor ripple current,  $R_{DS(ON)H}$  is the on-resistance of the high-side MOSFET,  $R_{DS(ON)L}$  is the on-resistance of the low-side MOSFET.

The power dissipated in the low-side MOSFET body diode during the non-overlap time can be calculated as follows:

Equation 38:

$$P_{NO} = V_{SD} \times I_{OUT} \times 2 \times t_{NO} \times f_{SW}$$

where  $V_{SD}$  is the source-to-drain voltage of the low-side MOSFET (typically 0.60 V), and  $t_{NO}$  is the non-overlap time.

The power dissipated in the internal gate drivers can be calculated using Equation 39:

Equation 39:

$$P_{DRIVER} = V_{GS} \times f_{SW}$$

where  $V_{GS}$  is the gate drive voltage.

Finally, the total power dissipated in the APM81911 is given by:

Equation 40:

$$P_{TOTAL} = P_{IN} + P_{SW} + P_{CH} + P_{CL} + P_{NO} + P_{DRIVER}$$

The average junction temperature ( $T_J$ ) can be calculated as follows.

Equation 41:

$$T_J = P_{TOTAL} \times R_{\theta JA} + T_A$$

where  $P_{TOTAL}$  is the total power dissipated from Equation 40,  $R_{\theta JA}$  is the junction-to-ambient thermal resistance (42°C/W on a 4-layer PCB), and  $T_A$  is the ambient temperature.

$R_{\theta JA}$  includes the thermal impedance from junction to case,  $R_{\theta JC}$  and the thermal impedance from case to ambient,  $R_{\theta CA}$ .  $R_{\theta CA}$  is generally determined by the amount of copper that is used underneath and around the device on the printed circuit board.

The maximum allowed power dissipation depends on how efficiently heat can be transferred from the junction to the ambient air, i.e., minimizing the  $R_{\theta JA}$ . As with any regulator, there are limits to the amount of heat that can be dissipated before risking thermal shutdown. There are tradeoffs between ambient operating temperature, input voltage, output voltage, output current, switching frequency, PCB thermal resistance, airflow, and other nearby heat sources. Even a small amount of airflow will reduce the junction temperature considerably.

## PCB LAYOUT GUIDELINES

The APM81911 is designed to minimize electromagnetic (EM) emissions when proper PCB layout techniques are adopted. A good PCB layout is also critical for the APM81911 to provide clean and stable output voltages. Design guidelines for EMI/EMC-aware PCB layout and minimum  $R_{0JA}$  are presented below. Figure 166 shows a typical application schematic of a synchronous buck regulator IC with critical power paths/loops.

- Place the ceramic input capacitors as close as possible to the VIN pin and PGND pins to make the loop area minimal, and the traces of the input capacitors to VIN pin should be short and wide to minimize the inductance. This critical loop is shown as trace 1 in Figure 166. The bulk/electrolytic input capacitor can be located further away from VIN pin. The input capacitors and APM81911 IC should be on the same side of the board with traces on the same layer.
- The loop from the input supply and capacitors, through the high-side MOSFET, into the output capacitor via the VOUT pins, and back to ground should be minimized with relatively wide traces.  
When the high-side MOSFET is off, free-wheeling current flows from ground, through the synchronous low-side MOSFET.
- Place the output capacitors relatively close to the output pins, VOUT. Ideally, the output capacitors and the APM81911 should be on the same layer. Connect the output capacitors with a fairly wide trace. The output capacitors must use a ground plane to make a very low-inductance connection to the PCB GND. These critical connections are shown as trace 2 in Figure 166.
- Compensation network must be as close as possible to GND and COMP pins.

- Voltage divider must be placed as close as possible to GND and FB pins in order to minimize the offset and gain error due to the parasitic resistance of the PCB traces.
- If a  $R_{FSET}$  resistor is used, place it as close as possible to the FSET pin.
- The output voltage sense trace should be routed as close as possible to the load to obtain the best load regulation.
- Allegro recommends a 4-layer PCB. Heavier copper layers, reduced material between layers and a good amount of thermal vias are the keys to improved thermal performance. Use TOP layer for routing high-current traces, layer 2 for a solid GND plane, layer 3 for most other routing, BOT layer for solid GND plane or optionally other components without low-impedance traces constraints—the PGOOD pull-up resistor could be on the BOT plane if desired.
- If a two-layer only (TOP and BOT) PCB is mandatory, place all the components on the TOP layer and limit the routing only to the top layer. Use BOT layer as GND plane.
- When connecting the input and output ceramic capacitors, use multiple vias to GND planes and place the vias as close as possible to the pads of the components. Do not use thermal reliefs around the pads for the input and output ceramic capacitors.
- To minimize thermal resistance ( $R_{0JA}$ ), extend ground planes on TOP layer as much as possible and use plenty of thermal vias to connect them to GND plane in BOT layer.
- To minimize PCB losses and improve system efficiency, the power traces should be as wide as possible.

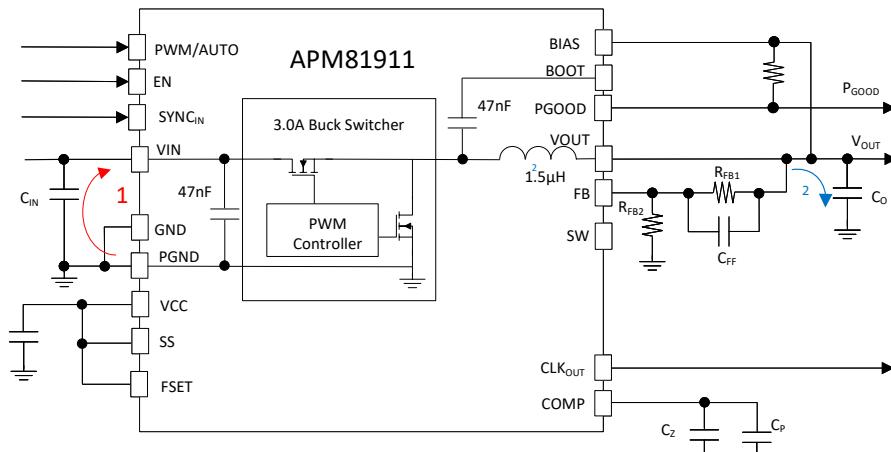


Figure 16: PCB Layout Critical Paths

## PACKAGE OUTLINE DRAWING AND RECOMMENDED PCB FOOTPRINT

## PRELIMINARY

For Reference Only; Not for Tooling Use  
(Reference DWG-0000753, Rev. 2, incl. Appendix APM81911)  
Dimensions in millimeters  
Exact case and lead configuration at supplier discretion within limits shown

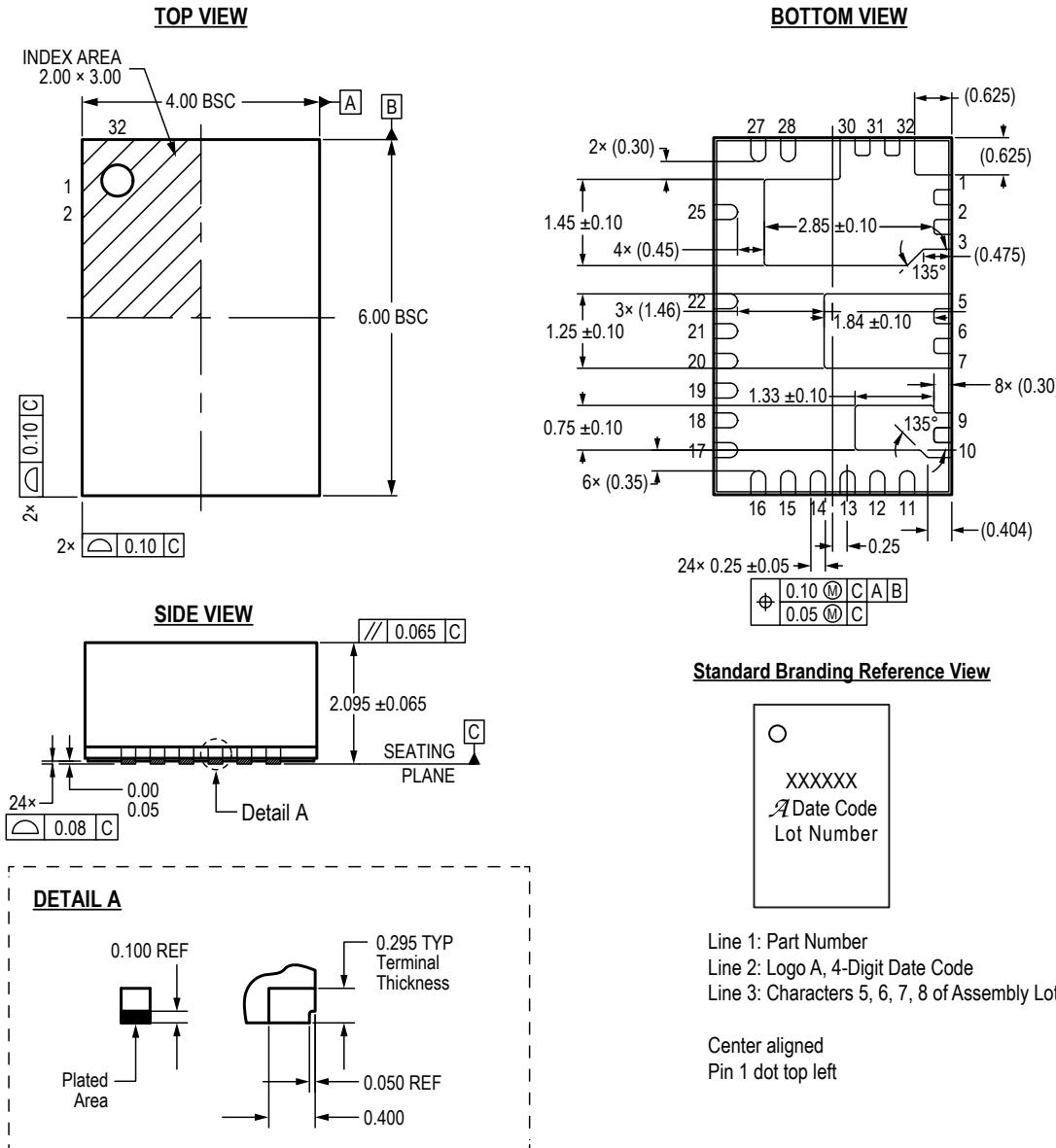


Figure 17: 32-Lead 4 mm x 6 mm QFN (Suffix NB)

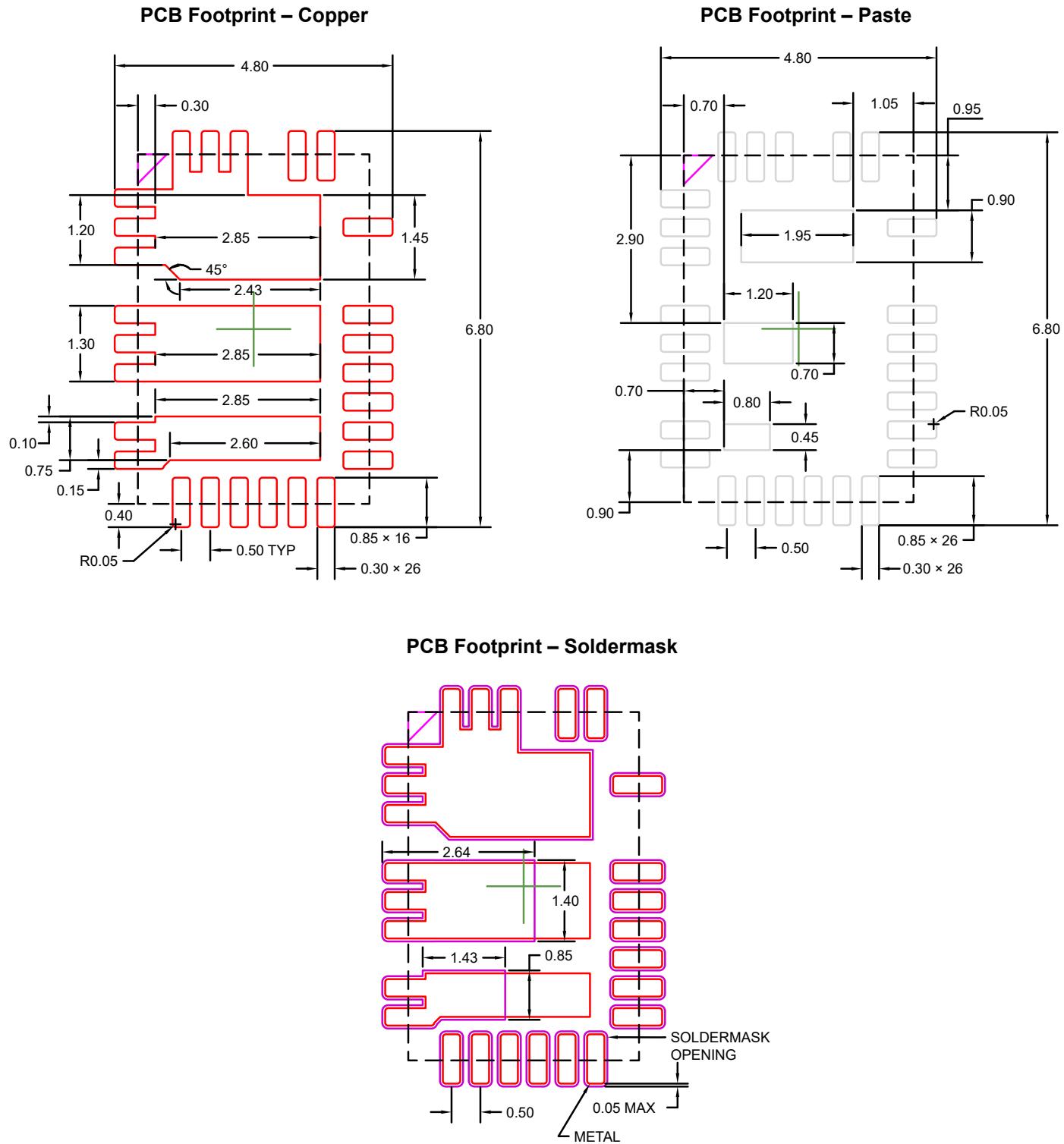


Figure 18: Recommended PCB Footprint

Altium and Cadence schematic and layout library files for the APM81911 are provided on the APM81911 product page on [Allegromicro.com](http://Allegromicro.com).

## Revision History

Number	Date	Description
–	February 23, 2023	Initial release
1	March 14, 2023	Updated Dropout Switching Frequency footnote in Characteristics table (page 5); updated test conditions of Bias Ovvoltage Protection in Electrical Characteristics table (page 8)
2	May 18, 2023	Updated package image (page 1)
3	May 10, 2024	Updated part numbers (pages 2 and 13)

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