

Image Reject Mixer 34 - 46 GHz

Rev. V1

Features

- Fundamental Image Reject Mixer
- 7.0 dB Conversion Loss
- 20.0 dB Image Rejection
- +24 dBm Input Third Order Intercept
- 100% On-Wafer RF Testing
- 100% Visual Inspection to MIL-STD-883 Method 2010
- RoHS* Compliant and 260°C Reflow Compatible

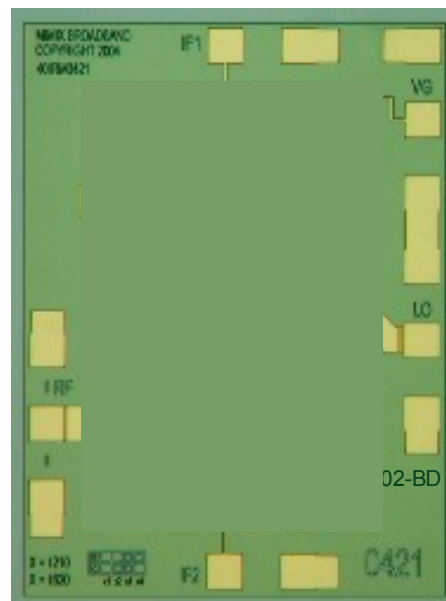
Description

M/A-COM Tech's 34.0-46.0 GHz GaAs MMIC fundamental image reject mixer can be used as an up- or down-converter. The device has a conversion loss of 7.0 dB with a 20.0 dB image rejection across the band. I and Q mixer outputs are provided and an external 90 degree hybrid is required to select the desired sideband. This MMIC uses M/A-COM Tech's GaAs PHEMT device model technology, and is based upon electron beam lithography to ensure high repeatability and uniformity. The chip has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process. This device is well suited for Millimeter-wave Point-to-Point Radio, LMDS, SATCOM and VSAT applications.

Ordering Information

Part Number	Package
XM1002-BD-000V	"V" - vacuum release gel paks
XM1002-BD-EV1	evaluation module

Chip Device Layout



Absolute Maximum Ratings

Parameter	Absolute Max.
Gate Bias Voltage (Vg)	+0.3 VDC
Input Power (RF Pin)	+20.0 dBm
Input Power (IF Pin)	+20.0 dBm
Storage Temperature (Tstg)	-65 °C to +165 °C
Operating Temperature (Ta)	-55 °C to +125 °C

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Electrical Specifications: 34-46 GHz (Upper Side Band) (Ambient Temperature T = 25°C)

Parameter	Units	Min.	Typ.	Max.
Frequency Range (RF) Lower Side Band	GHz	34.0	-	46.0
Frequency Range (LO)	GHz	30.0	-	50.0
Frequency Range (IF)	GHz	DC	-	4.0
RF Return Loss (S11)	dB	-	18.0	-
IF Return Loss (S22)	dB	-	10.0	-
LO Return Loss (S33)	dB	-	8.0	-
Conversion Loss (S21)	dB	-	7.0	8.0
LO Input Drive (P _{LO})	dBm	-	+12.0	-
Image Rejection	dBc	15.0	20.0	-
Isolation LO/RF	dB	-	11.0	-
Isolation LO/IF	dB	-	30.0	-
Isolation RF/IF	dB	-	30.0	-
Input Third Order Intercept (IIP3)	dBm	-	+24.0	-
Gate Bias Voltage (Vg1)	VDC	-2.0	-0.5	+0.1

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 2 devices.

Typical Performance Curves

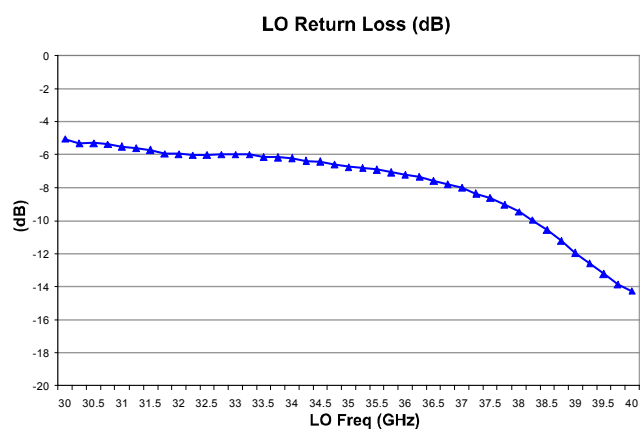
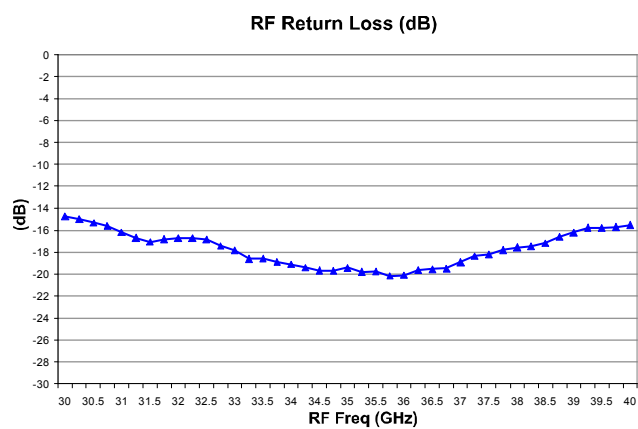
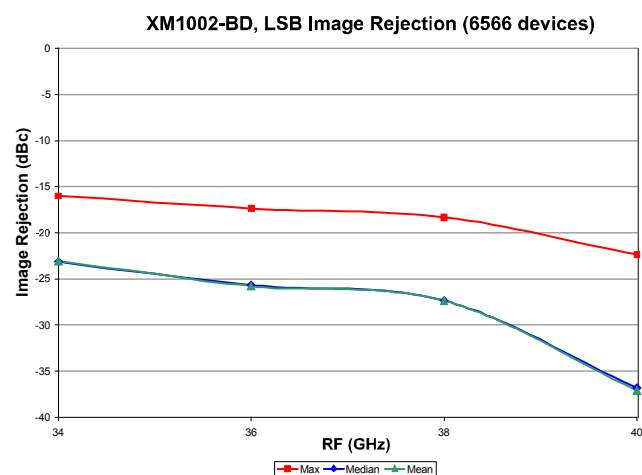
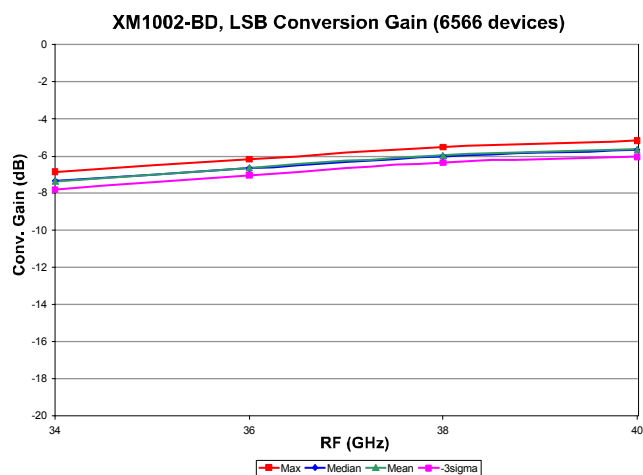
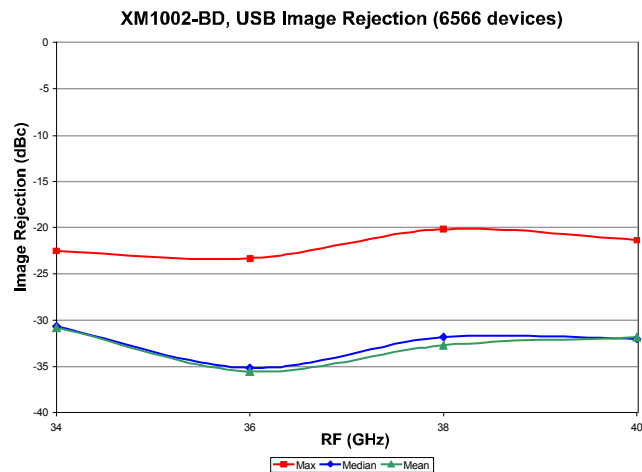
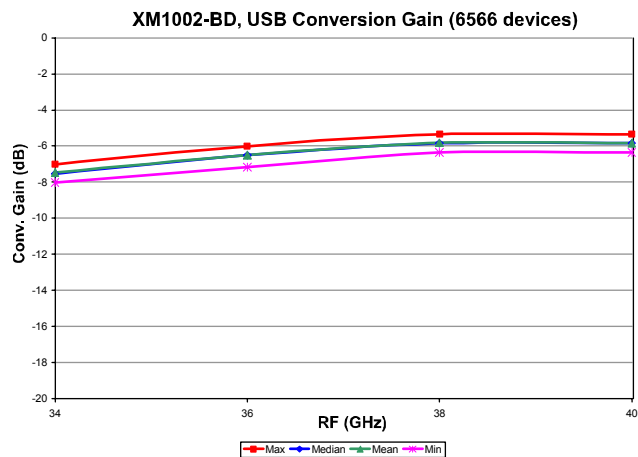


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Typical Performance Curves (cont.)

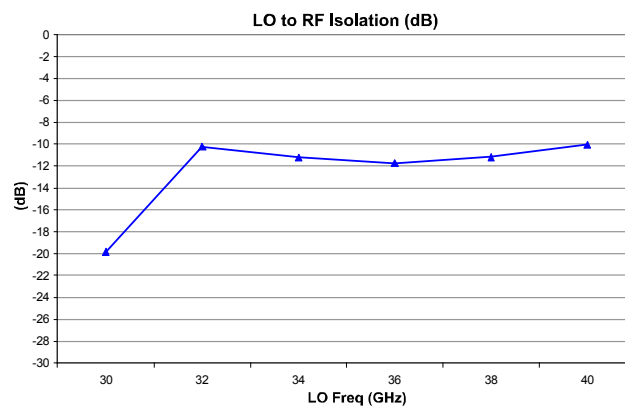
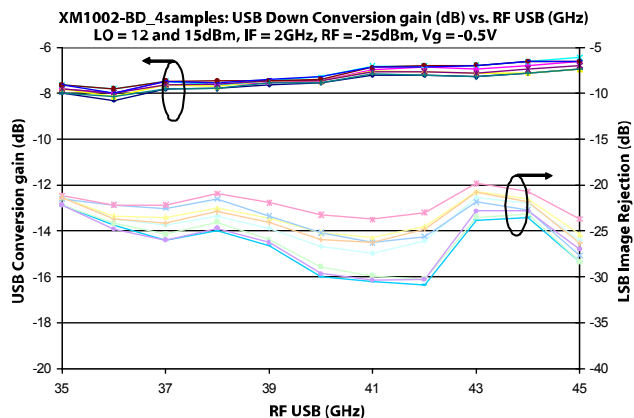


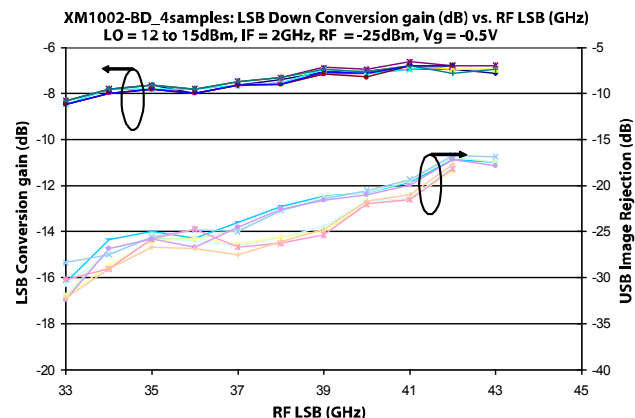
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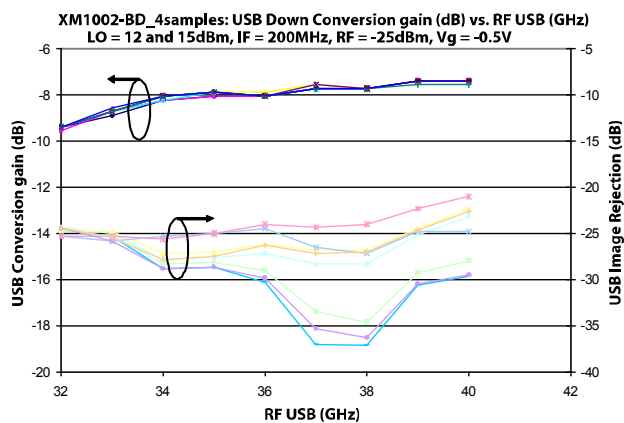
Typical Performance Curves (cont.)



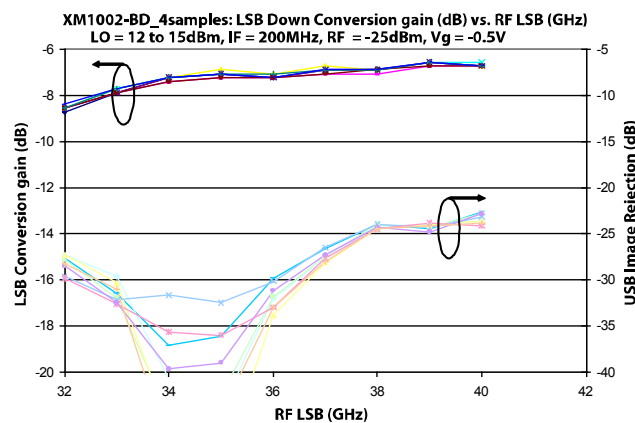
IF=2 GHz



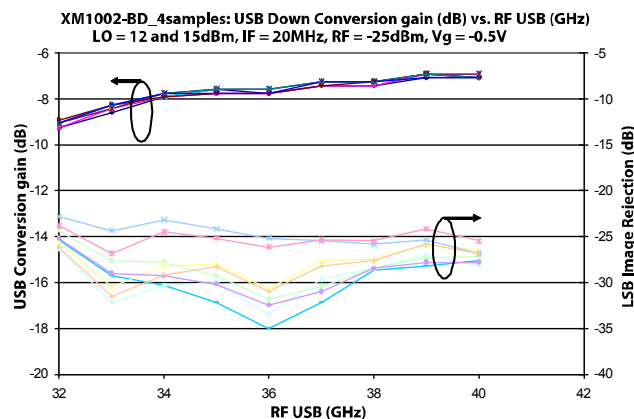
IF=2 GHz



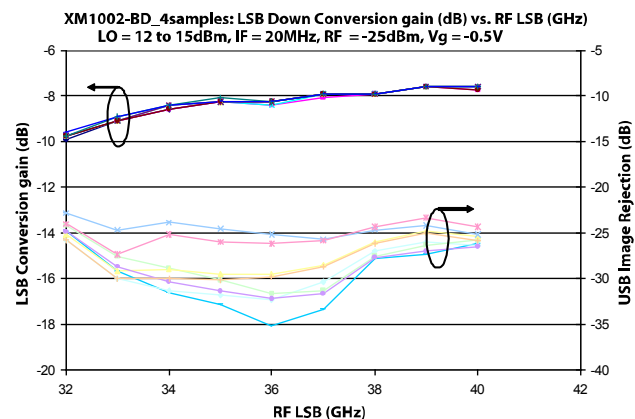
IF=200 MHz



IF=200 MHz



IF=20 MHz

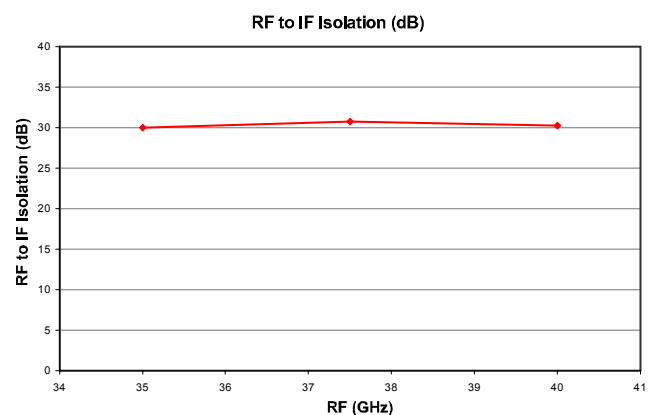
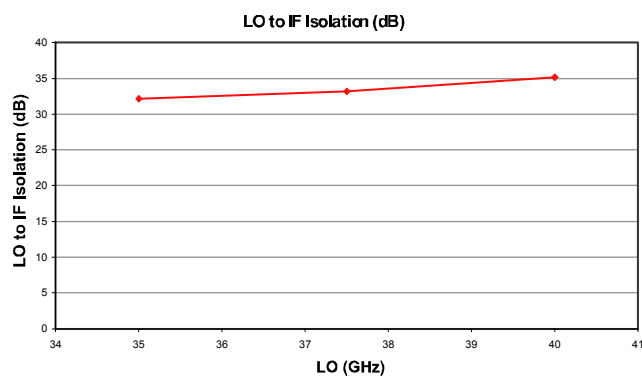
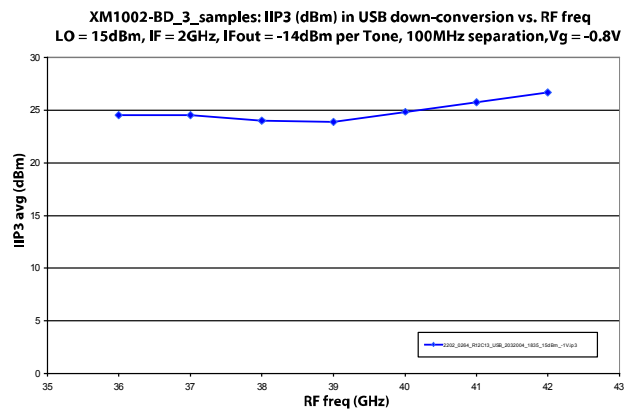
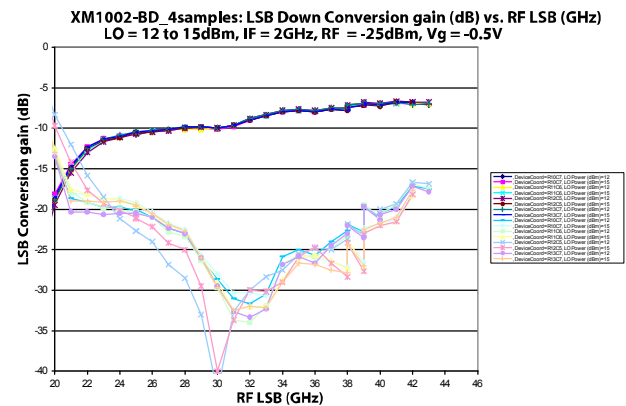
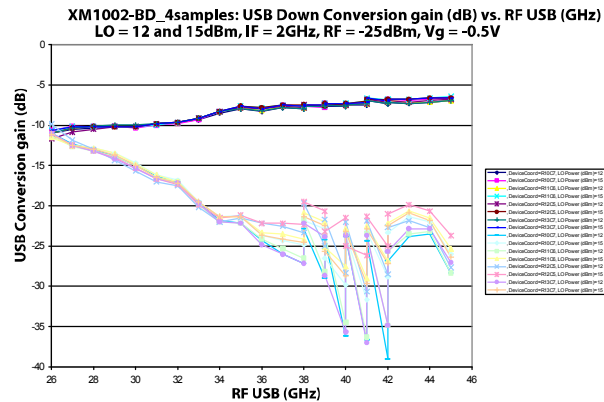


IF=20 MHz

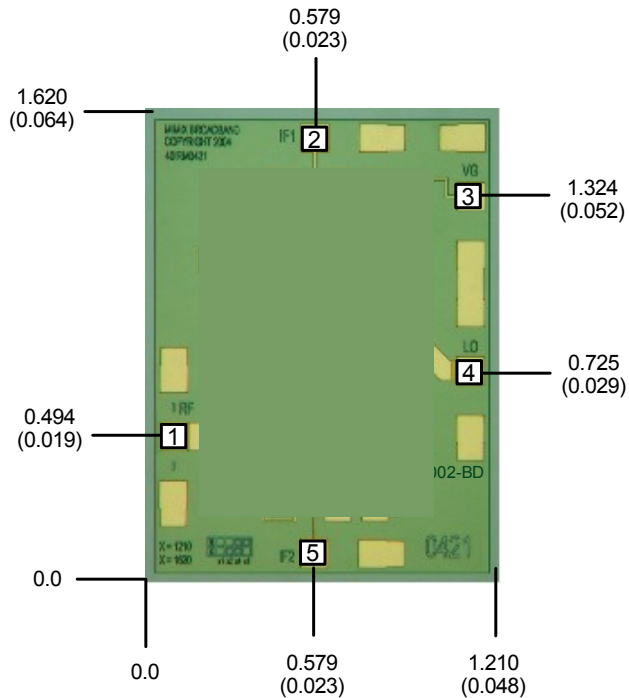
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Typical Performance Curves (cont.)



Mechanical Drawing



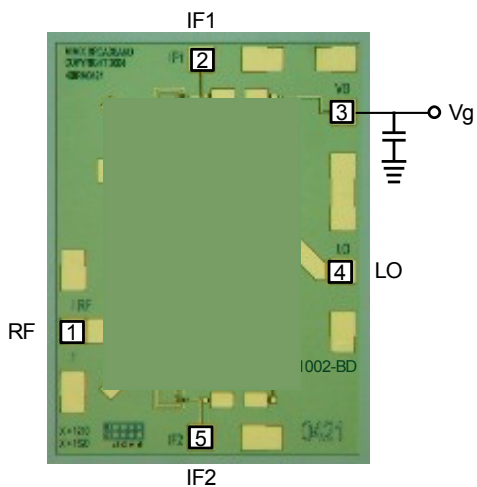
(Note: Engineering designator is 40IRM0421)

Units: millimeters (inches) Bond pad dimensions are shown to center of bond pad.
Thickness: 0.110 +/- 0.010 (0.0043 +/- 0.0004), Backside is ground, Bond Pad/Backside Metallization: Gold
All Bond Pads are 0.100 x 0.100 (0.004 x 0.004).

Bond pad centers are approximately 0.109 (0.004) from the edge of the chip.
Dicing tolerance: +/- 0.005 (+/- 0.0002). Approximate weight: 1.215 mg.

Bond Pad #1 (RF) Bond Pad #3 (Vg) Bond Pad #5 (IF2)
Bond Pad #2 (IF1) Bond Pad #4 (LO)

Bias Arrangement



Bypass Capacitors - See App Note [2]

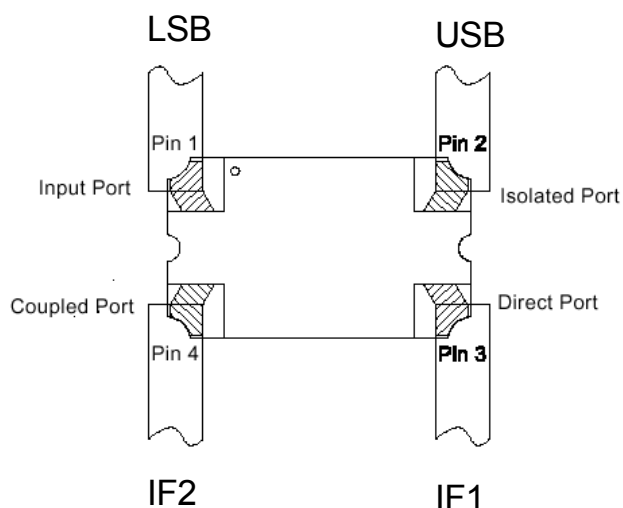
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App Note [1] Biasing - As shown in the bonding diagram, the pHEMT mixer devices are operated using a separate gate voltage V_{g1} . Set $V_{g1} = -0.5V$ for optimum conversion loss performance.

App Note [2] Bias Arrangement - Each DC pad (V_{g1}) needs to have DC bypass capacitance (~ 100 - 200 pF) as close to the device as possible. Additional DC bypass capacitance (~ 0.01 uF) is also recommended.

App Note [3] USB/LSB Selection -

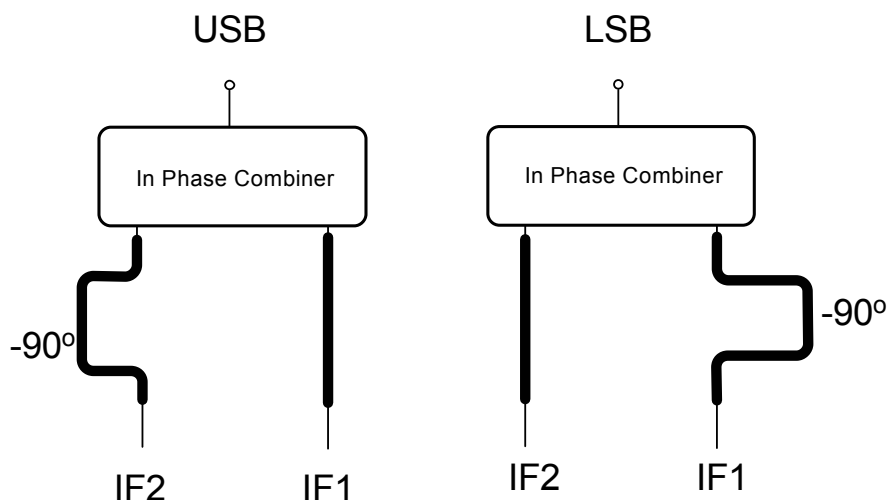


For Upper Side Band Operation (USB): With IF1 and IF2 connected to the direct port (0°) and coupled port (90°) respectively as shown in the diagram, the USB signal will reside on the isolated port. The input port must be loaded with 50 ohms.

For Lower Side Band Operation (LSB): With IF1 and IF2 connected to the direct port (0°) and coupled port (90°) respectively as shown in the diagram, the LSB signal will reside on the input port. The isolated port must be loaded with 50 ohms.

Note: The coupled port can be used as an alternative input but the port location of the Coupled and Direct ports reverse.

An alternate method of Selection of USB or LSB:



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