PFM™ in a VIA™ Package AC-DC Converter

PFM4414xB6M48D0yBz

Isolated AC-DC Converter with PFC

Features & Benefits

- Universal input (85 – 264V_{AC})
- 48V_{OUT}, regulated, isolated SELV
- 92% typical efficiency
- Built-in EMI filtering
- Chassis-mount or board-mount packaging options
- Always-on, self-protecting converter control architecture
- SELV Output
- Two temperature grades including operation to –40°C
- VIA Package
- Robust Mechanical Design
- Versatile thermal management capability
- Safe and reliable secondary-side energy storage
- High MTBF
- 140W/in^3 power density
- 4414 package
- AC Input Front-End Module provides external rectification and transient protection (AIM™ sold separately)

Typical Applications

- Small-cell base stations
- Telecom switching equipment
- LED lighting
- Industrial power systems

Product Ratings	
V_{IN} = 85 – 264V	P_{OUT} = up to 400W
V_{OUT} = 48V	I_{OUT} = 8.33A

Product Description

The PFM in a VIA Package is a highly advanced 400W AC-DC converter operating from a rectified universal AC input which delivers an isolated and regulated Safety Extra Low Voltage (SELV) 48V secondary output.

This unique, ultra-low-profile module incorporates AC-DC conversion, integrated filtering and transient surge protection in a chassis-mount or PCB-mount form factor.

The PFM enables a versatile two-sided thermal strategy which greatly simplifies thermal design challenges.

When combined with downstream Vicor DC-DC conversion components and regulators, the PFM allows the Power Design Engineer to employ a simple, low-profile design which will differentiate his end-system without compromising on cost or performance metrics.

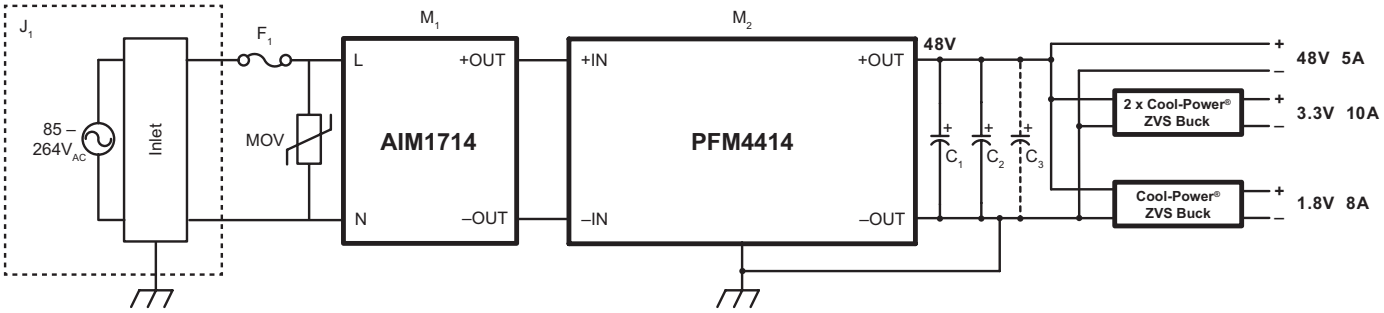
Shown with required companion component, AIM™ (see pages 2-3)

Size:
4.35 x 1.40 x 0.37in
[110.55 x 35.54 x 9.40mm]

Part Ordering Information

Product Function	Package Length	Package Width	Package Type	Input Voltage	Range Ratio	Output Voltage (Range)	Max Output Power	Product Grade	Option Field	
PFM	44	14	x	B6	M	48	D0	y	B	z
PFM = Power Factor Module	Length in Inches x 10	Width in Inches x 10	**B** = Board VIA **V** = Chassis VIA	Internal Reference				**C** = –20 to 100°C **T** = –40 to 100°C	**B0** = Chassis/Always On **B4** = Short Pin/Always On **B8** = Long Pin/Always On	

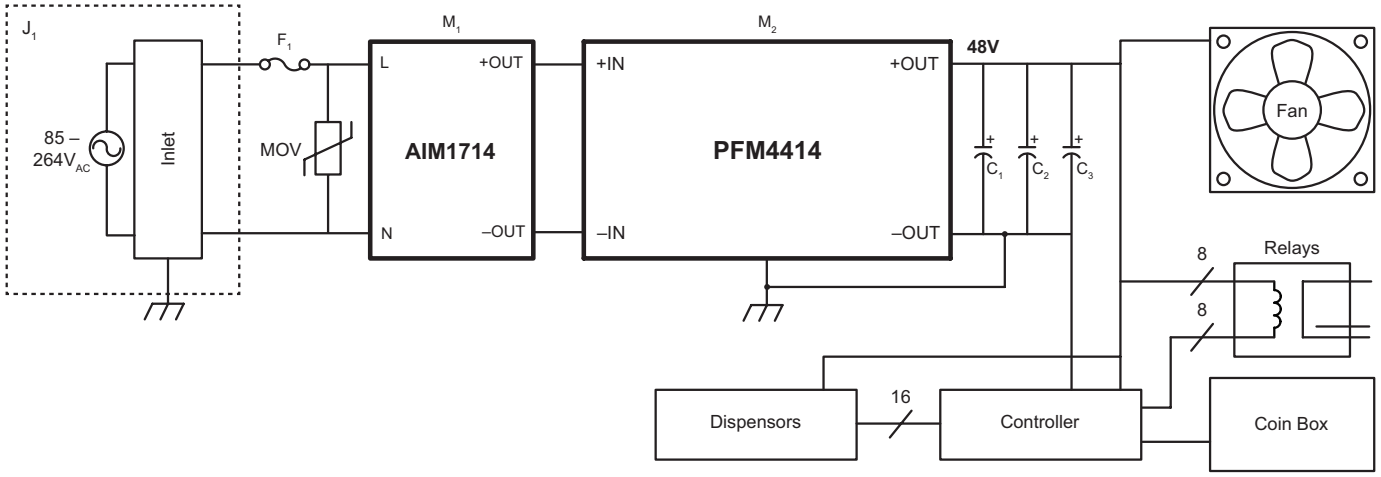
Typical PCB-Mount Applications



The PCB terminal option allows mounting on an industry standard printed circuit board, with two different pin lengths. Vicor offers a variety of downstream DC-DC converters driven by the 48V output of the PFM in a VIA package. The 48V output is usable directly by loads that are tolerant of the PFC line ripple, such as fans, motors, relays, and some types of lighting. Use downstream DC-DC point-of-load converters where more precise regulation is required.

Parts List for Typical PCB-Mount Applications	
J1	**Qualtek** 703W IEC 320-C14 Power Inlet
F1	Littelfuse 0216008.MXP 8A 250V_{AC} 5 x 20mm holder
M1	**Vicor AIM™** AIM1714BB6MC7D5yzz
M2	**Vicor PFM** PFM4414BB6M48D0yzz
C1	**Nichicon** UVR1J472MRD 4700µF 63V 3.4A 22 x 50mm bent 90° x 2 pcs **or**
	CDE 380LX472M063K022 4700µF 63V 4.9A 30 x 30mm snap x 2 pcs **or**
	Sic Safco Cubisic LP A712121 10,000µF 63V 6.4A 45 x 75 x 12mm rectangular **or** **CDE** MLPGE1571 6800µF 63V 5.2A 45 x 50 x 12.5mm, 1 or 2pcs.
MOV	**Littelfuse** TMOV20RP300E VARISTOR 10kA 300V 250J 20mm

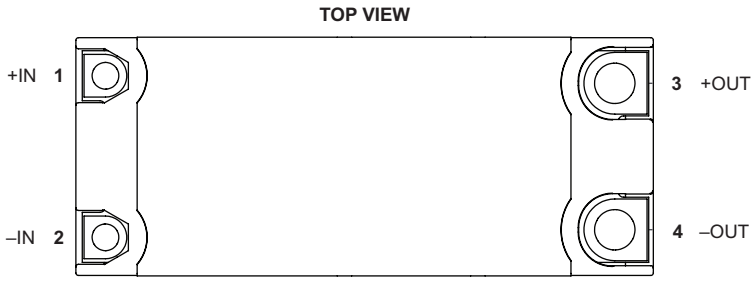
Typical Chassis-Mount Applications



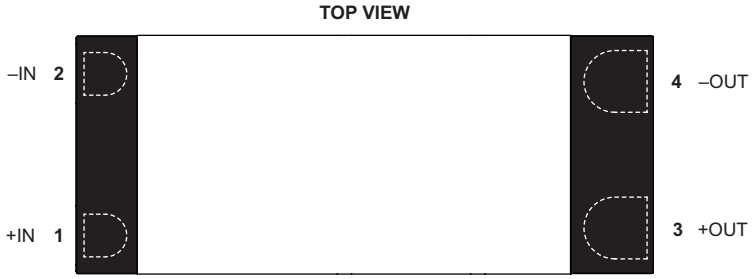
The PFM in a VIA package is available in chassis-mount option, saving the cost of a PCB and allowing access to both sides of the power supply for cooling. The parts list below minimizes the number of interconnects required between necessary components, and selects components with terminals traditionally used for point-to-point chassis wiring.

Parts List for Typical Chassis-Mount Applications	
J1	**Qualtek** 719W or 723W IEC 320-C14 Power Inlet
F1	**Littelfuse** 0216008.MXP 8A 250V_{AC} 5 x 20mm in a J1, or separate fuse holder
M1	**Vicor AIM™** AIM1714VB6MC7D5yzz
M2	**Vicor PFM** PFM4414VB6M48D0yzz
C1	**UCC** E32D630HPN103MA67M 10,000µF, 63V 7.4A, 35 x 67mm screw terminal **or** **Kemet** ALS30A103DE063, 10,000µF 63V 10.8A 36 x 84mm screw terminal
MOV	**Littelfuse** TMOV20RP300E VARISTOR 10kA 300V 250J 20mm

Pin Configuration



PFM4414 VIA - Chassis Mount - Terminals Up



PFM4414 VIA - PCB Mount - Pins Down

Please note that these Pin drawings are not to scale.

Pin Descriptions

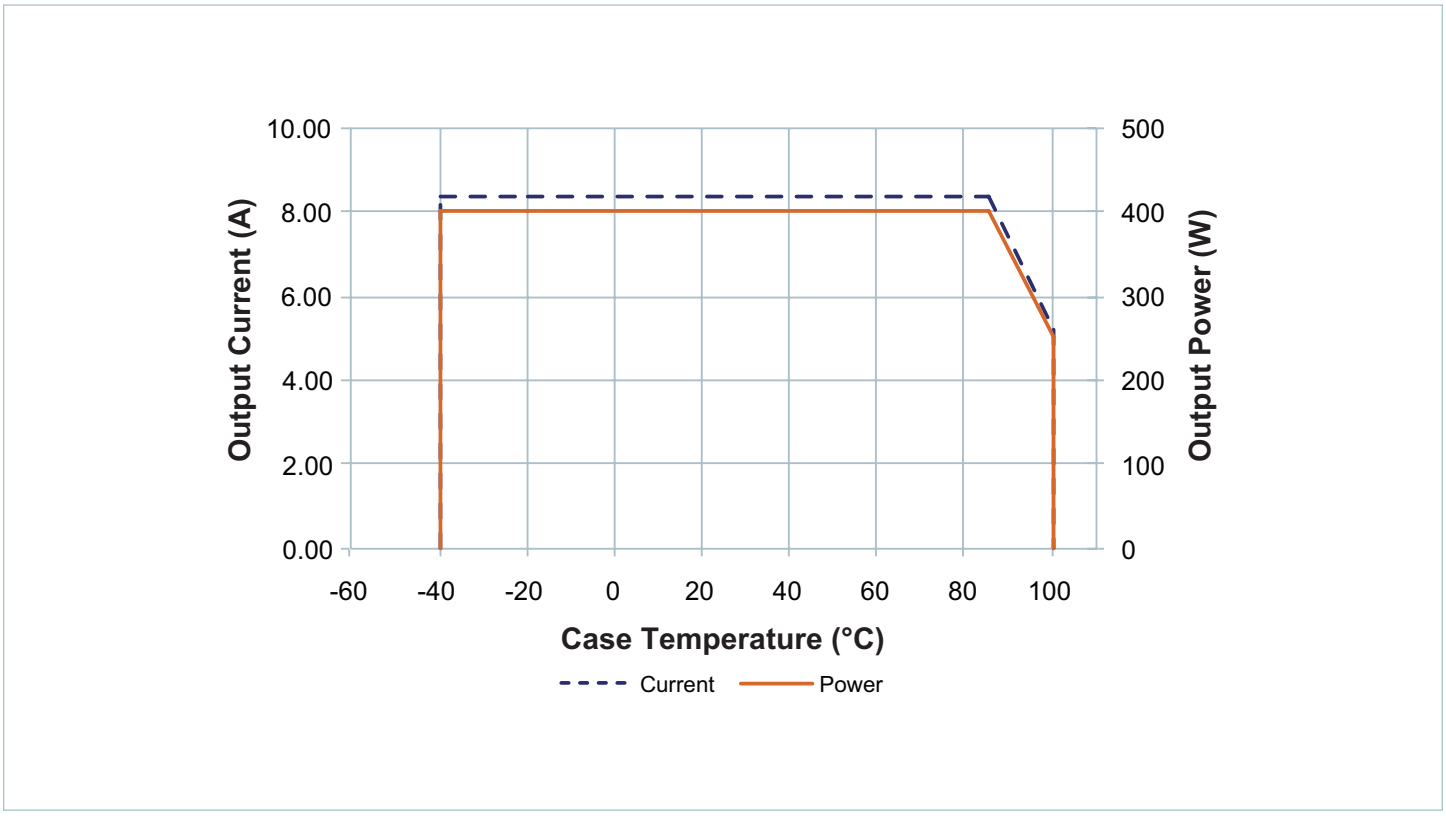
Pin Number	Signal Name	Type	Function
1	+IN	INPUT POWER	Positive input power terminal
2	–IN	INPUT POWER RETURN	Negative input power terminal
3	+OUT	OUTPUT POWER	Positive output power terminal
4	–OUT	OUTPUT POWER RETURN	Negative output power terminal

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
Input Voltage +IN to –IN	1ms max	0	600	V_{PK}
Input Voltage (+IN to –IN)	Continuous, Rectified	0	275	V_{RMS}
Output Voltage (+OUT to –OUT)		–0.5	58	V_{DC}
Output Current		0.0	12.4	A
Screw Torque	4 mounting, 2 input, 2 output		4 [0.45]	in·lbs [N·m]
Operating Internal Temperature	T-Grade	–40	125	°C
Storage Temperature	T-Grade	–65	125	°C
Dielectric Withstand [a]	See note below [b]			
Input – Case	Basic Insulation	1500 / 2121		V_{AC} / V_{DC}
Input – Output	Reinforced Insulation	3000 / 4242		V_{AC} / V_{DC}
Output – Case	Functional Insulation	1500 / 2121		V_{AC} / V_{DC}

[a] Please see Dielectric Withstand section. See page 19.
[b] AC hipot testing requires a minimum trip current setting of 10mA on the dielectric strength tester in order to prevent false failures.



Safe operating area

Electrical Specifications

Specifications apply over all line and load conditions, 50Hz and 60Hz line frequencies, T_{INT} = 25°C, unless otherwise noted; **boldface** specifications apply over the temperature range of the specified product grade. C_{OUT} is 10,000µF ±20% unless otherwise specified.

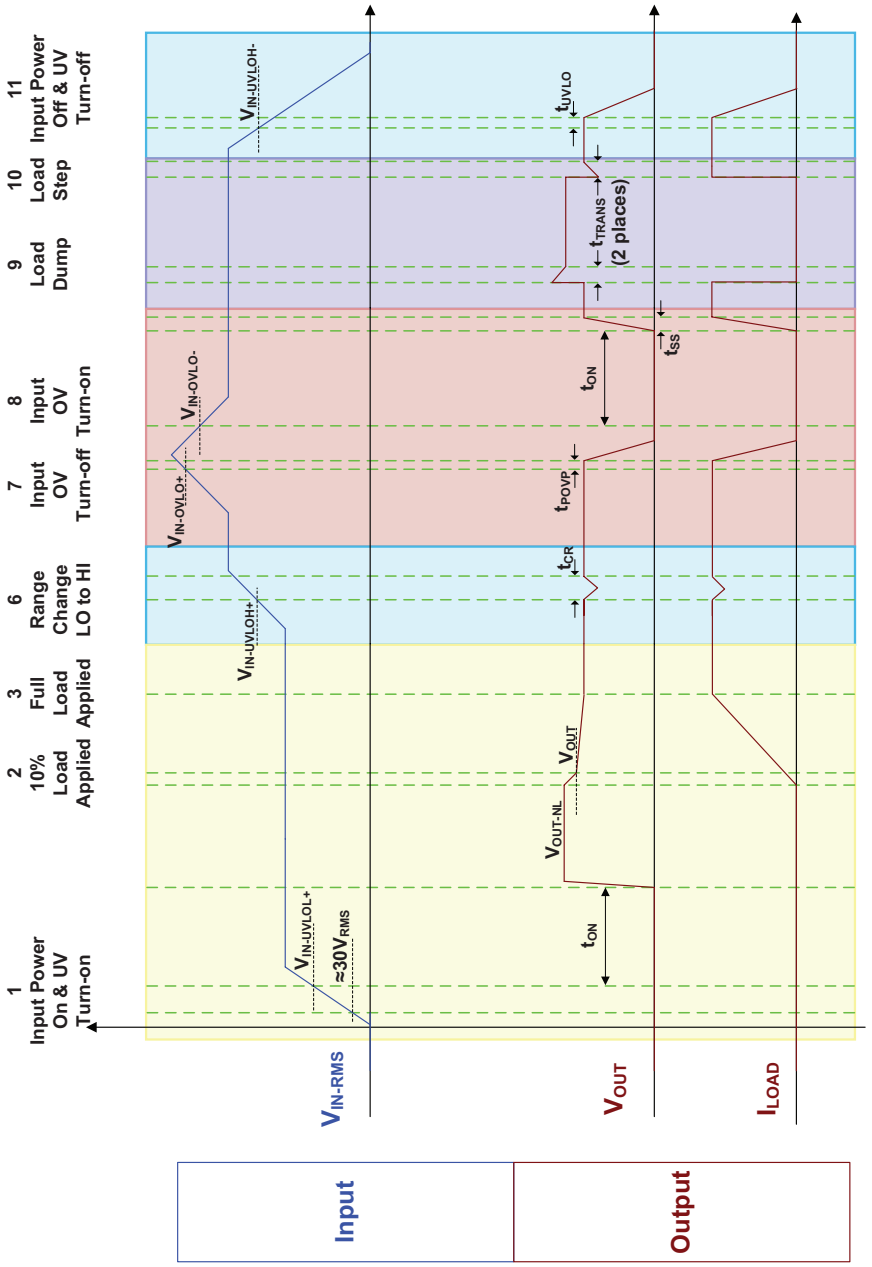
Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Power Input Specification						
Input Voltage Range, Continuous Operation	V_{IN}		**85**		**264**	V_{RMS}
Input Voltage Range, Transient, Non-Operational (Peak)	V_{IN}	1ms			600	V
Input Current (Peak)	I_{INRP}	See Figure 8, start-up waveforms			12	A
Source Line Frequency Range	f_{line}		47		63	Hz
Power Factor	PF	Input power >200W		0.96		-
Input Inductance, Maximum	L_{IN}	Differential mode inductance, common-mode inductance may be higher. See section "Source Inductance Considerations" on page 15.			1	mH
Input Capacitance, Maximum	C_{IN}	After AIM™, between +IN and –IN			1.5	µF
No Load Specification						
Input Power – No Load, Maximum	P_{NL}				15	W
Power Output Specification						
Output Voltage Set Point	V_{OUT}	V_{IN} = 230V_{RMS}, 100% load	46	48	50	V
Output voltage, No Load	V_{OUT-NL}	Over all operating steady state line conditions.	**42**		**54**	V
Output Voltage Range (Transient)	V_{OUT}	Non-faulting abnormal line and load transient conditions	**30**		**57.6**	V
Output Power	P_{OUT}	See SOA on Page 5			**400**	W
Efficiency	η	V_{IN} = 230V, full load, exclusive of AIM losses	90.5	92.4		%
		85V < V_{IN} < 264V, full load, exclusive of AIM losses	90.0	92.1		%
		85V < V_{IN} < 264V, full load, exclusive of AIM losses	**88.5**	**91.7**		%
Output Voltage Ripple, Switching Frequency	$V_{OUT-PP-HF}$	Over all operating steady-state line and load conditions, 20MHz BW, measured at output, Figure 5		200	**2000**	mV
Output Voltage Ripple Line Frequency	$V_{OUT-PP-LF}$	Over all operating steady-state line and load conditions, 20MHz BW		3.0	7.0	V
Output Capacitance (External)	$C_{OUT-EXT}$	Allows for ±20% capacitor tolerance	**6800**		**15000**	µF
Output Turn-On Delay	T_{ON}	From V_{IN} applied		500	**1000**	ms
Start-Up Set-Point Aquisition Time	T_{SS}	Full load		500	1000	ms
Cell Reconfiguration Response Time	T_{CR}	Full load		5.5	11	ms
Voltage Deviation (Transient)	$\%V_{OUT-TRANS}$		–37.5		20	%
Recovery Time	T_{TRANS}			300	600	ms
Line Regulation	$\%V_{OUT-LINE}$	Full load			3	%
Load Regulation	$\%V_{OUT-LOAD}$	10% to 100% load			3	%
Output Current (Continuous)	I_{OUT}	SOA			8.33	A
Output Current (Transient)	I_{OUT-PK}	20ms duration, average power ≤P_{OUT}, max			**12.5**	A

Electrical Specifications (Cont.)

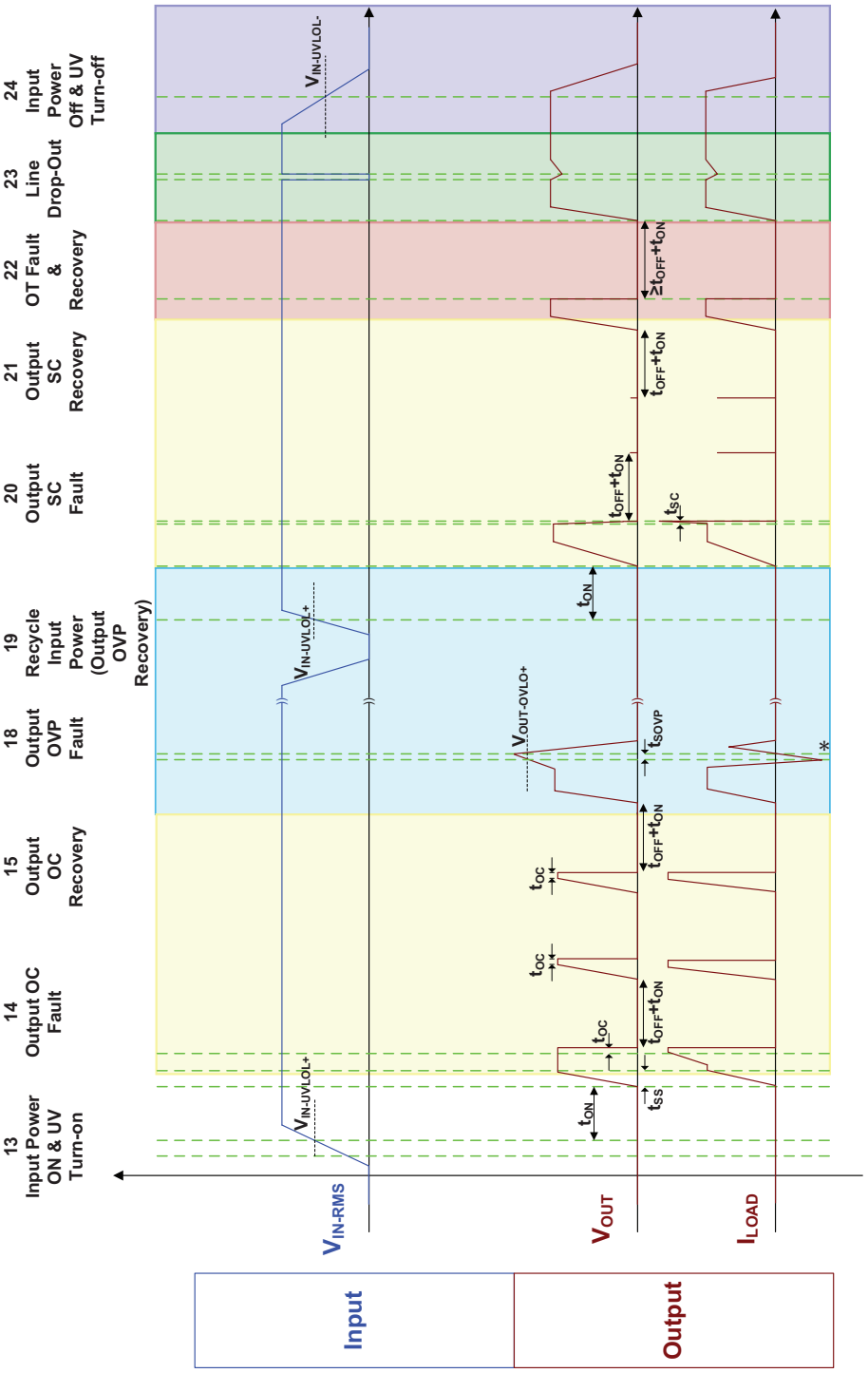
Specifications apply over all line and load conditions, 50Hz and 60Hz line frequencies, T_{INT} = 25°C, unless otherwise noted; **boldface** specifications apply over the temperature range of the specified product grade. C_{OUT} is 10,000µF ±20% unless otherwise specified.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Protections						
Input Undervoltage Threshold, High Range	V_{UVLOH-}		**132**	135		V_{RMS}
Input Undervoltage Recover, High Range	V_{UVLOH+}			145	**148**	V_{RMS}
Input Undervoltage Turn-On, Low Range	$V_{IN-UVLOL+}$	See Timing Diagram		74	**83**	V_{RMS}
Input Undervoltage Turn-Off, Low Range	$V_{IN-UVLOL-}$		**65**	71		V_{RMS}
Input Overvoltage Turn-On	$V_{IN-OVLO-}$	See Timing Diagram	**265**	270		V_{RMS}
Input Overvoltage Turn-Off	$V_{IN-OVLO+}$			273	**287**	V_{RMS}
Output Overvoltage Threshold	$V_{OUT-OVLO+}$	Instantaneous, latched shutdown	**58**	61	**64**	V
Upper Start / Restart Temperature Threshold (Case)	$T_{CASE-OTP-}$		**100**			°C
Overtemperature Shutdown Threshold (Internal)	$T_{INT-OTP+}$			125		°C
Overtemperature Shutdown Threshold (Case)	$T_{CASE-OTP+}$			**110**		°C
Overcurrent Blanking Time	T_{OC}	Based on line frequency	**400**	460	**550**	ms
Input Overvoltage Response Time	T_{POVP}			40		ms
Input Undervoltage Response Time	T_{UVLO}	Based on line frequency		200		ms
Output Overvoltage Response Time	T_{SOVP}	Powertrain on		30		ms
Short Circuit Response Time	T_{SC}	Powertrain on, operational state		270		µs
Fault Retry Delay Time	T_{OFF}	See Timing Diagram		10		s
Output Power Limit	P_{PROT}	50% overload for 20ms typ allowed	**400**			W

Timing Diagram



Timing Diagram (Cont.)



Application Characteristics

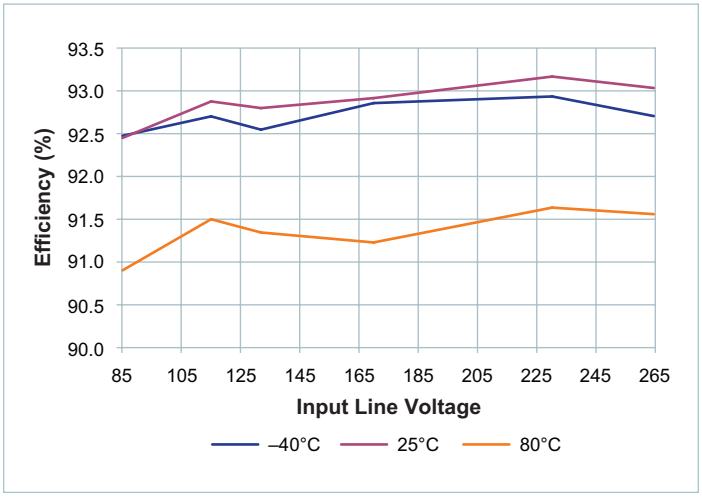


Figure 1 — *Full-load efficiency vs. line voltage*

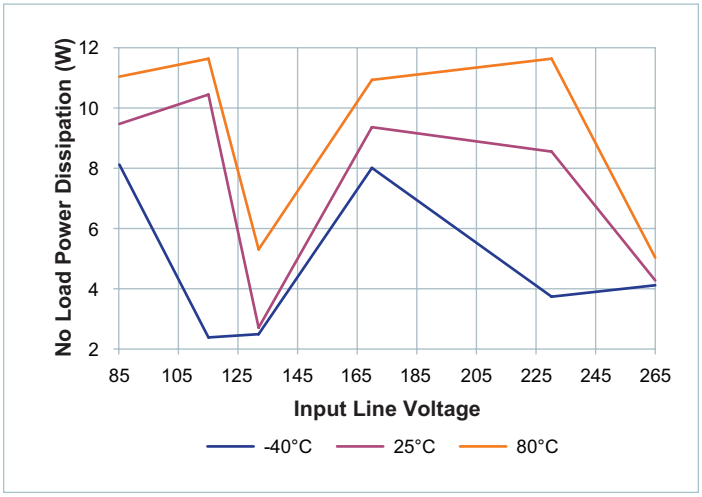


Figure 2 — *Typical no-load power dissipation vs. V_{IN}, module enabled*

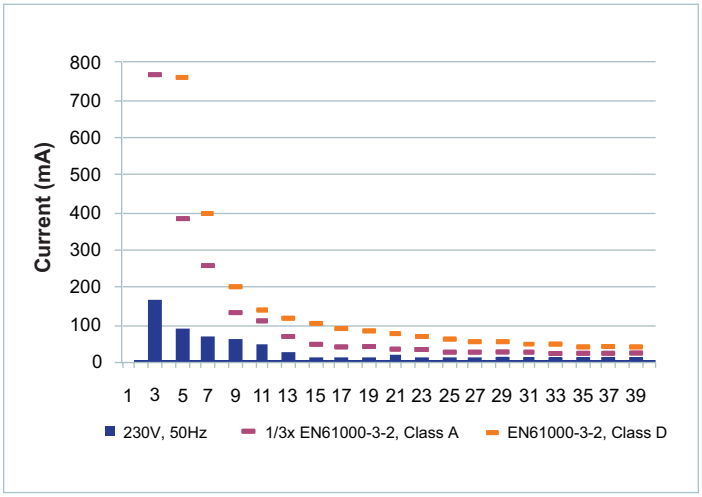


Figure 3 — *Typical input current harmonics, full load vs. V_{IN} using typical applications circuit on pages 2 & 3*

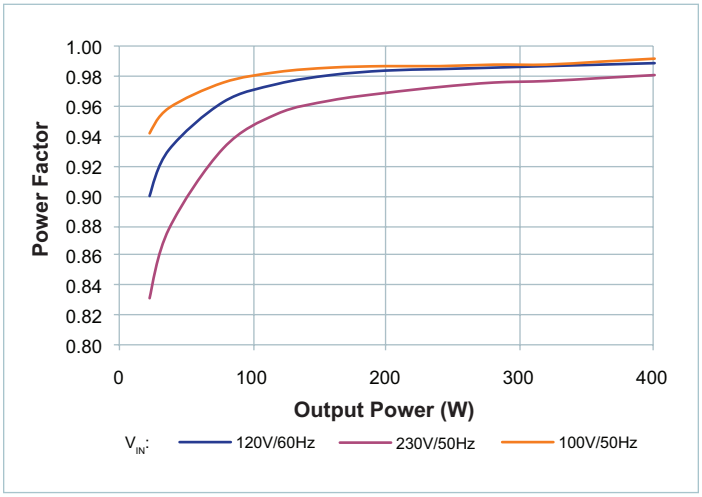


Figure 4 — *Typical power factor vs. V_{IN} and I_{OUT} using typical applications circuit on pages 2 & 3*

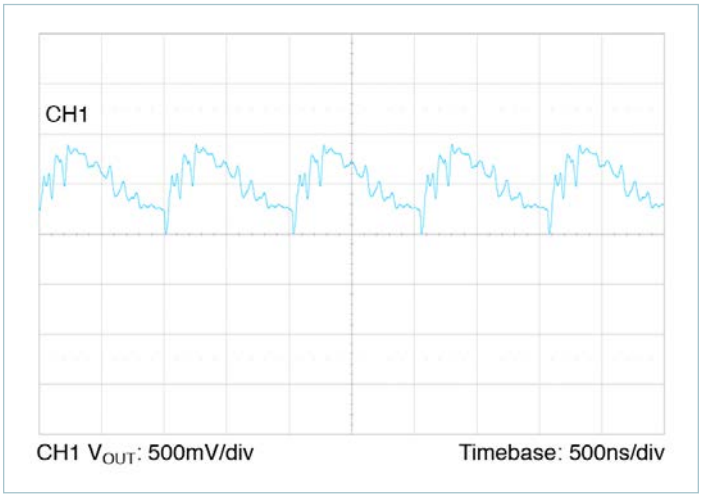


Figure 5 — *Typical switching frequency output voltage ripple waveform, T_{CASE} = 30°C, V_{IN} = 230V, I_{OUT} = 8.3A, no external ceramic capacitance, 20MHz BW*

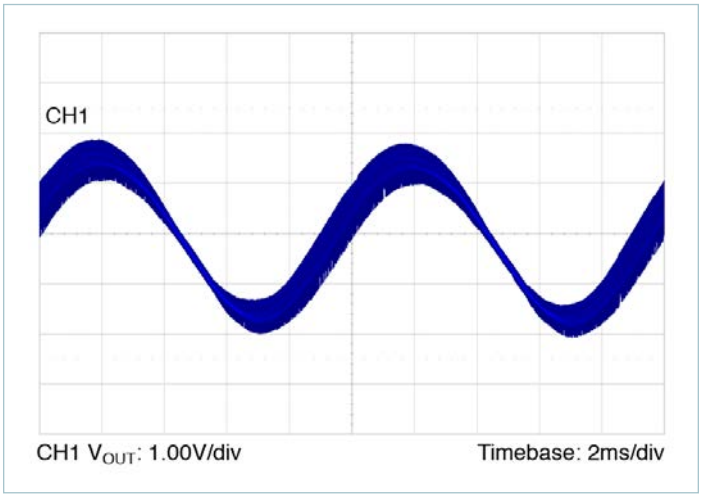


Figure 6 — *Typical line frequency output voltage ripple waveform, T_{CASE} = 30°C, V_{IN} = 230V, I_{OUT} = 8.3A, C_{OUT} = 10,000µF. 20MHz BW*

Application Characteristics (Cont.)

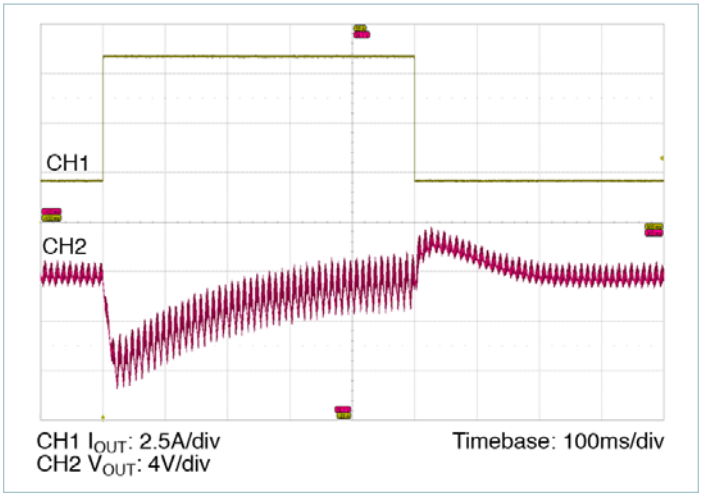


Figure 7 — *Typical output voltage transient response, T_{CASE} = 30°C, V_{IN} = 230V, I_{OUT} = 8.3A, 2.1A C_{OUT} = 10,000µF*

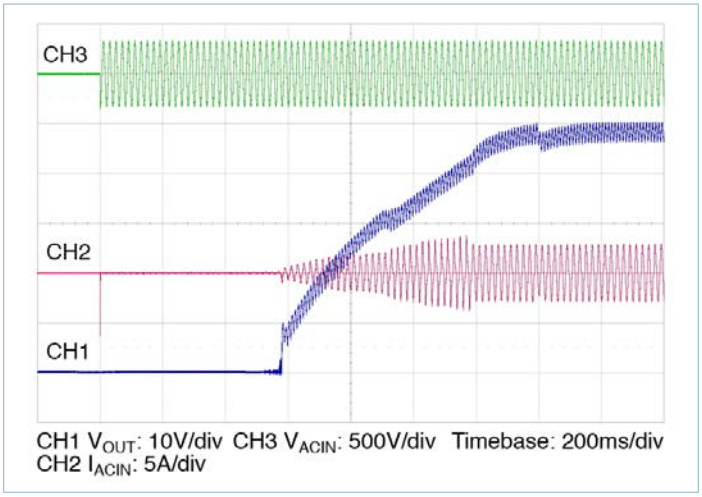


Figure 8 — *Typical start-up waveform, application of V_{IN}, I_{OUT} = 8.3A, C_{OUT} = 10,000µF*

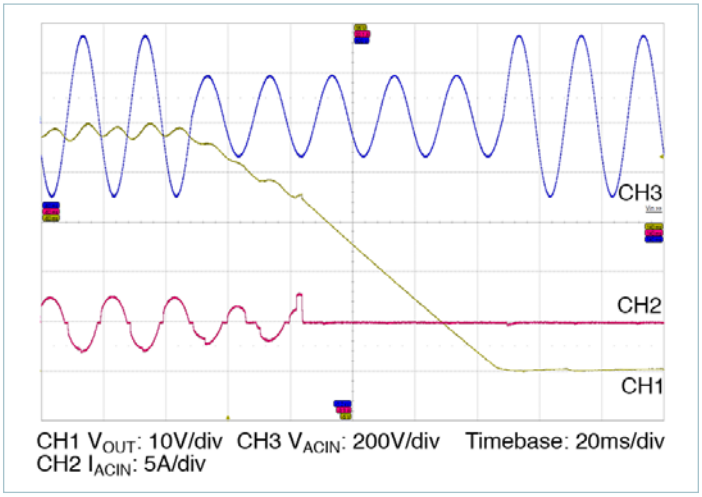


Figure 9 — *230V, 120V range change transient response, I_{OUT} = 8.3A, C_{OUT} = 10,000µF*

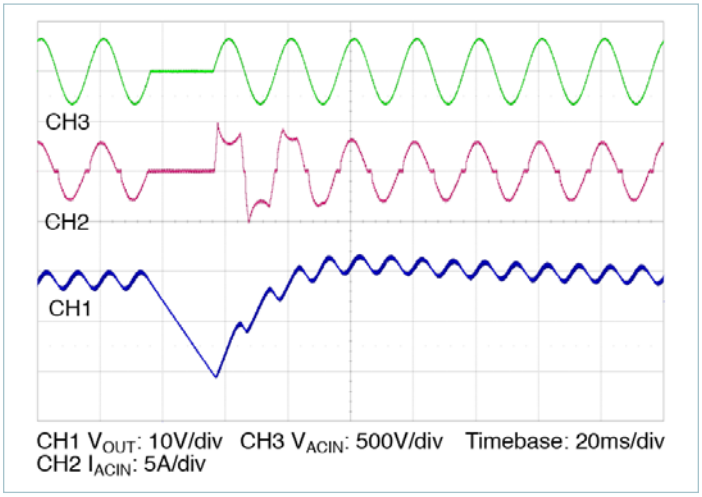


Figure 10 — *Line drop out, 230V 50Hz, 0° phase, I_{OUT} = 8.3A, C_{OUT} = 10,000µF*

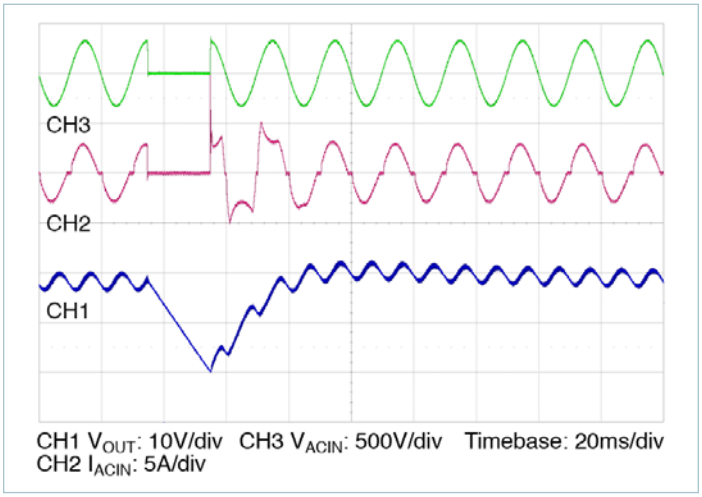


Figure 11 — *Line drop out, 90° phase, V_{IN} = 230V, I_{OUT} = 8.3A, C_{OUT} = 10,000µF*

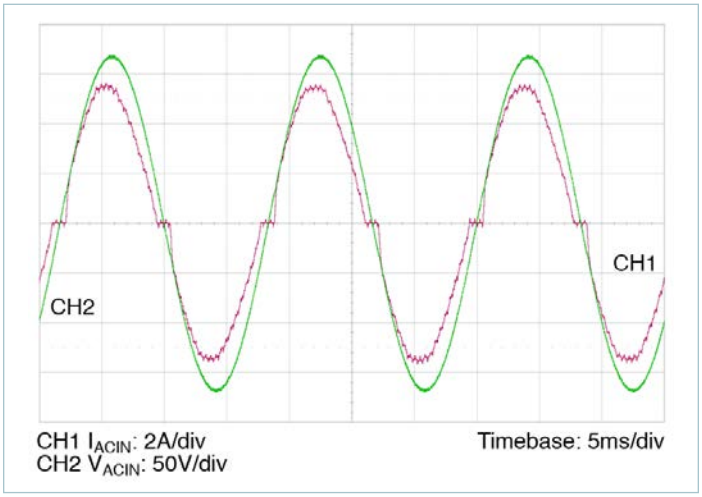


Figure 12 — *Typical line current waveform, V_{IN} = 120V, 60Hz I_{OUT} = 8.3A, C_{OUT} = 10,000µF*

Application Characteristics (Cont.)

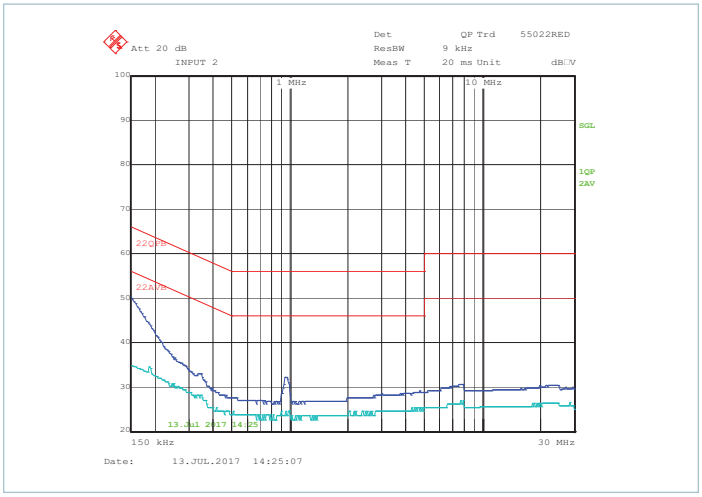


Figure 13 — *Typical EMI spectrum, peak scan, 90% load, V_{IN} = 115V, C_{OUT} = 10,000µF using typical chassis-mount application circuit*

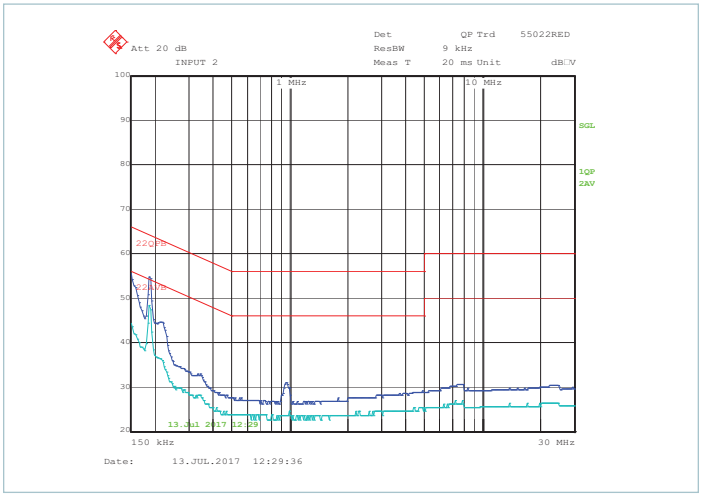


Figure 14 — *Typical EMI spectrum, peak scan, 90% load, V_{IN} = 230V, C_{OUT} = 10,000µF using typical chassis-mount application circuit*

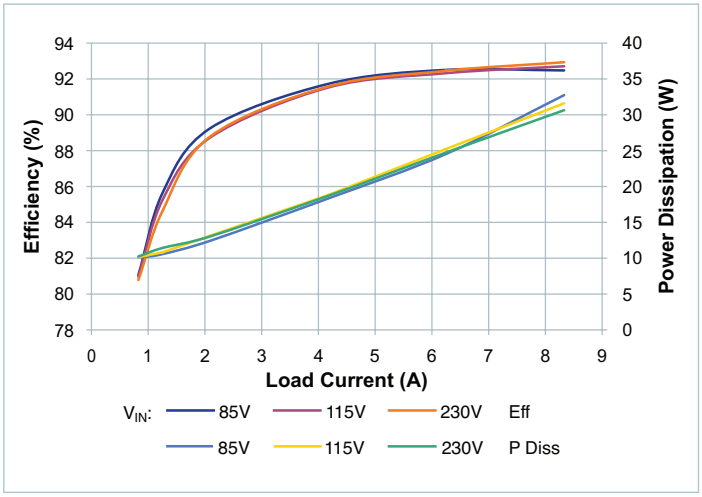


Figure 15 — *V_{IN} to V_{OUT} efficiency and power dissipation vs. V_{IN} and I_{OUT}, T_{CASE} = –40°C*

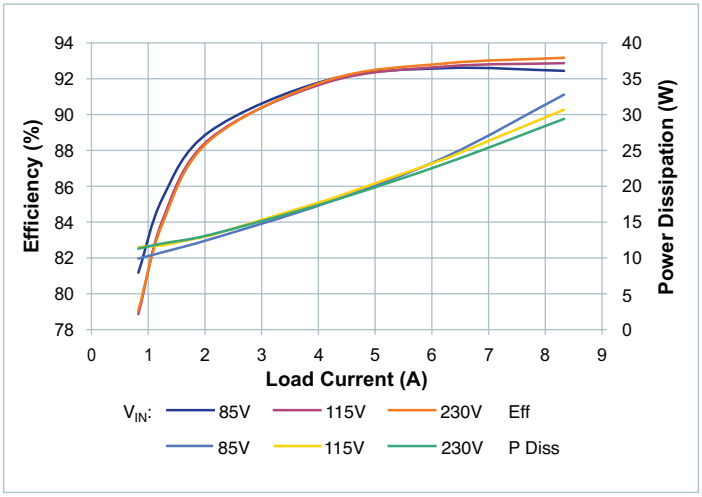


Figure 16 — *V_{IN} to V_{OUT} efficiency and power dissipation vs. V_{IN} and I_{OUT}, T_{CASE} = 25°C*

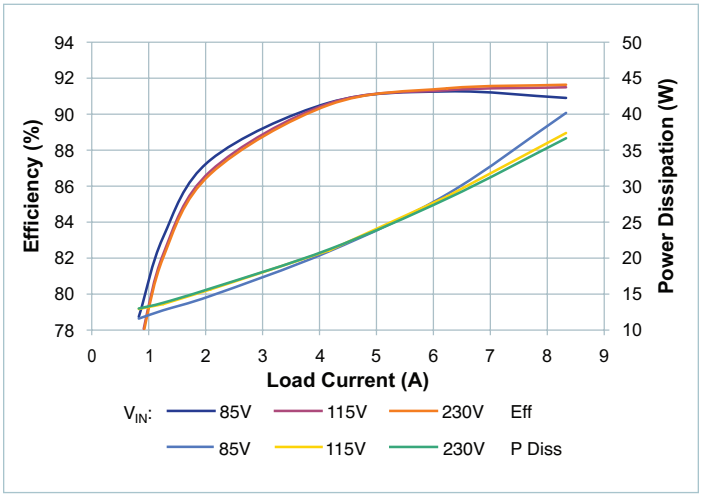


Figure 17 — *V_{IN} to V_{OUT} efficiency and power dissipation vs. V_{IN} and I_{OUT}, T_{CASE} = 80°C*

General Characteristics

Specifications apply over all line and load conditions, 50Hz and 60Hz line frequencies, T_C = 25°C, unless otherwise noted; **boldface** specifications apply over the temperature range of the specified Product Grade.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L		110.30 [4.34]	110.55 [4.35]	110.80 [4.36]	mm [in]
Width	W		35.29 [1.39]	35.54 [1.40]	35.79 [1.41]	mm [in]
Height	H		9.019 [0.355]	9.40 [0.37]	9.781 [0.385]	mm [in]
Volume	Vol	Without heat sink		36.9 [2.25]		cm^3 [in^3]
Weight	W			148 [5.2]		g [oz]
Pin Material		C145 copper, half hard				
Underplate		Low-stress ductile nickel	50		100	µin
Pin Finish		Palladium	0.8		6	µin
		Soft Gold	0.12		2	µin
Thermal						
Operating Case Temperature	T_C	C-Grade, see derating curve in SOA	–20		100	°C
		T-Grade, see derating curve in SOA	–40		100	°C
Thermal Resistance, Pin Side	$\theta_{INT\_PIN\_SIDE}$			1.3		°C/W
Thermal Resistance, Non-Pin Side	$\theta_{INT\_NON\_PIN\_SIDE}$			1.7		°C/W
Thermal Resistance, Housing	θ_{HOU}			0.57		°C/W
Shell Thermal Capacity				54		J/K
Thermal Design		See Thermal Considerations on Page 17				
Assembly						
ESD Rating	ESD_{HBM}	Human Body Model, JEDEC JESD 22-A114C.01	1,000			V
	ESD_{MM}	Machine Model, JEDEC JESD 22-A115B	N/A			
	ESD_{CDM}	Charged Device Model, JEDEC JESD 22-C101D	200			
Safety						
Agency Approvals / Standards		cTUVus, EN60950-1 and IEC 60950-1				
		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable				
		Touch Current measured in accordance with IEC 60990 using measuring network Figure 3 (PFM in a VIA package only)		0.5		mA

General Characteristics (Cont.)

Specifications apply over all line and load conditions, 50Hz and 60Hz line frequencies, T_C = 25°C, unless otherwise noted; **boldface** specifications apply over the temperature range of the specified Product Grade.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
EMI/EMC Compliance						
FCC Part 15, EN55022, CISPR22: 2006 + A1: 2007, Conducted Emissions		Class B Limits - with –OUT connected to GND				
EN61000-4-5: 2006, Surge Immunity		Level 3, Immunity Criteria A, external TMOV and fuse, shown on page 2 or 3, required				

Reliability						
Case	**Reliability Assurance Relex Modeling, Studio 2007, v2]**	**Temp (°C)**	**Duty Cycle**	**Condition**	**MTBF (MHrs)**	**FIT**
1	Telcordia Issue 2, Method I Case 1	25	100%	GB,GC	0.702	1424
2	MIL-HDBK-217FN2 Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer	25	100%	GB,GC	0.322	3102
3	Telcordia Issue 2, Method I Case 3	25	100%	GB,GC	2.43	412

Product Details and Design Guidelines

Building Blocks and System Designs

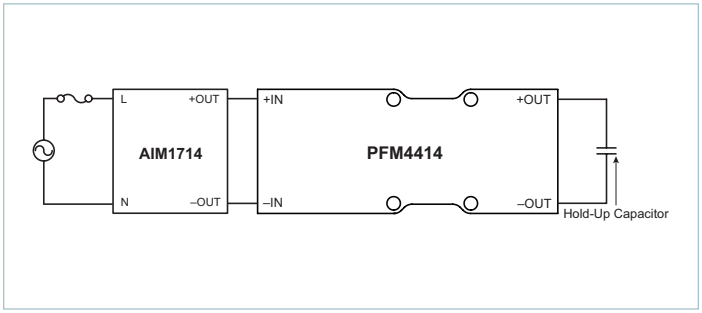


Figure 18 — *400W universal AC-DC supply*

The PFM in a VIA package is a high-efficiency AC-DC converter, operating from a universal AC input to generate an isolated SELV $48V_{DC}$ output bus with power factor correction. It is the key component of an AC-DC power supply system such as the one shown in Figure 18 above.

The input to the PFM in a VIA package is a rectified sinusoidal AC source with a power factor maintained by the module with harmonics conforming to IEC 61000-3-2. Internal filtering enables compliance with the standards relevant to the application (Surge, EMI, etc.). See EMI/EMC Compliance standards on Page 14.

The module uses secondary-side energy storage (at the SELV 48V bus) to maintain output hold up through line dropouts and brownouts. Downstream regulators also provide tighter voltage regulation, if required.

Traditional PFC Topology

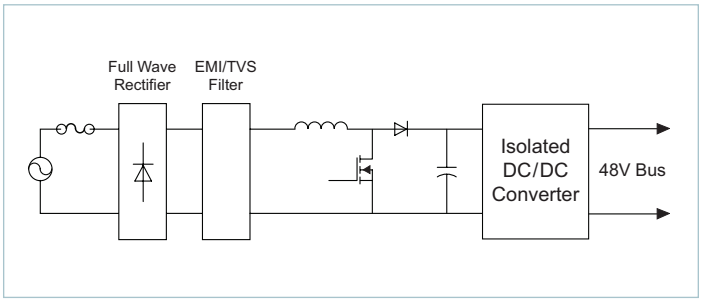


Figure 19 — *Traditional PFC AC-DC supply*

To cope with input voltages across worldwide AC mains ($85 – 264V_{AC}$), traditional AC-DC power supplies (Figure 19) use two power conversion stages: 1) a PFC boost stage to step up from a rectified input as low as $85V_{AC}$ to ~$380V_{DC}$; and 2) a DC-DC down converter from $380V_{DC}$ to a 48V bus.

The efficiency of the boost stage and of traditional power supplies is significantly compromised operating from worldwide AC lines as low as $85V_{AC}$.

Adaptive Cell™ Topology

With its single stage Adaptive Cell™ topology, the PFM in a VIA package enables consistently high-efficiency conversion from worldwide AC mains to a 48V bus and efficient secondary-side power distribution.

Input Fuse Selection

PFM in a VIA package products are not internally fused in order to provide flexibility in configuring power systems. Input line fusing is recommended at system level, in order to provide thermal protection in case of catastrophic failure. The fuse shall be selected by closely matching system requirements with the following characteristics:

- Recommended fuse: 216 Series Littelfuse 8A or lower current rating (usually greater than the PFM maximum current at lowest input voltage)
- Maximum voltage rating (usually greater than the maximum possible input voltage)
- Ambient temperature
- Breaking capacity per application requirements
- Nominal melting I^2t

Source Inductance Considerations

The PFM Powertrain uses a unique Adaptive Cell Topology that dynamically matches the powertrain architecture to the AC line voltage. In addition the PFM uses a unique control algorithm to reduce the AC line harmonics yet still achieve rapid response to dynamic load conditions presented to it at the DC output terminals. Given these unique power processing features, the PFM can expose deficiencies in the AC line source impedance that may result in unstable operation if ignored.

It is recommended that for a single PFM, the line source inductance should be no greater than 1mH for a universal AC input of 100 – 240V. If the PFM will be operated at 240V nominal only, the source impedance may be increased to 2mH. For either of the preceding operating conditions it is best to be conservative and stay below the maximum source inductance values. When multiple PFM's are used on a single AC line, the inductance should be no greater than 1mH/N, where N is the number of PFM's on the AC branch circuit, or 2mH/N for $240V_{AC}$ operation. It is important to consider all potential sources of series inductance including and not limited to, AC power distribution transformers, structure wiring inductance, AC line reactors, and additional line filters. Non-linear behavior of power distribution devices ahead of the PFM may further reduce the maximum inductance and require testing to ensure optimal performance.

If the PFM is to be utilized in large arrays, the PFMs should be spread across multiple phases or sources thereby minimizing the source inductance requirements, or be operated at a line voltage close to $240V_{AC}$. Vicor Applications should be contacted to assist in the review of the application when multiple devices are to be used in arrays.

Fault Handling

Input Undervoltage (UV) Fault Protection

The input voltage is monitored by the microcontroller to detect an input under voltage condition. When the input voltage is less than the UVLO threshold, a fault is detected. After a time t_{UVLO}, the unit shuts down. Faults lasting less than t_{UVLO} may not be detected. Such a fault does not go through an auto-restart cycle. Once the input voltage rises above the UVLO threshold, the unit recovers from the input UV fault, the powertrain resumes normal switching after a time t_{ON} and the output voltage of the unit reaches the set-point voltage within a time t_{SS}.

Overcurrent (OC) Fault Protection

If the output current exceeds its current limit, a fault is detected and the output voltage of the module falls after a time t_{OC}. As long as the fault persists, the module goes through an auto-restart cycle with off time equal to $t_{OFF} + t_{ON}$ and on time equal to t_{OC}. Faults shorter than a time t_{OC} may not be detected. Once the fault is cleared, the module follows its normal start-up sequence after a time t_{OFF}.

Short Circuit (SC) Fault Protection

The module responds to a short circuit event within a time t_{SC}. The module then goes through an auto restart cycle, with an off time equal to $t_{OFF} + t_{ON}$ and an on time equal to t_{SC}, for as long as the short circuit fault condition persists. Once the fault is cleared, the unit follows its normal start-up sequence after a time t_{OFF}. Faults shorter than a time t_{SC} may not be detected.

Temperature Fault Protection

The microcontroller monitors the temperature within the PFM. If this temperature exceeds $T_{INT\text{-}OTP+}$, an overtemperature fault is detected, and the output voltage of the PFM falls. Once the case temperature falls below $T_{CASE\text{-}OTP-}$, after a time greater than or equal to t_{OFF}, the converter recovers and undergoes a normal restart. Faults shorter than a time t_{OTP} may not be detected. If the temperature falls below $T_{CASE\text{-}UTP-}$, an undertemperature fault is detected, and the output voltage of the unit falls. Once the case temperature rises above $T_{CASE\text{-}UTP}$, after a time greater than or equal to t_{OFF}, the unit recovers and undergoes a normal restart.

Output Overvoltage Protection (OVP)

The microcontroller monitors the primary sensed output voltage to detect output OVP. If the primary sensed output voltage exceeds $V_{OUT\text{-}OVLO+}$, a fault is latched, and the output voltage of the module falls after a time t_{SOVP}. Faults shorter than a time t_{SOVP} may not be detected. This type of fault is a latched fault and requires that the input power be recycled to recover from the fault.

Ruggedized Auto Range Functionality

The input voltage range is determined at power up time, to cover the input voltage range of either 85 – 132V_{RMS} or 170 – 264V_{RMS}, called low range and high range. Once selected, dynamic range changes are limited by the logic explained below.

In low range, operation continues until the input either drops under the UVLO threshold (in which case the converter turns off), or until the input exceeds the range transition threshold.

The increase in input voltage can be temporary, as when handling a surge on the input, or it could be permanent, as can happen in the rare occasion when an input is turned on during a brown-out or sag condition on a high-voltage system:

- If the increase is temporary, and the input returns under range transition threshold within 0.8s, operation continues in low range.
- If the input stays over the range transition threshold, the converter changes to high range.

In high range, operation continue up to to the OVLO. A surge will cause the power train to turn off on a short-term basis to protect itself during the rise in input voltage, and it will return to operation when the input returns to the operating range.

When the input crosses under the range transition threshold, the input turns off as it considers this to be the high-range UVLO threshold. If the converter returns above the range transition threshold within 50ms, the converter will resume operation in high range. If the converter does not return to operating range, the system will reset to the default power down condition, monitoring the input and waiting to decide whether it should start up into low range or high range.

Input Line Cycle Skipping

This model does not have input line cycle skipping. As a result, the regulation spec is guaranteed from no load to full load. Because of this, this model does not present high peak-to-peak output voltage under low load conditions, limiting perturbation that may affect downstream regulators ability to regulate their outputs as tightly as desired. The only sources of output voltage perturbation (from largest to smallest amplitude) are:

- Discharge of output bulk caps during a dropout condition
- Surge transients that can cause similar dropout or short-term range change
- Input line cycle ripple, with amplitude proportional to output current
- Switching frequency ripple, which can be reduced further with a higher frequency filter stage if necessary

Noise-sensitive applications should still test to ensure they can handle or safely ignore these AC transitions on the PFM output bus, which are expected to be handled by the downstream point-of-load regulators.

Hold-Up Capacitance

The PFM in a VIA package uses secondary-side energy storage (at the SELV 48V bus) and downstream regulators to maintain output hold up through line dropouts and brownouts. The module's output bulk capacitance can be sized to achieve the required hold up functionality.

Hold-up time depends upon the output power drawn from the PFM in a VIA package based AC-DC front end and the input voltage range of downstream DC-DC converters.

The following formula can be used to calculate hold-up capacitance for a system comprised of PFM and a downstream regulator:

$$C = 2 \bullet P_{OUT} \bullet (0.005 + t_d) / (V_2^2 - V_1^2)$$

Where:

C PFM's output bulk capacitance in Farads

t_d Hold-up time in seconds

P_{OUT} PFM's output power in Watts

V_2 Output voltage of PFM's converter in Volts

V_1 Downstream regulator undervoltage turn off (Volts)
–OR–
P_{OUT} / I_{OUT-PK}, whichever is greater.

Output Filtering

The PFM in a VIA package requires an output bulk capacitor in the range of 6,800µF to 15,000µF for proper operation of the PFC front-end. A minimum 10,000µF is recommended for full rated output. Capacitance can be reduced proportionally for lower maximum loads.

The output voltage has the following two components of voltage ripple:

1. Line frequency voltage ripple: 2 • f_{LINE} Hz component

2. Switching frequency voltage ripple: 1MHz module switching frequency component (see Figure 5).

Line Frequency Filtering
Output line frequency ripple depends upon output bulk capacitance. Output bulk capacitor values should be calculated based on line frequency voltage ripple. High-grade electrolytic capacitors with adequate ripple current ratings, low ESR and a minimum voltage rating of 63V are recommended.

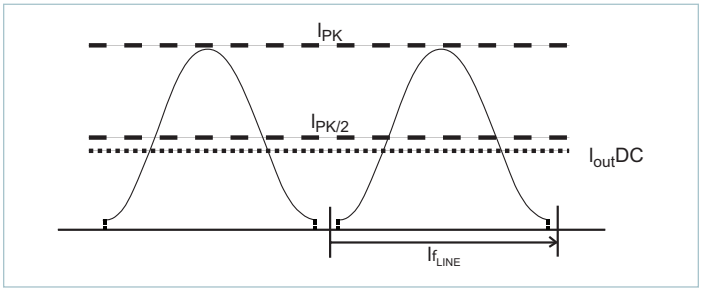


Figure 20 — *Output current waveform*

Based on the output current waveform, as seen in Figure 20, the following formula can be used to determine peak-to-peak line frequency output voltage ripple:

$$V_{PPL} \approx 0.2 \bullet P_{OUT} / (V_{OUT} \bullet f_{LINE} \bullet C)$$

Where:

V_{PPL} Output voltage ripple peak-to-peak line frequency

P_{OUT} Average output power

V_{OUT} Output voltage set point, nominally 48V

f_{LINE} Frequency of line voltage

C Output bulk capacitance

I_{DC} Maximum average output current

I_{PK} Peak-to-peak line frequency output current ripple

In certain applications, the choice of bulk capacitance may be determined by hold-up requirements and low frequency output voltage filtering requirements. Such applications may use the greater capacitance value determined from these requirements. The ripple current rating for the bulk capacitors can be determined from the following equation:

$$I_{RIPPLE} \approx 0.8 \bullet P_{OUT} / V_{OUT}$$

Switching Frequency Filtering
This is included within the PFM in a VIA. No external filtering is necessary for most applications. For the most noise-sensitive applications, a common-mode choke followed by two caps to PE GND will reduce switching noise further.

EMI Filtering and Transient Voltage Suppression

EMI Filtering

The PFM with PFC is designed such that it will comply with EN55022 Class B for Conducted Emissions with the Vicor AIM™, AIM1714xB6MC7D5yzz. The emissions spectrum is shown in Figures 13 & 14. If the positive output is connected to earth ground or both output terminals are to be left floating, a 4700pF 500V capacitor on the –OUT terminal to ground is also recommended.

EMI performance is subject to a wide variety of external influences such as PCB construction, circuit layout etc. As such, external components in addition to those listed herein may be required in specific instances to gain full compliance to the standards specified. Radiated emissions require certification at the system level. For best results, enclose the product in a steel enclosure. Filtering must be considered for every conductor leaving the enclosure, which can present itself as a potential transmission antenna.

Transient Voltage Suppression

The PFM contains line transient suppression circuitry to meet specifications for surge (i.e. EN61000-4-5) and fast transient conditions (i.e. EN61000-4-4 fast transient/"burst") when coupled with an external TMOV as shown on pages 2 and 3.

When more than one PFM is used in a system, each PFM should have its own fuse, TMOV and AIM in a VIA package.

Thermal Considerations

The VIA package provides effective conduction cooling from either of the two module surfaces. Heat may be removed from the pin-side surface, the non-pin-side surface or both. The extent to which these two surfaces are cooled is a key component for determining the maximum power that can be processed by a PFM, as can be seen from specified thermal operating area on Page 5. Since the PFM has a maximum internal temperature rating, it is necessary to estimate this internal temperature based on a system-level thermal solution. To this purpose, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors. Figure 21 shows the "thermal circuit" for the PFM in a VIA package.

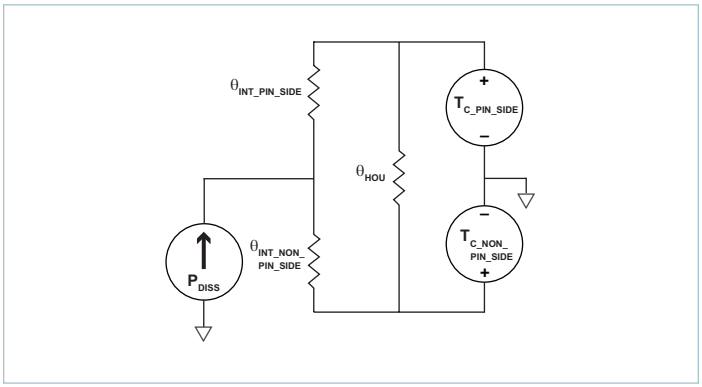


Figure 21 — *Double-sided cooling thermal model*

In this case, the internal power dissipation is P_{DISS}, $\theta_{INT\_PIN\_SIDE}$ and $\theta_{INT\_NON\_PIN\_SIDE}$ are thermal resistance characteristics of the VIA module and the pin-side and non-pin-side surface temperatures are represented as $T_{C\_PIN\_SIDE}$, and $T_{C\_NON\_PIN\_SIDE}$. It interesting to notice that the package itself provides a high degree of thermal coupling between the pin-side and non-pin-side case surfaces (represented in the model by the resistor θ_{HOU}). This feature enables two main options regarding thermal designs:

- Single-side cooling: the model of Figure 21 can be simplified by calculating the parallel resistor network and using one simple thermal resistance number and the internal power dissipation curves; an example for non-pin-side cooling only is shown in Figure 22.

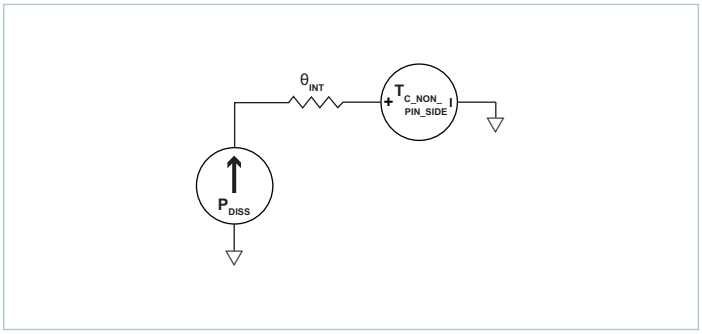


Figure 22 — *Single-sided cooling thermal model*

In this case, θ_{INT} can be derived as following:

$$\theta_{INT} = \frac{\left(\theta_{INT\_PIN\_SIDE} + \theta_{HOU}\right) \bullet \theta_{INT\_NON\_PIN\_SIDE}}{\theta_{INT\_PIN\_SIDE} + \theta_{HOU} + \theta_{INT\_NON\_PIN\_SIDE}}$$

- Double-side cooling: while this option might bring limited advantage to the module internal components (given the surface-to-surface coupling provided), it might be appealing in cases where the external thermal system requires allocating power to two different elements, like for example heat sinks with independent airflows or a combination of chassis/air cooling.

Powering a Constant-Power Load

When the output voltage of the PFM in a VIA package module is applied to the input of the downstream regulator, the regulator turns on and acts as a constant-power load. When the module's output voltage reaches the input undervoltage turn on of the regulator, the regulator will attempt to start. However, the current demand of the downstream regulator at the undervoltage turn-on point and the hold-up capacitor charging current may force the PFM in a VIA package into current limit. In this case, the unit may shut down and restart repeatedly. In order to prevent this multiple restart scenario, it is necessary to delay enabling a constant-power load when powered up by the upstream PFM in a VIA package until after the output set point of the PFM in a VIA package is reached.

This can be achieved by

1. Keeping the downstream constant-power load off during power up sequence,

   and

2. Turning the downstream constant-power load on after the output voltage of the module reaches 48V steady state.

After the initial start up, the output of the PFM can be allowed to fall to 30V during a line dropout at full load. In this case, the circuit should not disable the downstream regulator if the input voltage falls after it is turned on; therefore, some form of hysteresis or latching is needed on the enable signal for the constant-power load. The output capacitance of the PFM in a VIA package should also be sized appropriately for a constant-power load to prevent collapse of the output voltage of the module during line dropout (see Hold up Capacitance on Page 17). A constant-power load can be turned off after completion of the required hold up time during the power-down sequence or can be allowed to turn off when it reaches its own undervoltage shutdown point.

The timing diagram in Figure 23 shows the output voltage of the PFM in a VIA package and the downstream regulator's enable pin voltage and output voltage of the PRM regulator for the power up and power down sequence. It is recommended to keep the time delay approximately 10 – 20ms.

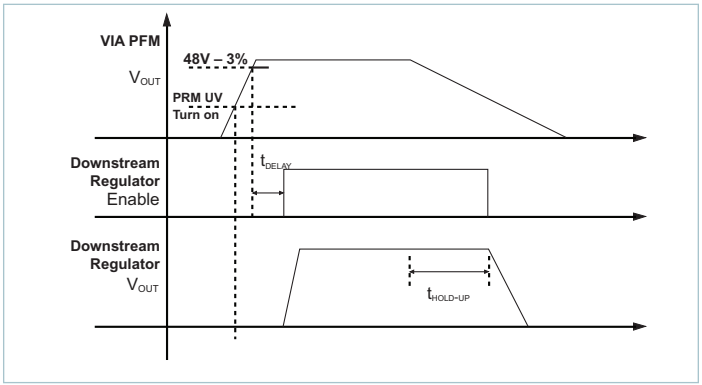


Figure 23 — *PRM enable hold-off waveforms*

Special care should be taken when enabling the constant-power load near the auto-ranger threshold, especially with an inductive source upstream of the PFM in a VIA package. A load current spike may cause a large input voltage transient, resulting in a range change which could temporarily reduce the available power (see Adaptive Cell Topology below).

Adaptive Cell™ Topology

The Adaptive Cell topology utilizes magnetically coupled "top" and "bottom" primary cells that are adaptively configured in series or parallel by a configuration controller comprised of an array of switches. A microcontroller monitors operating conditions and defines the configuration of the top and bottom cells through a range control signal.

A comparator inside the microcontroller monitors the line voltage and compares it to an internal voltage reference.

If the input voltage of the PFM crosses above the positive going cell reconfiguration threshold voltage, the top cell and bottom cell configure in series and the unit operates in "high" range.

These transitions between low and high range are controlled by software to respond only to input voltage transients. Longer term input voltage changes are subject to time limits and varying UVLO limits, as described on page 16, Ruggedized Auto Range Functionality.

Power processing is held off while transitioning between ranges and the output voltage of the unit may temporarily droop. External output hold up capacitance should be sized to support power delivery to the load during cell reconfiguration. The minimum specified external output capacitance is sufficient to provide adequate ride-through during cell reconfiguration for typical applications. Waveforms showing active cell reconfiguration can be seen in Figure 9.

Dielectric Withstand

The chassis of the PFM is required to be connected to Protective Earth when installed in the end application and must satisfy the requirements of IEC 60950-1 for Class I products. Protective earthing can be accomplished through dedicated wiring harness (example: ring terminal clamped by mounting screw).

The PFM contains an internal safety approved isolating component (ChiP™) that provides the Reinforced Insulation from Input to Output. The isolating component is individually tested for Reinforced Insulation from Input to Output at $3000V_{AC}$ or $4242V_{DC}$ prior to the final assembly of the PFM in a VIA package.

Summary

The final package assembly contains basic insulation from input to case, reinforced insulation from input to output, and functional insulation from output to case.

The output of the PFM in a VIA package complies with the requirements of SELV circuits so only functional insulation is required from the output (SELV) to case (PE) because the case is required to be connected to protective earth in the final installation.

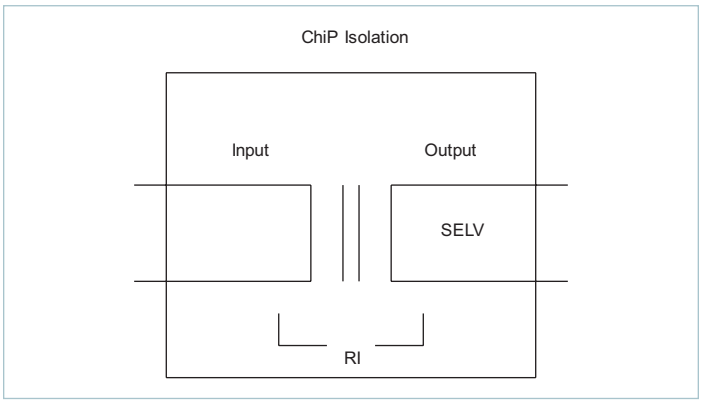


Figure 24 — *PFM in a ChiP™ package before final assembly in the VIA package*

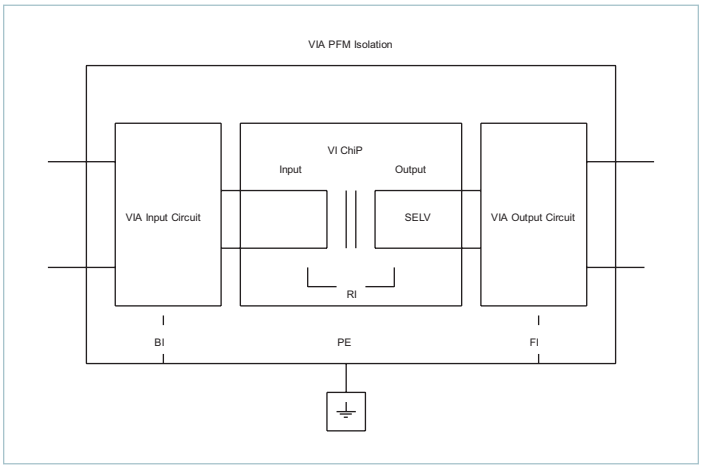
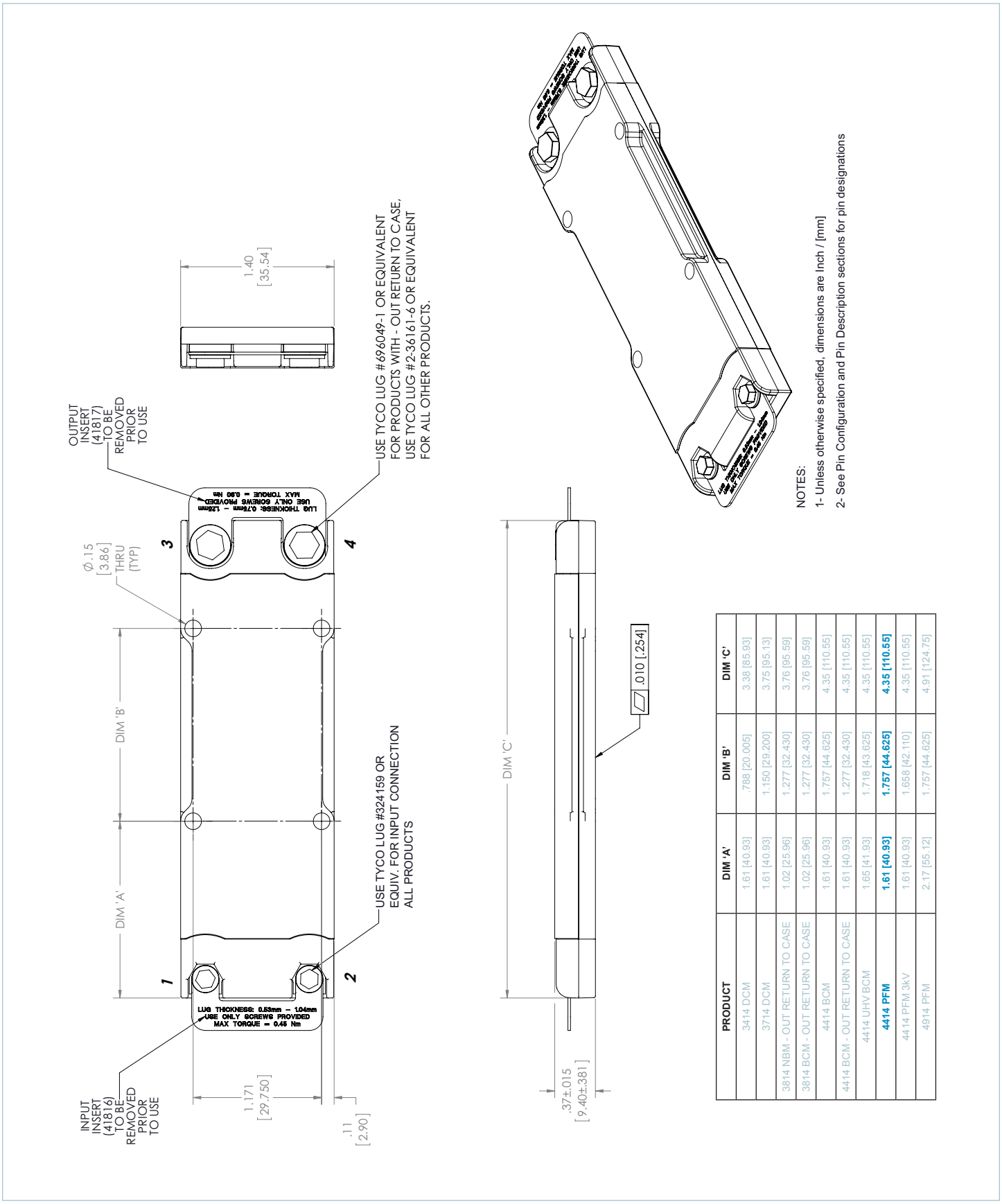


Figure 25 — *PFM in a VIA package after final assembly*

PFM in a VIA Package Chassis-Mount Package Mechanical Drawing

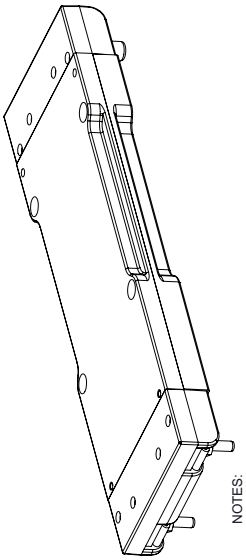


PRODUCT	DIM 'A'	DIM 'B'	DIM 'C'
3414 DCM	1.61 [40.93]	.788 [20.005]	3.38 [85.93]
3714 DCM	1.61 [40.93]	1.150 [29.200]	3.75 [95.13]
3814 NBM - OUT RETURN TO CASE	1.02 [25.96]	1.277 [32.430]	3.76 [95.59]
3814 BCM - OUT RETURN TO CASE	1.02 [25.96]	1.277 [32.430]	3.76 [95.59]
4414 BCM	1.61 [40.93]	1.757 [44.625]	4.35 [110.55]
4414 BCM - OUT RETURN TO CASE	1.61 [40.93]	1.277 [32.430]	4.35 [110.55]
4414 UHV BCM	1.65 [41.93]	1.718 [43.625]	4.35 [110.55]
4414 PFM	**1.61 [40.93]**	**1.757 [44.625]**	**4.35 [110.55]**
4414 PFM 3kV	1.61 [40.93]	1.658 [42.110]	4.35 [110.55]
4914 PFM	2.17 [55.12]	1.757 [44.625]	4.91 [124.75]

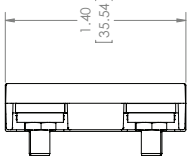
Product outline drawing; product outline drawings are available in .pdf and .dxf formats.
3D mechanical models are available in .pdf and .step formats.

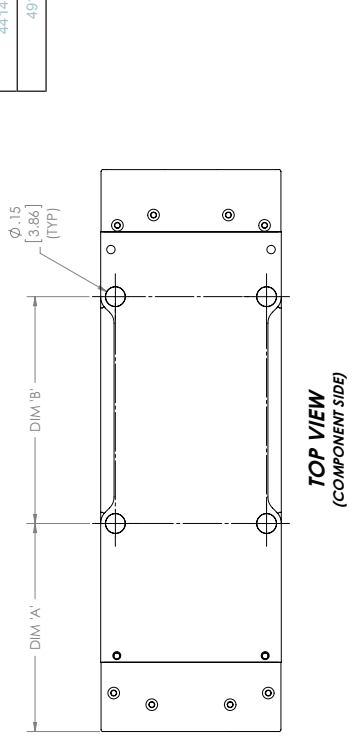
PFM in a VIA Package PCB-Mount Package Mechanical Drawing

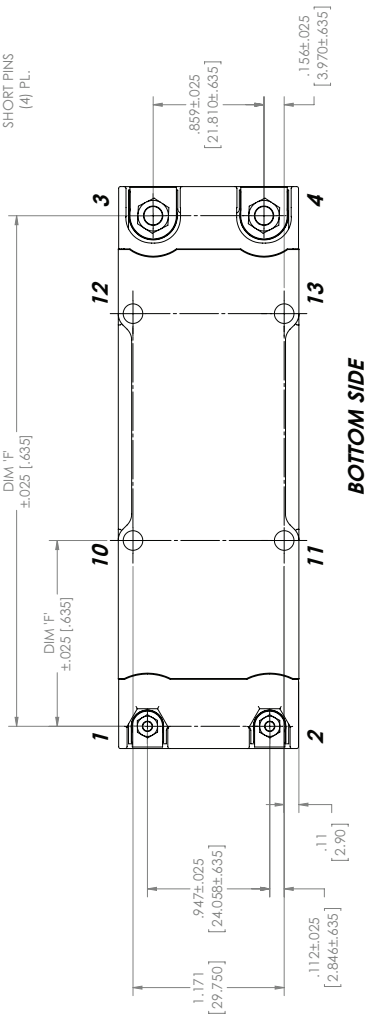
PRODUCT	DIM 'A'	DIM 'B'	DIM 'C'	DIM 'D'	DIM 'F'
3414 DCM	1.61 [40.93]	.788 [20.005]	3.38 [85.93]	2.988 [75.897]	1.439 [36.554]
3714 DCM	1.61 [40.93]	1.150 [29.200]	3.75 [95.13]	3.350 [85.092]	1.439 [36.554]
4414 BCM	1.61 [40.93]	1.757 [44.625]	4.35 [110.55]	3.957 [100.517]	1.439 [36.554]
4414 UHV BCM	1.65 [41.93]	1.718 [43.625]	4.35 [110.55]	3.957 [100.517]	1.479 [37.554]
4414 PFM	**1.61 [40.93]**	**1.757 [44.625]**	**4.35 [110.55]**	**3.957 [100.517]**	**1.439 [36.554]**
4414 PFM 3kV	1.61 [40.93]	1.658 [42.110]	4.35 [110.55]	3.957 [100.517]	1.439 [36.554]
4914 PFM	2.17 [55.12]	1.757 [44.625]	4.91 [124.75]	4.517 [114.741]	1.999 [50.777]



NOTES:
1- Unless otherwise specified, dimensions are Inch [mm]
2- See Pin Configuration and Pin Description sections for pin designations

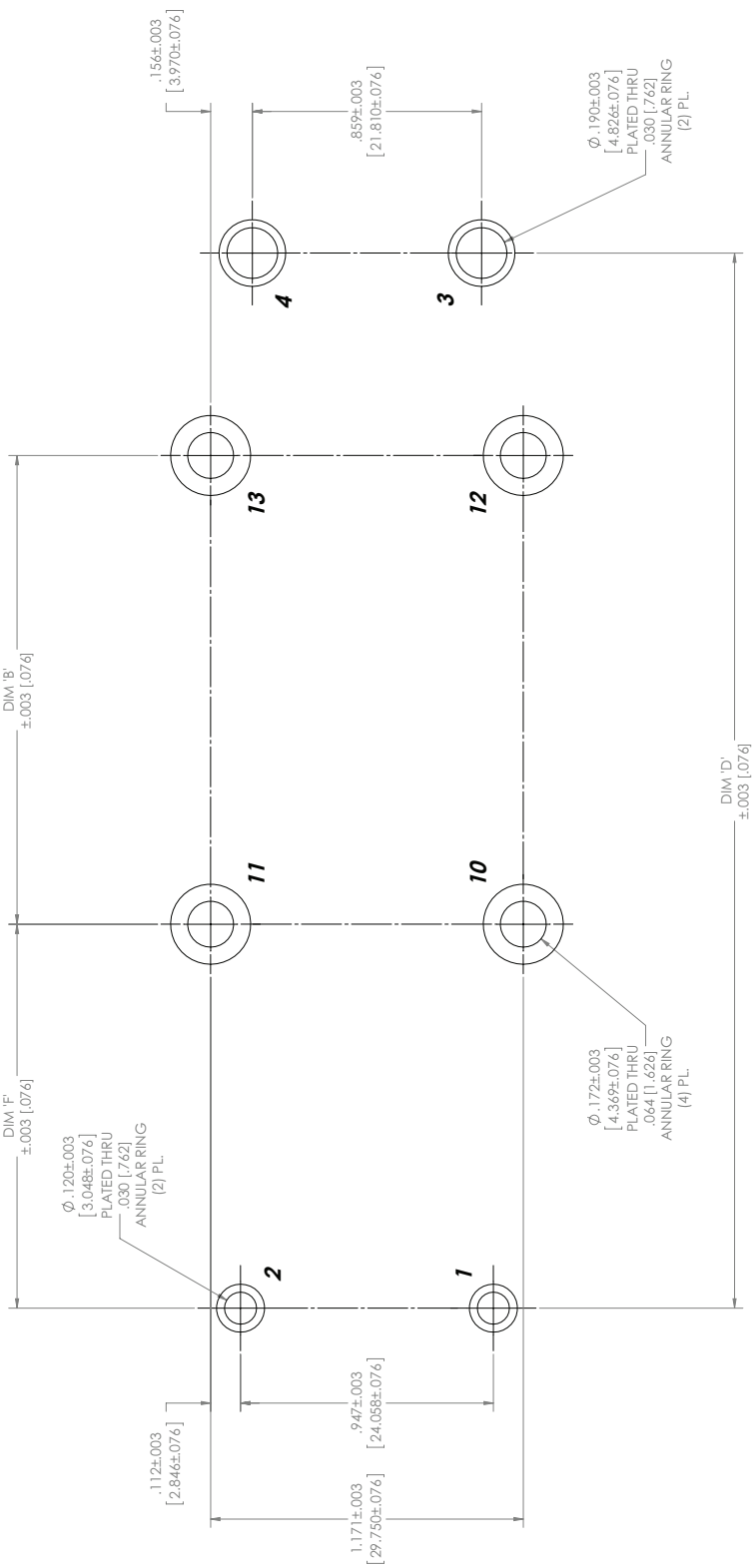






PFM in a VIA Package PCB-Mount Package Recommended Land Pattern

PRODUCT	DIM 'A'	DIM 'B'	DIM 'C'	DIM 'D'	DIM 'F'
3414 DCM	1.61 [40.93]	.788 [20.005]	3.38 [85.93]	2.988 [75.897]	1.439 [36.554]
3714 DCM	1.61 [40.93]	1.150 [29.200]	3.75 [95.13]	3.350 [85.092]	1.439 [36.554]
4414 BCM	1.61 [40.93]	1.757 [44.625]	4.35 [110.55]	3.957 [100.517]	1.439 [36.554]
4414 UHV BCM	1.65 [41.93]	1.718 [43.625]	4.35 [110.55]	3.957 [100.517]	1.479 [37.554]
4414 PFM	**1.61 [40.93]**	**1.757 [44.625]**	**4.35 [110.55]**	**3.957 [100.517]**	**1.439 [36.554]**
4414 PFM 3kV	1.61 [40.93]	1.658 [42.110]	4.35 [110.55]	3.957 [100.517]	1.439 [36.554]
4914 PFM	2.17 [55.12]	1.757 [44.625]	4.91 [124.75]	4.517 [114.741]	1.999 [50.777]



RECOMMENED HOLE PATTERN
(COMPONEBT SIDE)

NOTES:
1- Unless otherwise specified, dimensions are Inch [mm]
2- See Pin Configuration and Pin Description sections for pin designations

Revision History

Revision	Date	Description	Page Number(s)
1.0	05/21/18	Initial release	n/a
1.1	08/31/18	Updated mechanical specifications Updated mechanical drawings	13 21 – 23

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