

Circuits from the Lab™ Reference Circuits

Circuits from the Lab™ reference circuits are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0241.

Devices Connected/Referenced

ADA4096-2	30 V, Micropower, Overvoltage Protection, Rail-to-Rail Input/Output Amplifier
AD7920	250 kSPS, 12-bit, 250 kSPS ADC in 6-Lead SC70
ADP3336	High Accuracy Ultralow I _Q 500 mA anyCAP® Adjustable Low Dropout Linear Regulator

High-Side Current Sensing with Input Overvoltage Protection

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

[CN-0241 Circuit Evaluation Board \(EVAL-CN0241-SDPZ\)](#)
[System Demonstration Platform \(EVAL-SDP-CB1Z\)](#)

Design and Integration Files

[Schematics, Layout Files, Bill of Materials](#)

CIRCUIT FUNCTION AND BENEFITS

High-side current monitors are likely to encounter overvoltage conditions from transients or when the monitoring circuits are connected, disconnected, or powered down. This circuit, shown

in Figure 1, uses the overvoltage protected [ADA4096-2](#) op amp connected as a difference amplifier to monitor the high-side current. The [ADA4096-2](#) has input overvoltage protection, without phase reversal or latch-up, for voltages of 32 V higher than and lower than the supply rails.

The circuit is powered by the [ADP3336](#) adjustable low dropout 500 mA linear regulator, which can also be used to supply power to other parts of the system, if desired. Its input voltage can range from 5.2 V to 12 V when set for a 5 V output. To save power, the current sensing circuit can be powered down by removing power to the [ADP3336](#); however, the power source, such as a solar panel, can still operate.

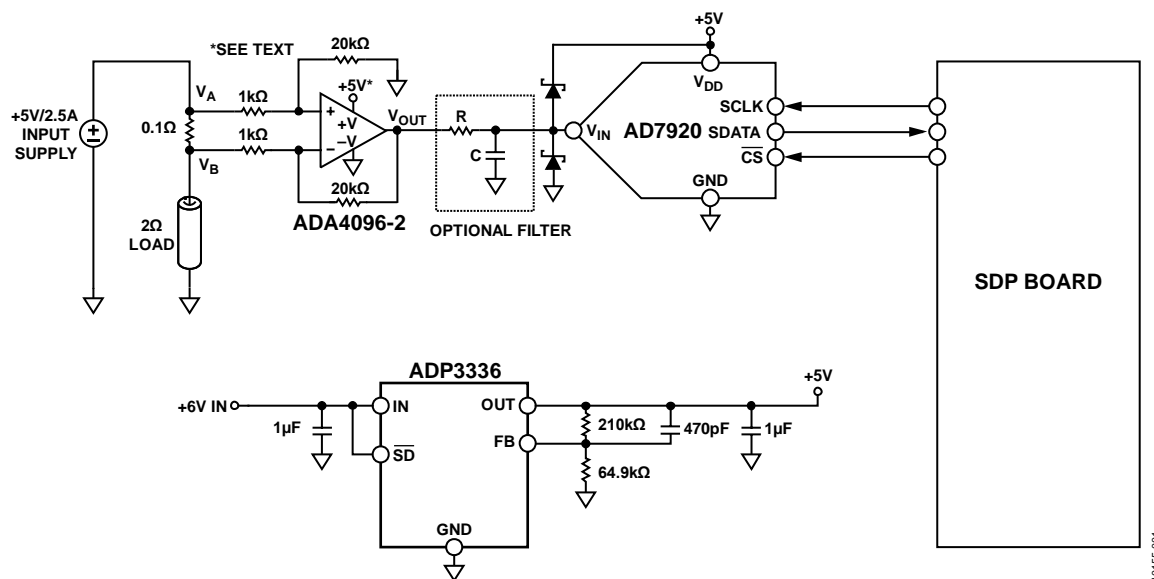


Figure 1. High-Side Current Sensing with Input Overvoltage Protection (Simplified Schematic: All Connections and Decoupling Not Shown)

Rev. A

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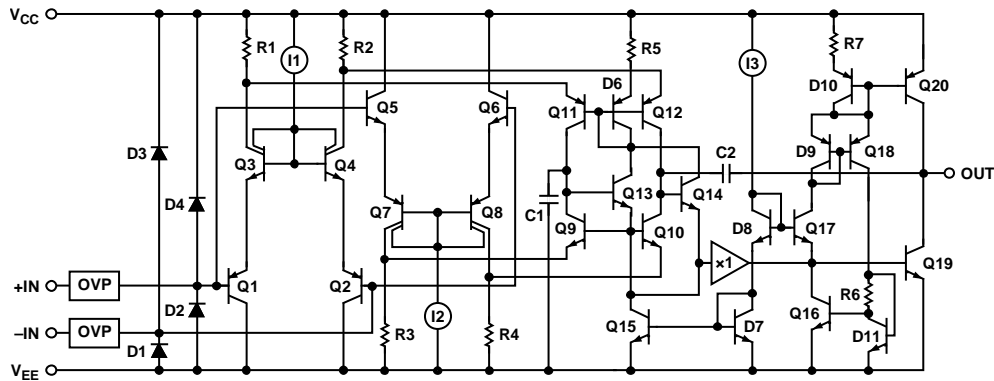


Figure 2. ADA4096-2 Simplified Schematic

This applies voltage to the inputs of the unpowered ADA4096-2; however, no latch-up or damage occurs for input voltages up to 32 V. If slower throughput rates are required, the AD7920 can also be powered down between samples. The AD7920 draws a maximum of 5 μ W when powered down and 15 mW when powered up. The ADA4096-2 requires only 120 μ A under operational conditions. When operating at 5 V, this is only 0.6 mW. The ADP3336 draws only 1 μ A in the shutdown mode.

CIRCUIT DESCRIPTION

The circuit is a classic high-side current sensing circuit topology with a single sense resistor. The other four resistors (dual 1 k Ω /20 k Ω divider) are in a thin film network (for ratio matching) and are used to set the difference amplifier gain. This amplifies the difference between the two voltages seen across the sense resistor and rejects the common-mode voltage.

$$V_{OUT} = (V_A - V_B) (20 \text{ k}\Omega / 1 \text{ k}\Omega)$$

Figure 2 shows a simplified schematic of the ADA4096-2. The input stage comprises two differential pairs (Q1 to Q4 and Q5 to Q8) operating in parallel. When the input common-mode voltage approaches $V_{CC} - 1.5$ V, Q1 to Q4 shut down as I1 reaches its minimum voltage compliance. Conversely, when the input common-mode voltage approaches $V_{EE} + 1.5$ V, Q5 to Q8 shut down as I2 reaches its minimum voltage compliance. This topology allows for maximum input dynamic range because the amplifier can function with its inputs at 200 mV outside the rail (at room temperature).

As with any rail-to-rail input amplifier, V_{OS} mismatch between the two input pairs determines the CMRR of the amplifier. If the input common-mode voltage range is within 1.5 V of each rail, transitions between the input pairs are avoided, thus improving the CMRR by approximately 10 dB.

The ADA4096-2 inputs are protected from input voltage excursions up to 32 V outside each rail. This feature is of particular importance in applications with power supply sequencing issues that can cause the signal source to be active before the supplies to the amplifier are applied.

Figure 3 shows the input current limiting capability of the ADA4096-2 provided by low $R_{DS(ON)}$ internal series FETs (green curves) compared to using a 5 k Ω external series resistor with an unprotected op amp (red curves).

Figure 3 was generated with the ADA4096-2 in a unity-gain buffer configuration with the supplies connected to GND (or ± 15 V) and the positive input swept until it exceeds the supplies by 32 V. In general, input current is limited to 1 mA during positive overvoltage conditions and 200 μ A during negative undervoltage conditions. For example, at an overvoltage of 20 V, the ADA4096-2 input current is limited to 1 mA, providing a current limit equivalent to a series 20 k Ω resistor.

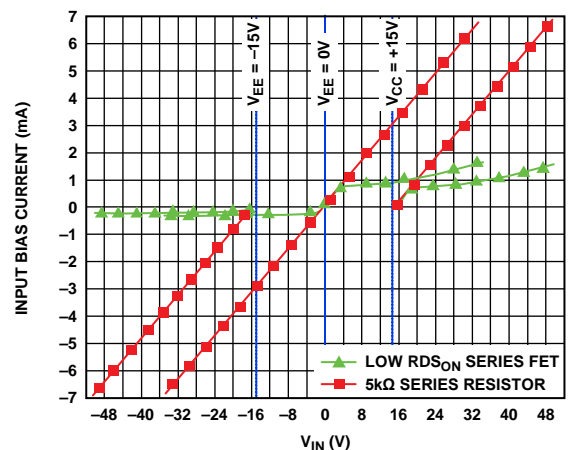


Figure 3. Input Current Limiting Capability

Figure 3 also shows that the current limiting circuitry is active whether the amplifier is powered or not.

Figure 3 represents input protection under abnormal conditions only. The correct amplifier operation input voltage range (IVR) is specified in Table 2 to Table 4 of the ADA4096-2 data sheet.

The AD7920 is a 12-bit, high speed, low power, successive approximation ADC. The part operates from a single 2.35 V to 5.25 V power supply and features throughput rates up to 250 kSPS. The part contains a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 13 MHz.

The conversion process and data acquisition are controlled using $\overline{\text{CS}}$ and the serial clock, SCLK, allowing the devices to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{\text{CS}}$, and the conversion is initiated at this point. There are no pipeline delays associated with the part.

The AD7920 uses advanced design techniques to achieve very low power dissipation at high throughput rates.

To enter power-down mode, the conversion process must be interrupted by bringing $\overline{\text{CS}}$ high anywhere after the second falling edge of SCLK, and before the tenth falling edge of SCLK. Once $\overline{\text{CS}}$ is brought high in this window of SCLKs, the part enters power-down mode, the conversion that was initiated by the falling edge of $\overline{\text{CS}}$ is terminated, and SDATA goes back into three-state. If $\overline{\text{CS}}$ is brought high before the second SCLK falling edge, the part remains in normal mode and does not power down. This avoids accidental power down due to glitches on the $\overline{\text{CS}}$ line.

To exit this mode of operation and power up the AD7920 again, a dummy conversion is performed. On the falling edge of $\overline{\text{CS}}$, the device begins to power up and continues to power up as long as $\overline{\text{CS}}$ is held low until after the falling edge of the tenth SCLK. The device is fully powered up once 16 SCLKs have elapsed, and valid data results from the next conversion.

If $\overline{\text{CS}}$ is brought high before the tenth SCLK falling edge, the AD7920 goes back into power-down mode again. This avoids accidental power up due to glitches on the $\overline{\text{CS}}$ line or an inadvertent burst of eight SCLK cycles while $\overline{\text{CS}}$ is low. Although the device can begin to power up on the falling edge of $\overline{\text{CS}}$, it powers down again on the rising edge of $\overline{\text{CS}}$ as long as it occurs before the tenth SCLK falling edge.

Further details regarding the timing can be found in the AD7920 data sheet.

Test Results

An important measure of the performance of the circuit is the amount of noise in the final output voltage measurement.

Figure 4 shows a histogram of 10,000 measurement samples. This data was taken with the CN-0241 Evaluation Board connected to the EVAL-SDP-CB1Z SDP-B evaluation board. Details of the setup are described in the Circuit Evaluation and Test section.

The power supply was set to 3.0 V, and 10,000 samples of data were acquired at the maximum rate of 250 kSPS without having turned the output of the LDO off. Figure 4 shows the results of this acquisition. The peak-to-peak noise is approximately 2 LSBs, corresponding to about 0.3 LSB rms.

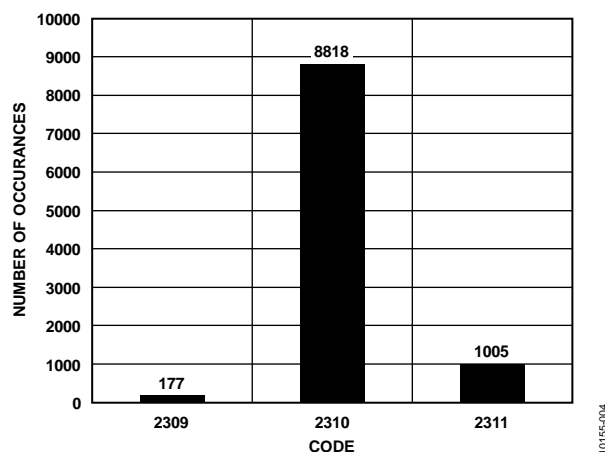


Figure 4. Histogram of Codes for 10,000 Samples Before Power Down

The $\overline{\text{SD}}$ shutdown pin connected to the ADP3336 was then asserted low in the software causing the output of the LDO to turn off. After approximately 1 minute, the shutdown pin on the ADP3336 was then asserted high, turning the output back on, and the same number of data samples were acquired. Figure 5 shows the results of this acquisition.

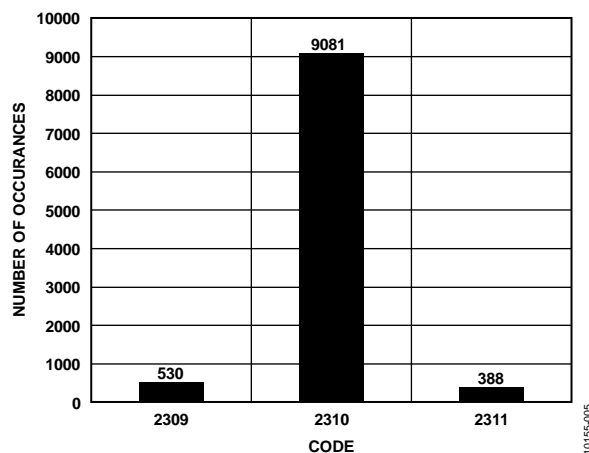


Figure 5. Histogram of Codes for 10,000 Samples After Power Down

Figure 5 shows that the output of the ADA4096-2 did not latch during power down when the input was held high.

A complete design support package for this circuit note can be found at www.analog.com/CN0241-DesignSupport.

COMMON VARIATIONS

The circuit is proven to work with good stability and accuracy. This board is also compatible with the SDP-S controller board (EVAL-SDP-CS1Z).

A slight modification to the circuit shown in Figure 1 allows monitoring the current for input supply voltages up to 30 V. Rather than connect the +V pin of the ADA4096-2 to 5 V from the ADP3336, connect it directly to the input supply being monitored. In this configuration, the ADA4096-2 is powered directly from the input supply.

CIRCUIT EVALUATION AND TEST

This circuit uses the [EVAL-CN0241-SDPZ](#) circuit board and the [EVAL-SDP-CB1Z](#) SDP-B controller board. The two boards have 120-pin mating connectors, allowing for the quick setup and evaluation of the performance of the circuit. The [EVAL-CN0241-SDPZ](#) board contains the circuit to be evaluated, as described in this note, and the SDP-B controller board is used with the CN0241 evaluation software to capture the data from the [EVAL-CN0241-SDPZ](#) circuit board.

Equipment Needed

The following equipment is needed:

- A PC with a USB port and Windows® XP, Windows Vista®, or Windows® 7 (32-bit)
- [EVAL-CN0241-SDPZ](#) circuit evaluation board
- [EVAL-SDP-CB1Z](#) SDP-B controller board
- CN0241 SDP evaluation software
- DC power supply capable of driving 6 V/1 A
- DC power supply capable of driving 5 V/2.5 A
- 2 Ω /12 W load resistor

Getting Started

Load the evaluation software by placing the CN0241 evaluation software CD in the CD drive of the PC. Using **My Computer**, locate the drive that contains the evaluation software.

Functional Block Diagram

See Figure 1 of this circuit note for the circuit block diagram and the EVAL-CN0241-SDPZ-SCH-RevA.pdf file for the circuit schematics. This file is contained in the [CN0241 Design Support Package](#).

Setup

Connect the 120-pin connector on the [EVAL-CN0241-SDPZ](#) circuit board to the CON A connector on the [EVAL-SDP-CB1Z](#) controller (SDP-B) board. Use Nylon hardware to firmly secure the two boards, using the holes provided at the ends of the 120-pin connectors. With power to the supply off, connect a 6 V power supply to the +6 V and GND pins on the board. If available, a 6 V wall wart can be connected to the barrel connector on the board and used in place of the 6 V power supply. Connect the USB cable supplied with the SDP-B board to the USB port on the PC. Do not connect the USB cable to the mini-USB connector on the SDP-B board at this time.

Connect the 5 V/2.5 A dc supply to +VIN and GND on J1 of the [EVAL-CN0241-SDPZ](#) board. Connect the 2 Ω /12 W load resistor to LOAD and GND of the [EVAL-CN0241-SDPZ](#) board.

Test

Apply power to the 6 V supply (or wall wart) connected to the [EVAL-CN0241-SDPZ](#) circuit board. Launch the evaluation software and connect the USB cable from the PC to the USB miniconnector on the SDP-B board.

Once USB communications are established, the SDP-B board can be used to send, receive, and capture serial data from the [EVAL-CN0241-SDPZ](#) board.

Turn the 5 V/2.5 A dc supply on when data is ready to be acquired. Adjust the voltage output accordingly to output the amount of current needed to be measured.

Figure 6 shows a screenshot of the CN0241 SDP evaluation software interface, and Figure 7 shows a screenshot of the [EVAL-CN0241-SDPZ](#) evaluation board. Information regarding the SDP-B board can be found in the [SDP-B User Guide](#).

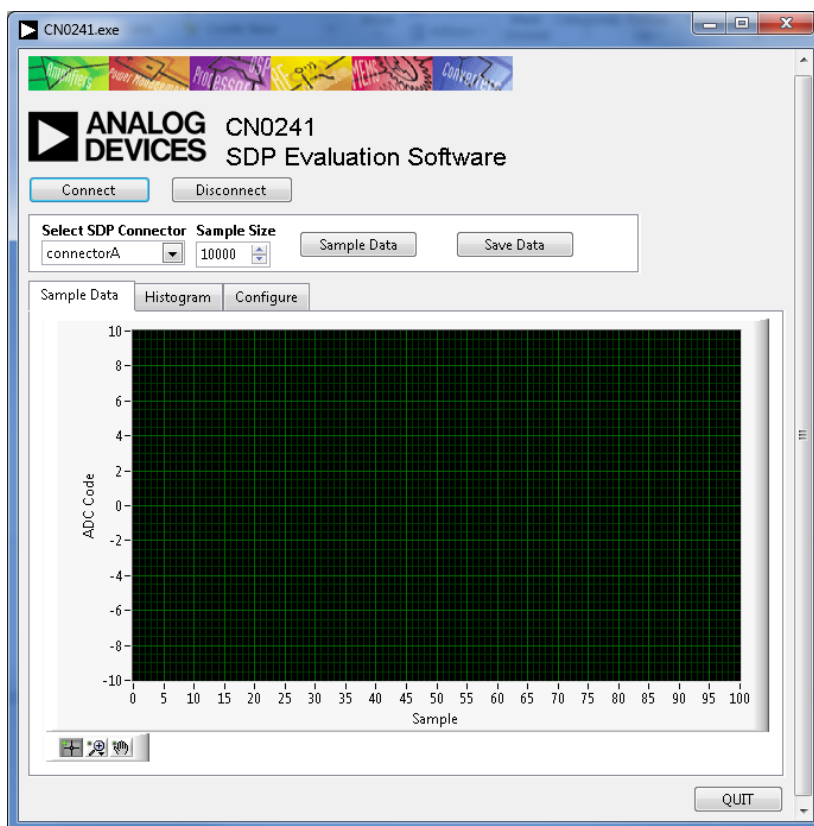


Figure 6. CN-0241 SDP Evaluation Software Interface

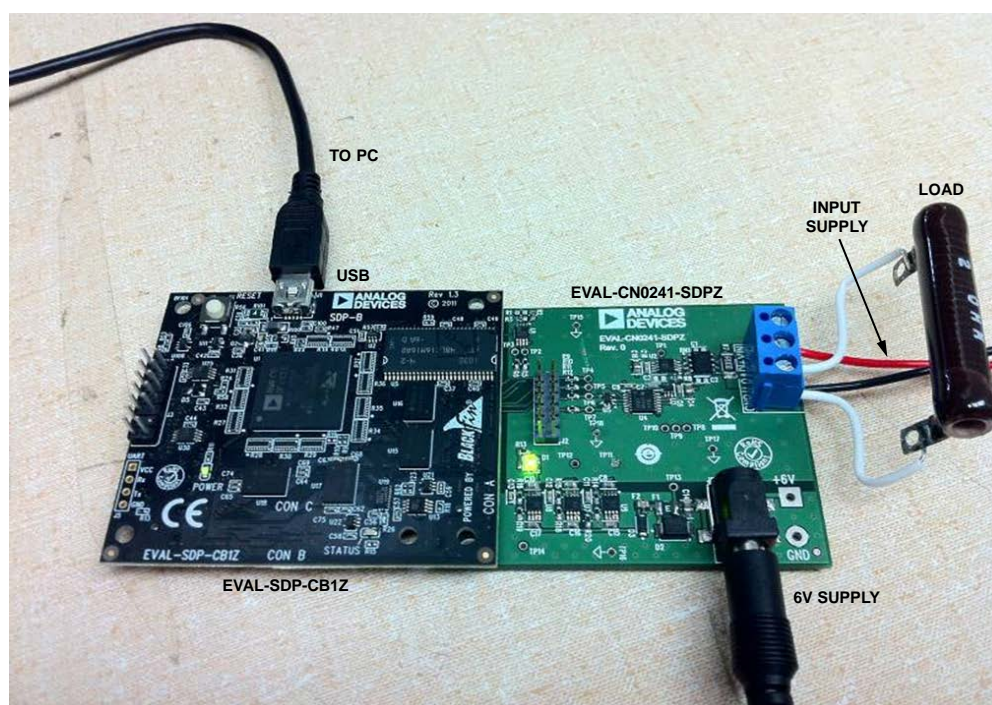


Figure 7. EVAL-CN0241-SDPZ Evaluation Board Connected to the SDP Board

LEARN MORE

CN0241 Design Support Package:

<http://www.analog.com/CN0241-DesignSupport>

SDP-B User Guide

Ardizzoni, John. *A Practical Guide to High-Speed Printed-Circuit-Board Layout*, Analog Dialogue 39-09, September 2005.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-035, *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues*, Analog Devices.

MT-036 Tutorial, *Op Amp Output Phase-Reversal and Input Over-Voltage Protection*, Analog Devices.

MT-068 Tutorial, *Difference and Current Sense Amplifiers*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Data Sheets and Evaluation Boards

[CN-0241 Circuit Evaluation Board \(EVAL-CN0241-SDPZ\)](#)

[System Demonstration Platform \(EVAL-SDP-CB1Z\)](#)

[ADA4096-2 Data Sheet](#)

[AD7920 Data Sheet](#)

[ADP3336 Data Sheet](#)

REVISION HISTORY

5/12—Rev. 0 to Rev. A

Changes to Circuit Function and Benefits Section and Figure 11

Changes to Figure 6.....5

1/12—Revision 0: Initial Version

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