

Power Amplifier 10.0 - 15.35 GHz

Rev. V2

Features

- Fully Integrated Power Amplifier
- Wide Bandwidth 10.0 - 15.35 GHz
- 30 dB Small Signal Gain
- 40 dBm Third Order Intercept Point (OIP3)
- 31 dBm Output P1dB
- Integrated Power Detector
- Bias Voltage 5 V, 1.3 A
- Lead-Free 5 mm 24-lead QFN Package
- RoHS* Compliant

Description

The MAAP-110150 is a packaged linear power amplifier that operates over the range 10.0 - 15.35 GHz. The device typically provides 30 dB of gain and 40 dBm OIP3 with more than 31 dBm of output P1dB.

This power amplifier is assembled in a lead free, fully molded 5 mm QFN package and consists of a 3 stage power amplifier with integrated, on-chip peak power detector and envelope detector. The device includes on-chip ESD protection structures and DC by-pass capacitors to ease the implementation and volume assembly.

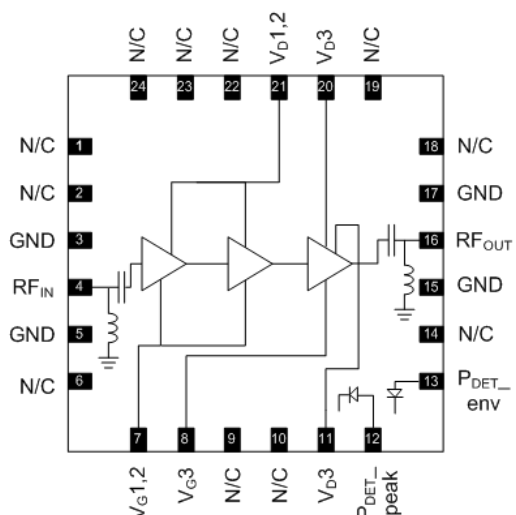
The device is well suited for use in the 10, 11, 13, 15 GHz cellular backhaul applications.

Ordering Information^{1,2}

Part Number	Package
MAAP-110150	Bulk
MAAP-110150-TR0500	Tape and Reel
MAAP-110150-001SMB	Sample Board

1. Reference Application Note M513 for reel size information.
2. All sample boards include 5 loose parts.

Functional Schematic



Pin Configuration^{3,4}

Pin No.	Function	Pin No.	Function
1	No Connection	13	Envelope Power Detector
2	No Connection	14	No Connection
3	Ground	15	Ground
4	RF Input	16	RF Output
5	Ground	17	Ground
6	No Connection	18	No Connection
7	Gate Voltage 1,2	19	No Connection
8	Gate Voltage 3	20	Drain Voltage 3
9	No Connection	21	Drain Voltage 1,2
10	No Connection	22	No Connection
11	Drain Voltage 3	23	No Connection
12	Peak Power Detector	24	No Connection

3. MACOM recommends connecting unused package pins to ground.
4. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

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Electrical Specifications:

Freq. = 10.0 - 15.35 GHz, $I_{DQ} = 1.3$ A, $T_A = 25^\circ\text{C}$, $V_D = 5$ V, $Z_0 = 50$ Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	10.00 - 10.30 GHz	dB	—	30.75	—
	10.30 - 11.70 GHz		27.0	31.00	
	12.75 - 13.25 GHz		27.0	30.00	
	14.50 - 15.35 GHz		27.0	31.00	
P1dB, @ 1 dB Compression	10.00 - 10.30 GHz	dBm	—	31.50	—
	10.30 - 11.70 GHz			31.75	
	12.75 - 13.25 GHz			31.75	
	14.50 - 15.35 GHz			31.50	
P_{SAT}	10.00 - 10.30 GHz	dBm	—	34.25	—
	10.30 - 11.70 GHz		32.5	34.50	
	12.75 - 13.25 GHz		32.5	34.00	
	14.50 - 15.35 GHz		31.5	33.50	
OIP3	10.00 - 10.30 GHz	dBm	—	40.50	—
	10.30 - 11.70 GHz		38.0	41.00	
	12.75 - 13.25 GHz		38.0	40.00	
	14.50 - 15.35 GHz		35.5	37.50	
Input Return Loss	—	dB	—	12	—
Output Return Loss	—	dB	—	12	—
PAE, @ 1 dB Compression	—	%	—	20	—
Quiescent Current	—	mA	—	1300	—

Absolute Maximum Ratings^{5,6,7}

Parameter	Rating
Drain Voltage (V_D 1,2,3)	7 V
Gate Voltage (V_G 1,2,3)	-3 V
Drain to Gate Voltage ($V_D - V_G$)	10 V
Storage Temperature	-65°C to +150°C
Junction Temperature	+175°C

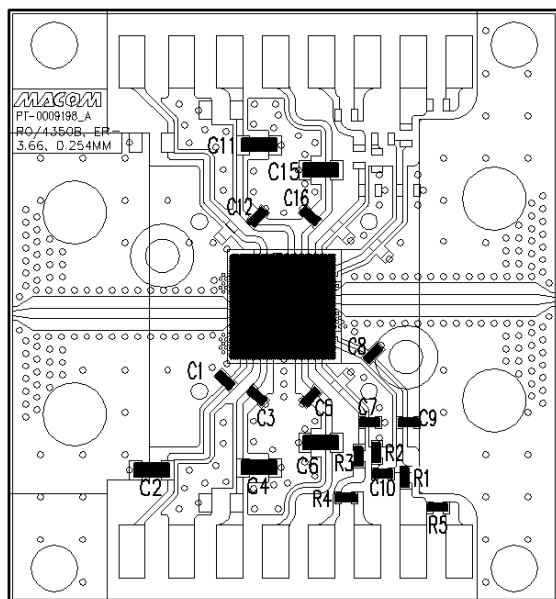
- Exceeding any one or combination of these limits may cause permanent damage to this device.
- MACOM does not recommend sustained operation near these survivability limits.
- Operating at nominal conditions with $T_J \leq +150^\circ\text{C}$ will ensure MTTF > 1×10^6 hours.

Maximum Operating Ratings^{8,9}

Parameter	Rating
P_{DISS}	10 W
Operating Temperature	-40°C to +85°C
Junction Temperature	+150°C

- Channel temperature directly affects device MTTF. Channel temperature should be kept as low as possible to maximize lifetime. Thermal resistance, Θ_{JC} is 9.2 °C/W.
- For saturated performance, it is recommended that the sum of $(2V_{DD} + \text{abs}(V_{GG})) < 15$ V.

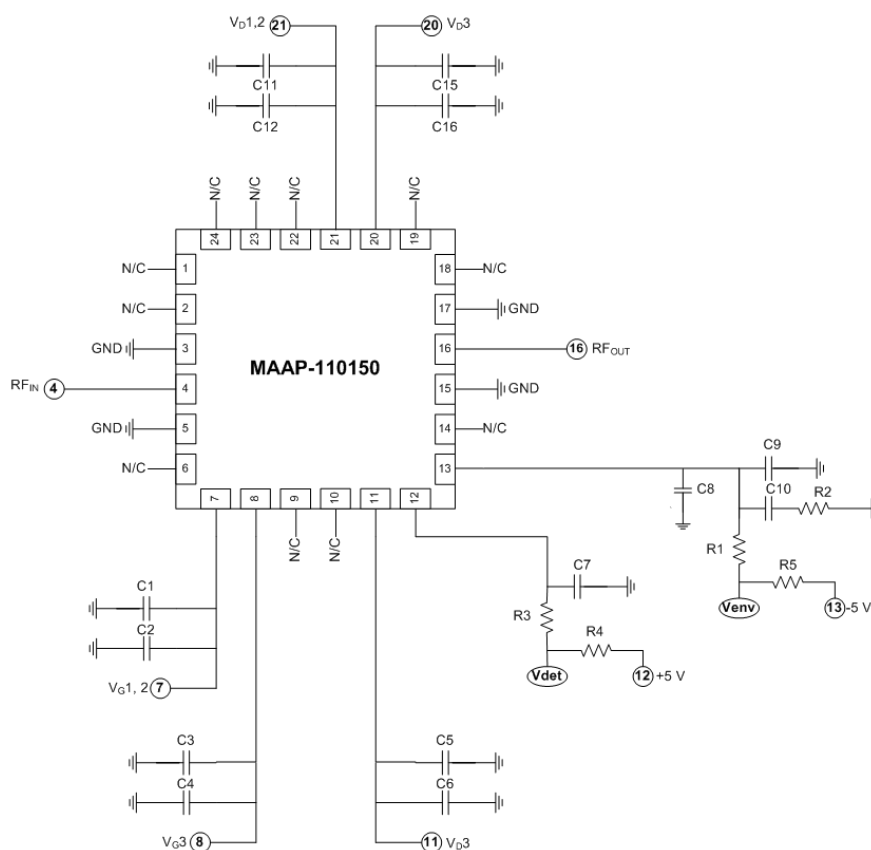
PCB Layout



Parts List

Part	Value	Case Style
C1,C3,C5,C7,C8,C9,C10,C12,C16	100 nF	0402
C2,C4,C6,C11,C15	4.7 μ F	0603
R1,R3	100 Ω	0402
R2	10 K Ω	0402
R4,R5	560 Ω	0402

Application Schematic



Biasing

All gates should be pinched-off, $V_G < -2$ V, before applying the drain voltage, $V_D = 5$ V (do not exceed maximum specified V_{DG} value of 10 V). Then the gate voltages can be increased until the desired quiescent drain current is reached in each stage. The recommended quiescent bias is $V_D = 5$ V, $I_{D12} + I_{D3} = 1300$ mA (total). The performance in this datasheet has been measured with a fixed gate voltage and no drain current regulation under large signal operation. It is also possible to regulate the drain current dynamically, to limit the DC power dissipation under RF drive. To turn off the device, the turn on bias sequence should be followed in reverse.

Detector Operation

MAAP-110150 includes a power and envelope detector. As per the application schematic, the power detector requires an external 5 V supply and the envelope detector requires -5 V. The output from the resistive voltage divider can be fed into a ADC or multimeter for the result.

Bias Arrangement

Each DC pin ($V_{D1,2}$, V_{D3} and $V_{G1,2}$, V_{G3}) needs to have bypass capacitance of 100 nF mounted as close to the packaged device as possible.

Handling Procedures

Please observe the following precautions to avoid damage:

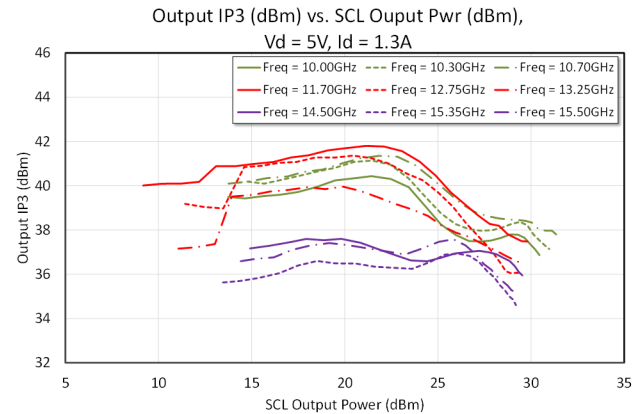
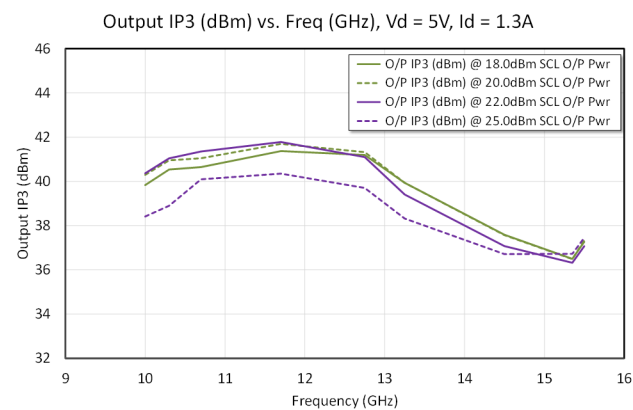
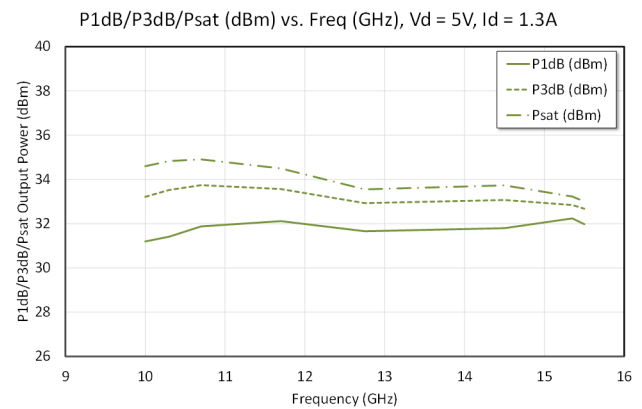
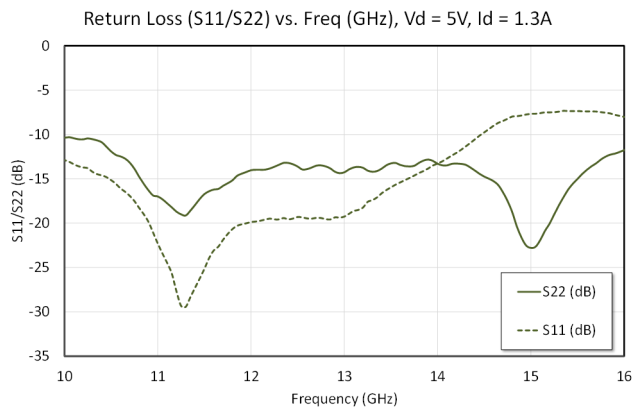
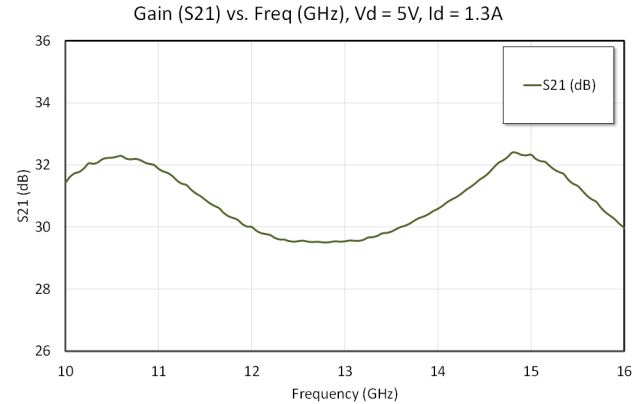
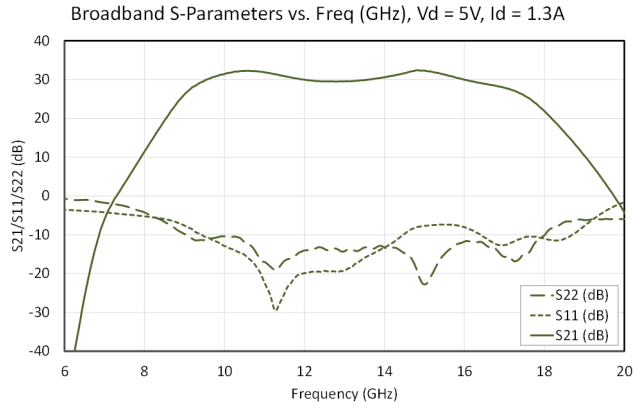
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these CDM class C1, HBM Class 0A devices.

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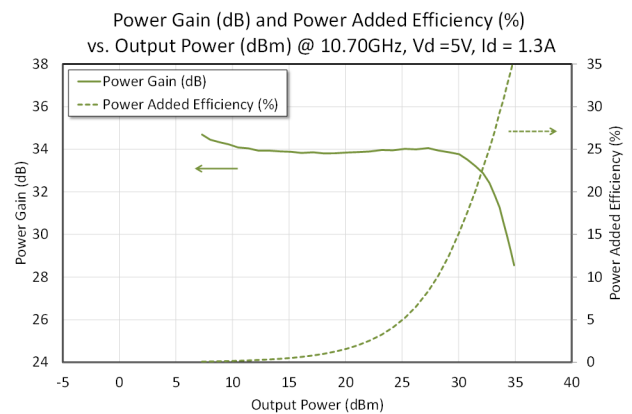
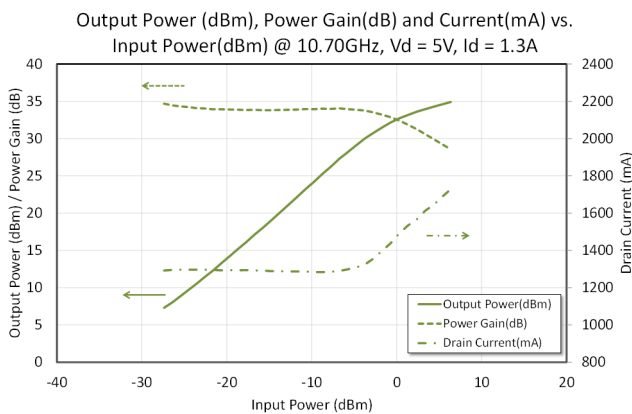
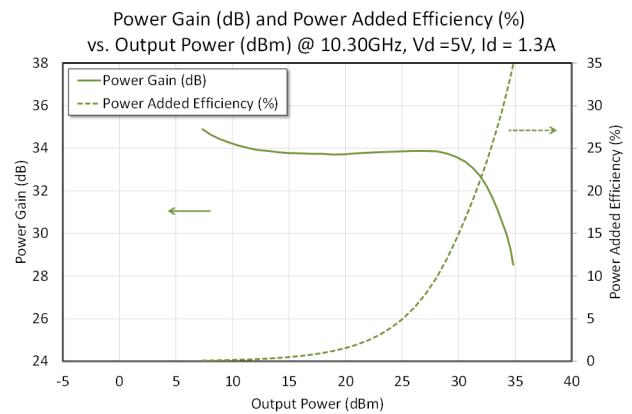
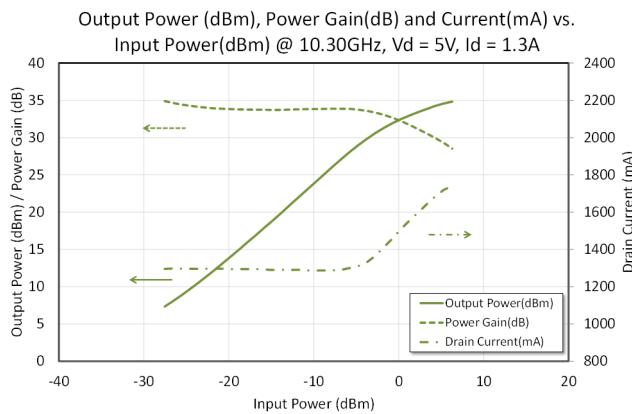
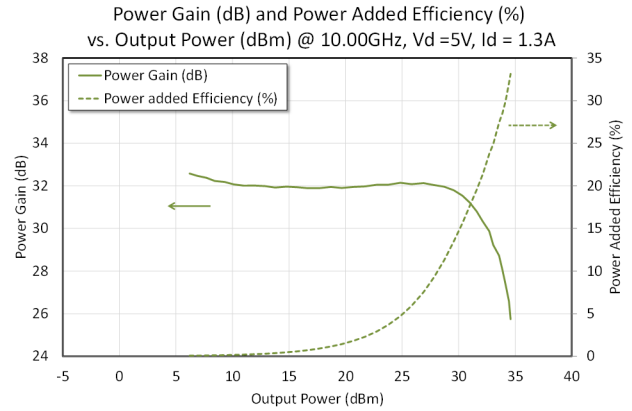
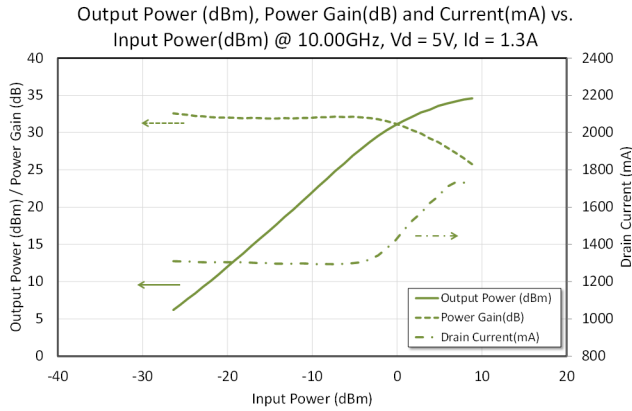
Typical Performance Curves: $V_D = 5\text{ V}$, $I_{DQ} = 1.3\text{ A}$, $V_G = -1.05 \sim -0.85\text{ V}$, $T_A = +25^\circ\text{C}$



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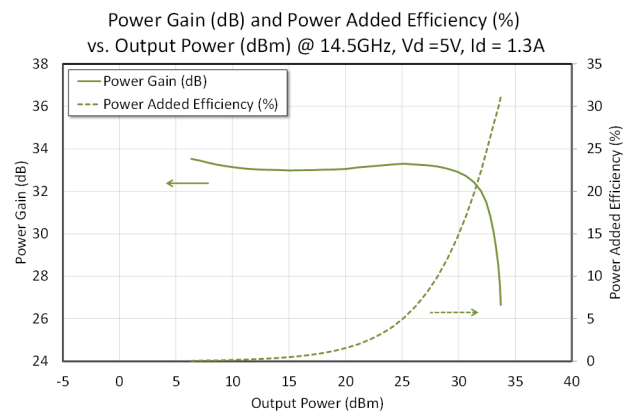
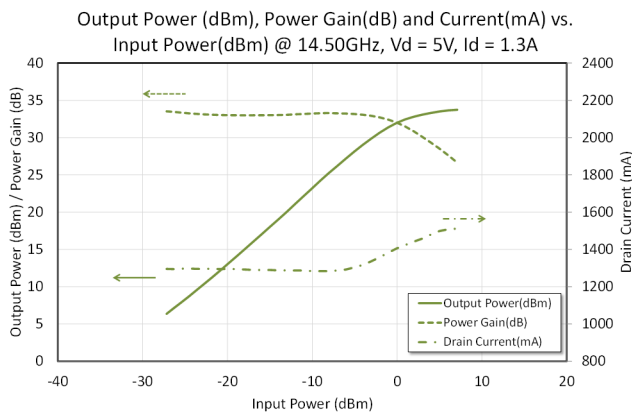
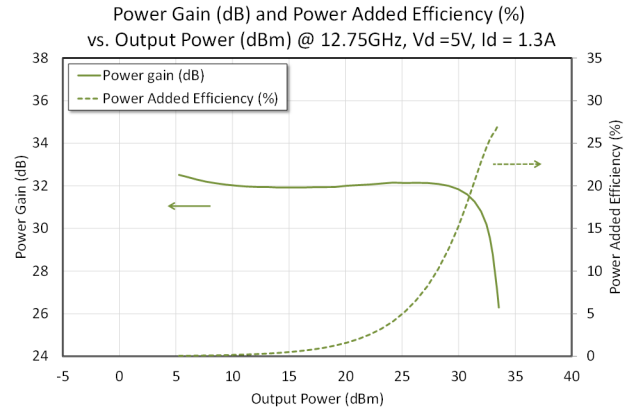
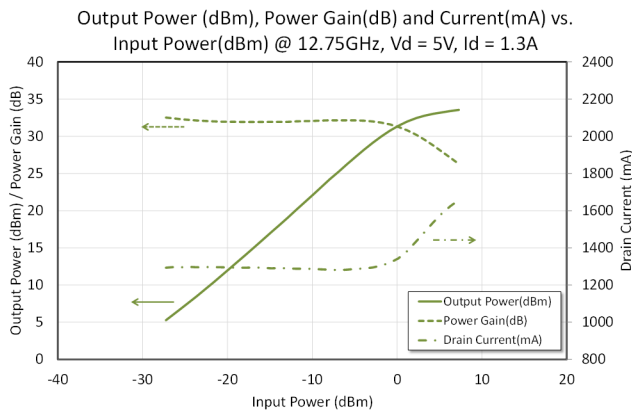
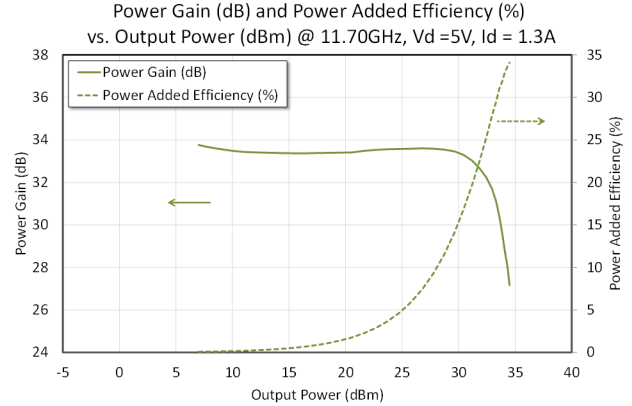
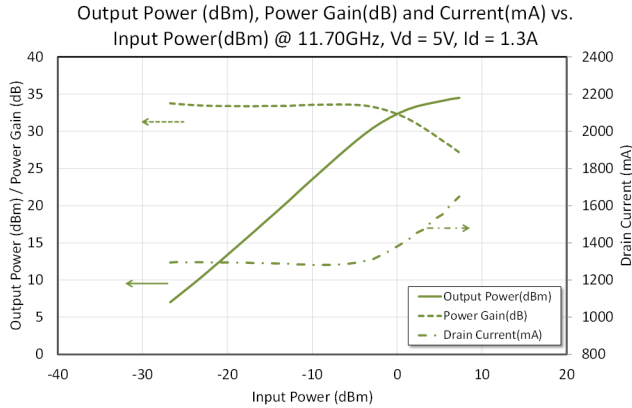
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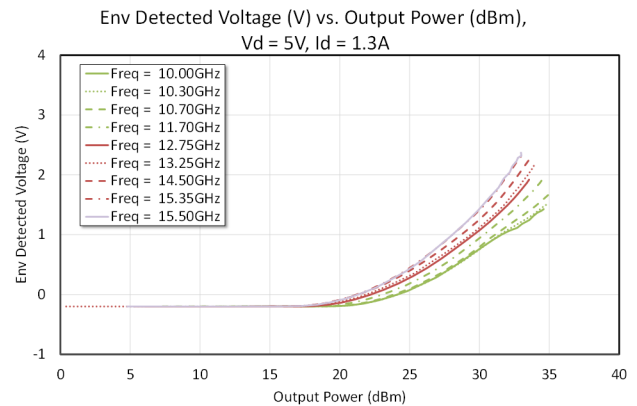
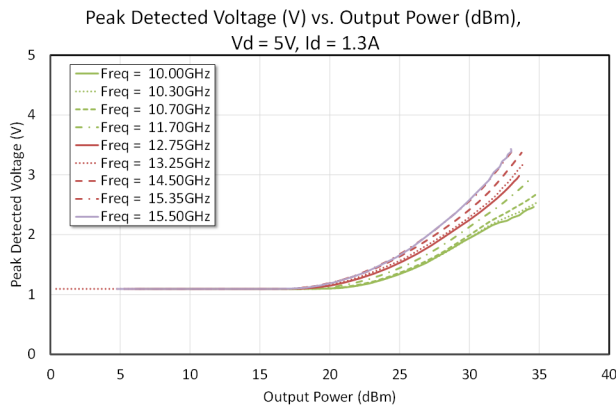
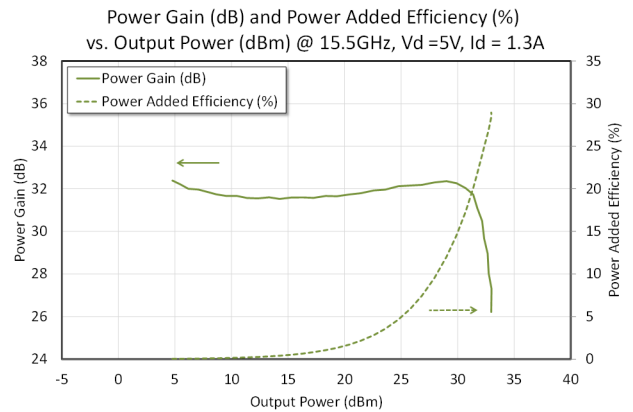
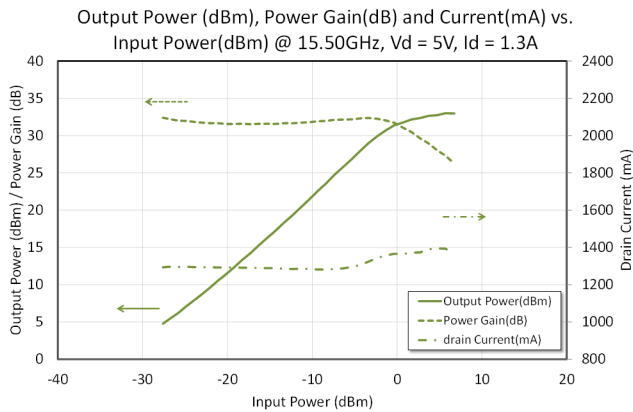
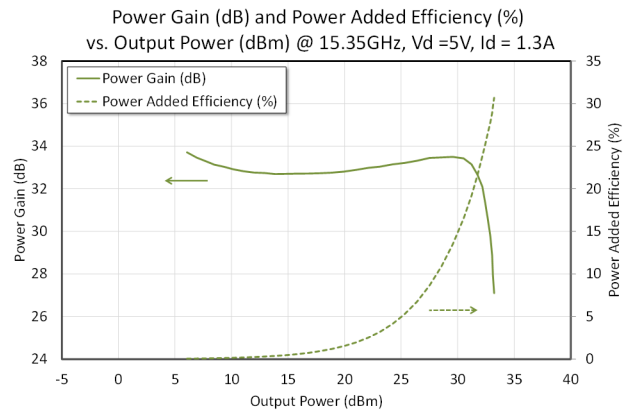
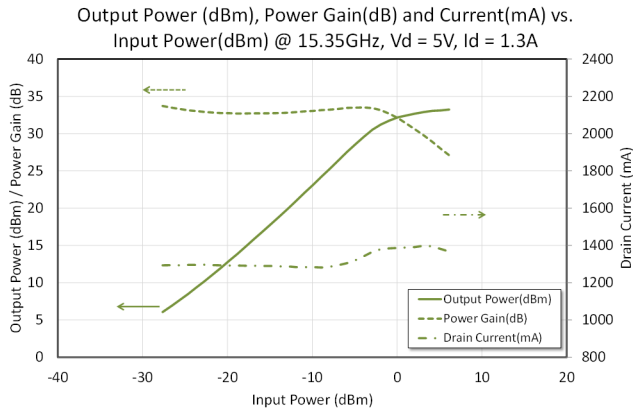
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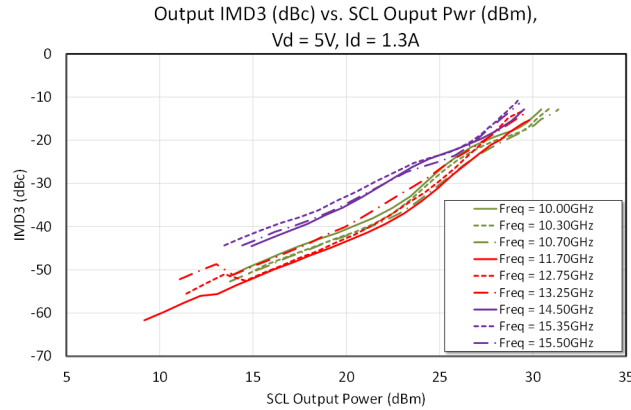
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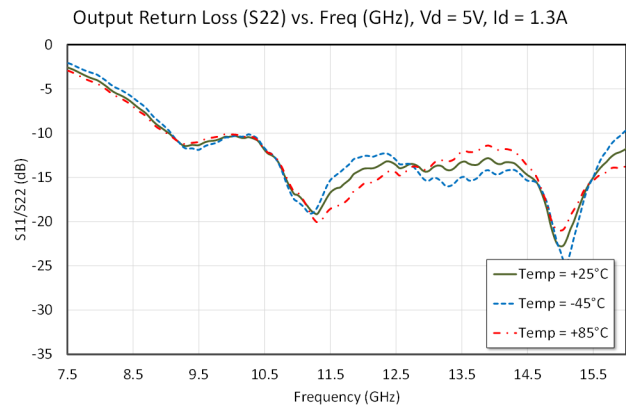
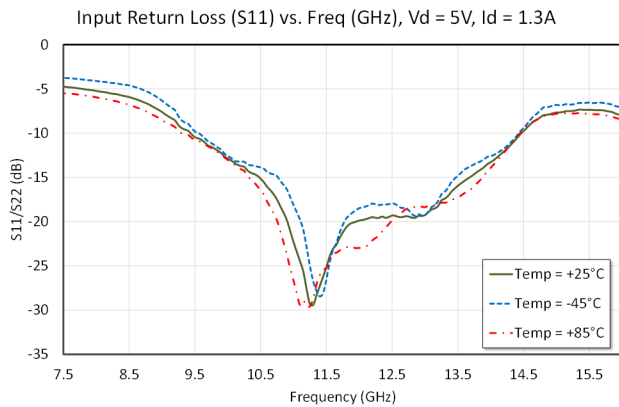
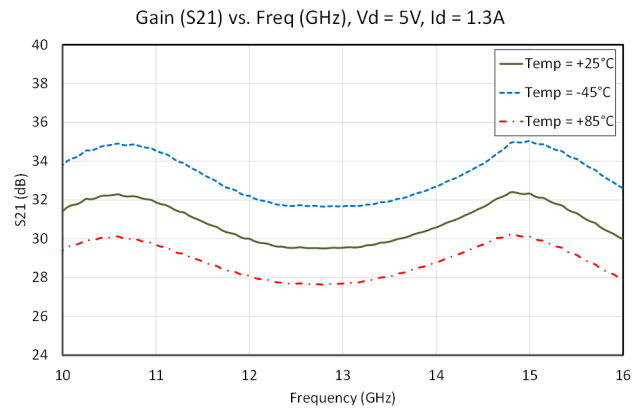
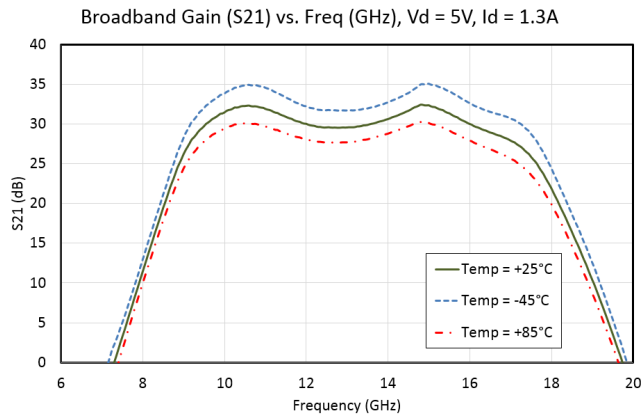
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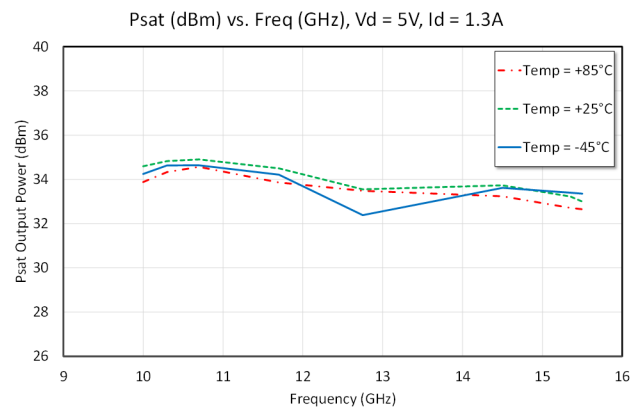
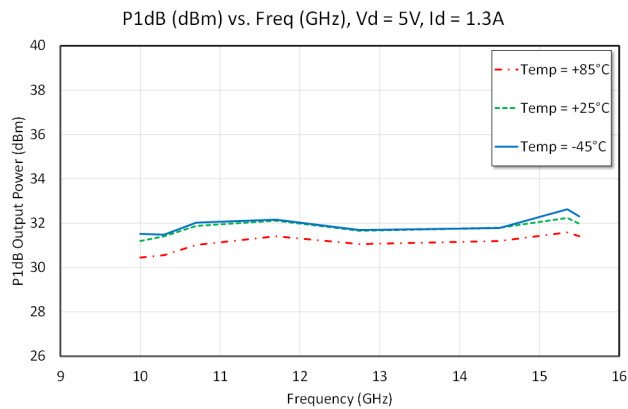
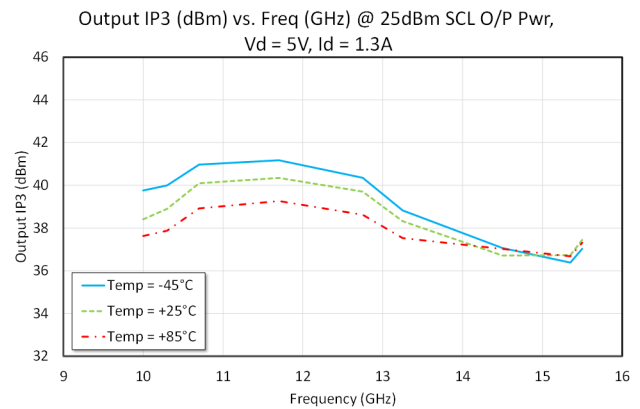
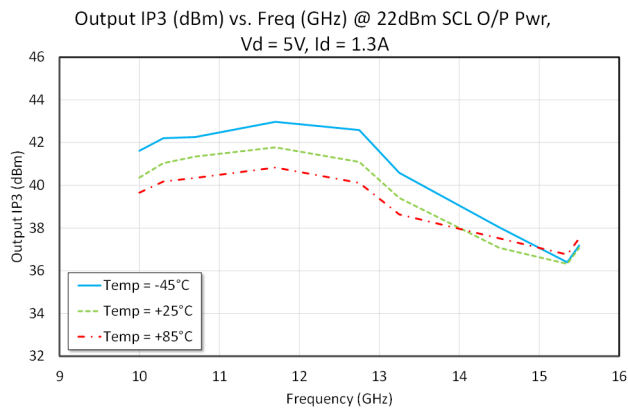
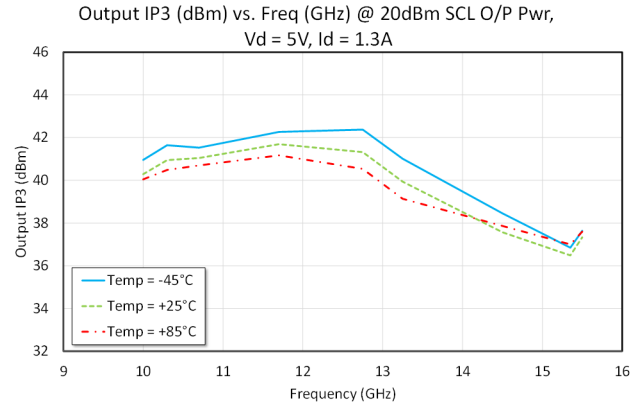
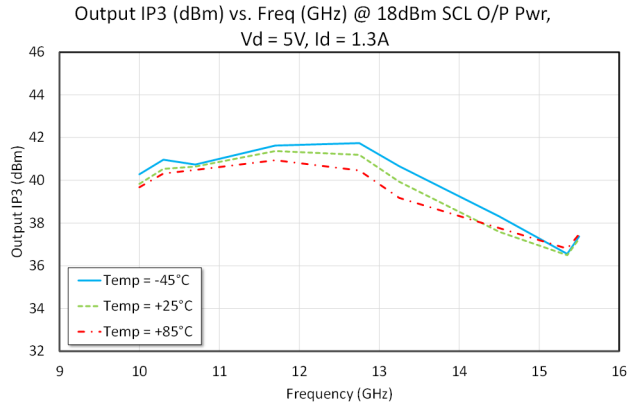
Typical Performance Curves: $V_D = 5\text{ V}$, $I_{DQ} = 1.3\text{ A}$, $V_G = -1.05 \sim -0.85\text{ V}$, $T_A = +25^\circ\text{C}$



Typical Performance Curves: $V_D = 5\text{ V}$, $I_{DQ} = 1.3\text{ A}$, $V_G = -1.05 \sim -0.85\text{ V}$, $T_A = -40^\circ \sim +85^\circ\text{C}$



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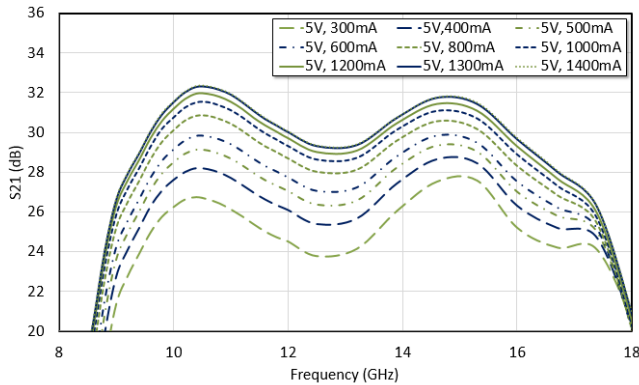


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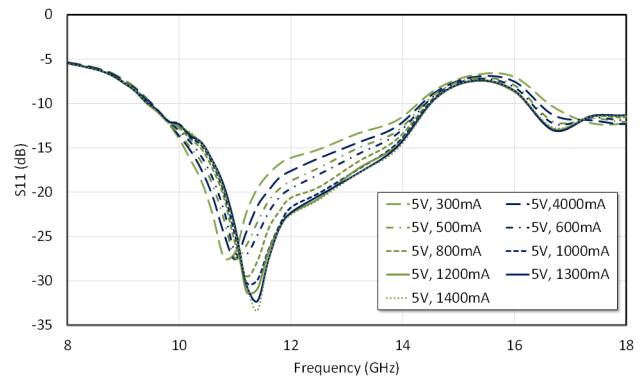
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Typical Performance Curves: $V_D = 5\text{ V}$, $I_{DQ} = \text{Various}$, $V_G = -1.05 \sim -0.85\text{ V}$, $T_A = +25^\circ\text{C}$

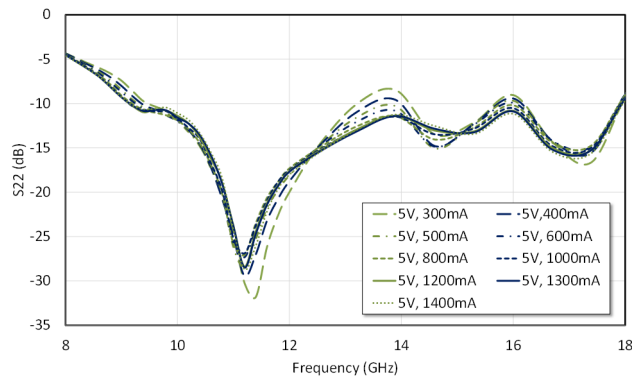
Gain (S21) vs. Freq (GHz), Various Bias Points



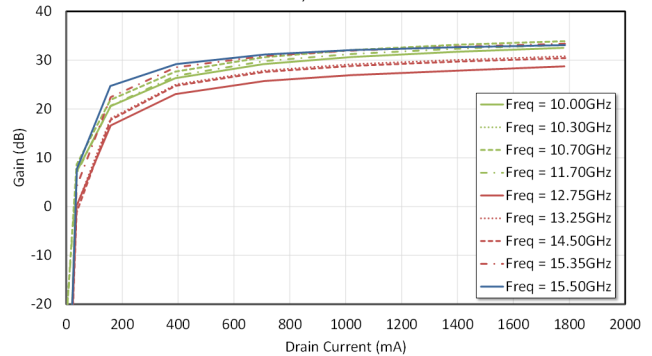
Gain (S11) vs. Freq (GHz), Various Bias Points



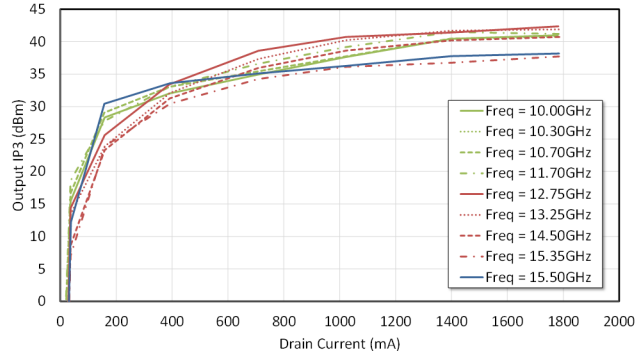
Gain (S22) vs. Freq (GHz), Various Bias Points



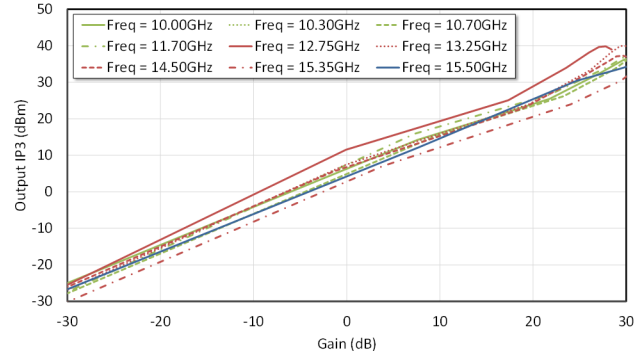
Gain (dB) vs. Drain Current (mA),
 $V_D = 5\text{ V}$, $I_D = \text{Various}$



Output IP3 (dBm) vs. Drain Current (mA),
 $V_D = 5\text{ V}$, $I_D = \text{Various}$



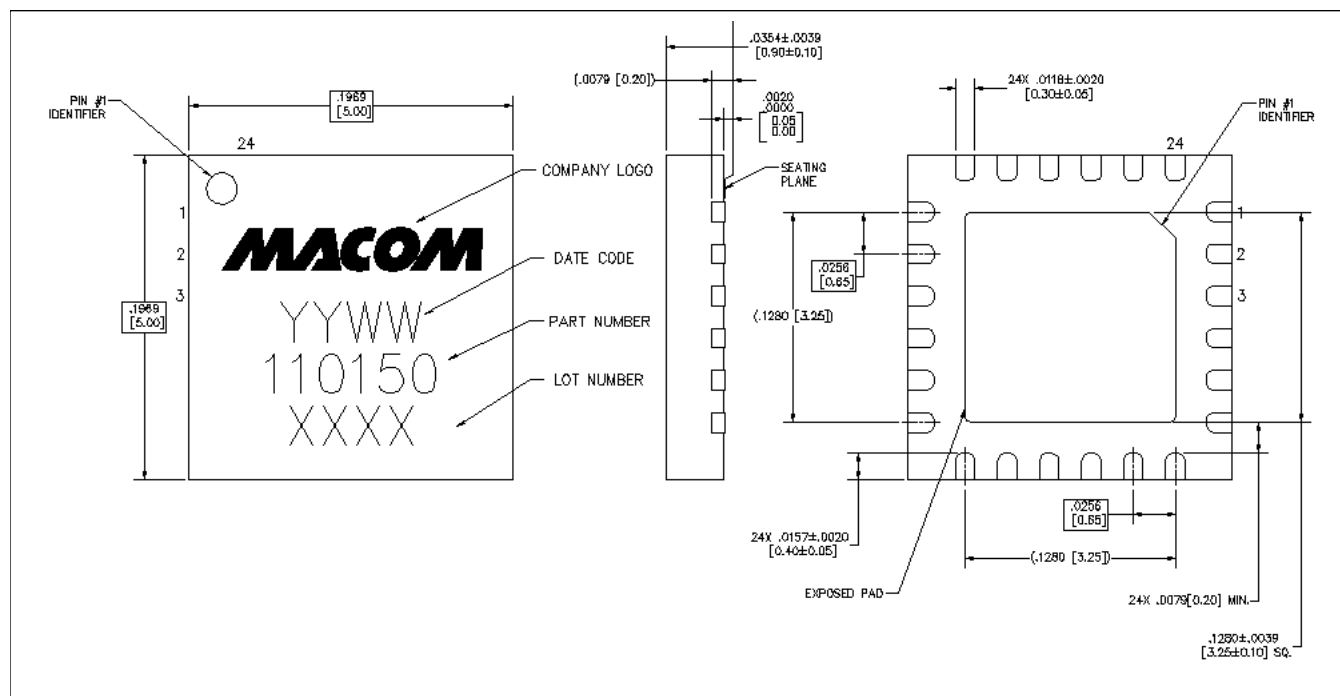
Output IP3 (dBm) vs. Gain (dB),
 $V_D = 5\text{ V}$, $I_D = \text{Various}$



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Lead-Free 5 mm 24-Lead PQFN



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements.
Plating is NiPdAu

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