

# Datasheet

# ZDB5101 Z-Wave Development Board

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Description:	This datasheet is for the ZM5101 Z Wave SiP Module based ZDB5101 Z-Wave Development Board.
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	REVISION RECORD					
Doc. Rev	Date	Ву	Pages affected	Brief description of changes		
3	20170517	MHansen	Table 5	Specified if measurements are radiated or conducted		
1D	20140506	slarsen	Figure 3.1, Table 4, p.1, p.10	Removed all references to matching network component as no matching is done on the board. Removed references to EU/US/HK BOM splits. BOMs are identical.		
1C	20131122	MVithanage	Figure 4.1	Removed caption		
1B	20131119	MVithanage	Figure 3.1, §All, Table 4	Removed 2.4GHz antenna Changed API to variant/library Changed OTP to Flash		
1A	20131118	MVithanage	§All	Updated ZM4125 datasheet		
2	20180308	BBR	All	Added Silicon Labs template		

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# 1 ABBREVIATIONS

Abbreviation	Explanation
D	Differential
EEPROM	Electrically Erasable Programmable Read-Only Memory
HW	Hardware
1	Input
NM	Not Mounted
NVM	Non-Volatile Memory
0	Output
PCB	Printed Circuit Board
SiP	System-in-Package
SMA	Sub-Miniature A
SW	Software
ZDB	Z-Wave Development Board
ZDP	Z-Wave Development Platform

# 2 INTRODUCTION

### 2.1 Purpose

The purpose of this datasheet is to describe the ZDB5101 Z-Wave Development Board. The ZDB5101 Z-Wave Development Board contains the highly integrated ZM5101 Z-Wave SiP Module, NVM, HW interface protection circuitry, PCB antennas and a SMA connector for whip antenna mounting.

#### 2.2 Audience and prerequisites

The audience is customers who want to use or evaluate the ZM5101 Z-Wave SiP Module or find inspiration for implementing the ZM5101 on a 4-layer application PCB.

### 3 ZDB5101 Z-WAVE DEVELOPMENT BOARD

The ZDB5101 Z-Wave Development Board contains the ZM5101 Z-Wave SiP Module, NVM, HW Interface protection circuitry, PCB antennas and a SMA connector for whip antenna mounting. The key components on ZDB5101 are shown in Figure 3.1.

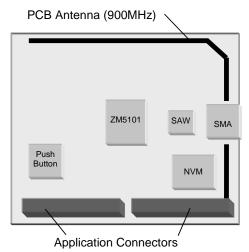


Figure 3.1: ZDB5101 Z-Wave Development Board

### 3.1 Application Connector Specification

The Application Connectors, J1, J2, on ZDB5101 Z-Wave Development Board are 2x10 2mm pitch pin rows. The signal availability on the application connectors are shown in Table 1.

Table 1: ZDB5101 Application Connector Pin List

	ZDB5101 / ZM4125-S		ZDB5101 / ZM4125-S
J1 no.	Pin Name	J2 no.	Pin Name
1	VPP	1	Ground
2	P2.6-MISO0	2	Ground
3	P3.7-PWM-ADC3-ZEROX-KEYPAD	3	P1.3-Keypad
4	P0.7-KEYPAD	4	P1.7-Keypad
5	P3.6-IRTX2-ADC2-TRIAC-KEYPAD	5	P0.6-Keyoad
6	P1.1-INT1-KEYPAD	6	P1.6-Keypad
7	P3.5-IRTX1-ADC1-KEYPAD	7	P0.5-Keypad
8	P2.5-MOSI0	8	P1.5-Keypad
9	USB_DM	9	P0.4-Keypad
10	P2.3-MISO1	10	P1.4-Keypad
11	USB_DP	11	P0.3-Keyoad
12	P2.4-SCK1	12	P1.2-Keypad
13	GND	13	P0.2-Keypad
14	P2.2-MOSI1	14	P1.0-INT0-Keypad
15	RESET_N	15	
16	P2.1-TXD0	16	P3.1-IRRX-TXD1-Keypad
17	VCC	17	P0.0-Keypad
18	P2.0-RXD0	18	P3.0
19	P2.7-SCK0	19	NC
20	P3.4-IRTX0-ADC0-KEYPAD	20	NC

Table 2 gives an overview of the communication interfaces, signaling pins, and some ZM5101 HW features available on the application connectors. All GPIOs from ZM5101 are available on application

connectors J1, J2. For a complete list of signals and functionalities available, refer to the ZM5101 Z-Wave SiP Module Datasheet [1].

Table 2: ZDB5101 Z-Wave Development Board Application Connector Layout

## ADC[3:0]  ADC[3:0]  ADC[3:0]  J1: 3  J1: 5  J1: 5  J1: 7  ADC2: input  ADC2: input  ADC3: input  ADC4: input/ligher reference  ADC0: input/higher reference  GND  J1: 13  J2: 1, 2  INT1  INT0  J2: 14  INT0  J2: 14  INT0  Appendix A for IO pin number  P[0.0-0.0], Refer to Appendix A for IO pin number  P[3.0-3-1]  P[3.4-3.7]  MISO1  J1: 10  MOSI1  J1: 10  I/O  Master only SPI - Master-In-Slave-Out, and prog interface.  Work as a keypad matrix.  INT0  J1: 15  I Reset: Active low reset. The ZM5101 Z-Wave SIP Module has an integrated Power-On-Reset and Brown-out detection circuitry.  RXD0  J1: 18  I UART Receive Data: Supports up to 230.4kbaud.  SCK1  TRIAC  J1: 16  O UART Transmit Data: Supports up to 230.4kbaud.  ZEROX  J1: 1  Power  J2: 10  Master or slave SPI. Master-In-Slave-Out SPI interface.  OTERIAC Control: A triac controller is implemented in the ZM5101 Z-Wave SiP Module has an integrated Power-On-Reset and Brown-out detection circuitry.  RXD0  J1: 16  O UART Transmit Data: Supports up to 230.4kbaud.  ZEROX  J1: 1  Power  J2: 10  Master only SPI - SPI Clock, and SPI clock for prog interface.  VPP  J1: 1  Power  OTERIAC Control: A triac controller is implemented in the ZM5101 Z-Wave SiP Module that can control a triac on the Application Module like light dimmer modules etc.  TXD0  J1: 16  O UART Transmit Data: Supports up to 230.4kbaud.  ZEROX  J1: 3  I Zero Cross Detection: Used on dimmer modules for detecting 120/240V zero crossing.  VPP  J1: 1  Power  OTERIAC Control: A triac controller is implemented in the ZM5101 Z-Wave SiP Module that can control a triac on the Application Module like light dimmer modules etc.  ACCO TRIAC Control SPI SIP Clock and SPI clock for prog interface.  WPM  J1: 1  Power  J1: 1  Power  J2: 10  Master or slave SPI. Master-In-Slave-Out SPI interface.  MOSIO  J1: 19  I/O  Master or s		Table 2: ZDB5101 Z-Wave Development Board Application Connector Layout					
ADC[3:0]  Analog-to-Digital Converter input. The ADC is 12/8 bit and can use +3.3V, an internal or an external voltage as reference.  ADC3: input ADC2: input ADC1: input/lower reference ADC3: input ADC1: input/lower reference ADC3: input ADC3: input ADC3: input ADC4: input/lower reference ADC5: input/lower reference GND J1: 13 J2: 1, 2  INT1 J1: 6 INT0 J2: 14  INT1 INT0 J2: 14  INT1 INT1 INT1 INT1 INT1 INT1 INT1 INT	Name	Pin#	I/O	Description			
Hand the state of	+3.3V	J1: 17	Power				
J1: 3 J1: 5 J1: 7 ADC3: input ADC2: input ADC3: input ADC3: input/lower reference ADC0: input/higher reference ADC0: input/higher reference ADC0: input/higher reference ADC0: input/higher reference  GND J1: 13 J2: 1, 2 INT1 J1: 6 I/O Interrupt: The signals are level triggered. When in power down mode, the ZDB5101 Z-Wave Development Board's MCU can be woken by asserting the interrupt signal. P[0.0-0.0], Appendix A for IO pin number P[3.0-3.1] P[3.0-3.1] P[3.4-3.7] MISO1 J1: 10 I/O Master only SPI - Master-In-Slave-Out, and prog interface.  MOSI1 J1: 14 I/O Master only SPI - Master Out Slave In, and prog interface. PWM J1: 3 I Reset: Active low reset. The ZM5101 Z-Wave SiP Module has an integrated Power-On-Reset and Brown-out detection circuitry.  RXD0 J1: 18 I UART Receive Data: Supports up to 230.4kbaud.  Master Only SPI - SPI Clock, and SPI clock for prog interface.  TXD0 J1: 16 O UART Transmit Data: Supports up to 230.4kbaud.  MISO0 J1: 2 I/O Master or slave SPI. Master-In-Slave-Out SPI interface.  TXD1 J2: 16 O UART Transmit Data: Supports up to 230.4kbaud.  MISO0 J1: 2 I/O Master or slave SPI. Master-In-Slave-Out SPI interface.  MOSI0 J1: 8 I/O Master or slave SPI. Master-In-Slave-Out SPI interface.  MISO0 J1: 19 I/O Master or slave SPI. Master-In-Slave-Out SPI interface.  Mosio J1: 19 I/O Master or slave SPI. Master-In-Slave-Out SPI interface.  Mosio J1: 19 I/O Master or slave SPI. Master-In-Slave-Out SPI interface.  Mosio J1: 19 I/O Master or slave SPI. Master-In-Slave-Out SPI interface.  Mosio J1: 19 I/O Master or slave SPI. Master-In-Slave-Out SPI interface.  Mosio J2: 18 I UART Receive Data: Supports up to 230.4kbaud.	ADC[3:0]		I				
J1: 5   J1: 7   ADC2: input   ADC1: input/lower reference   ADC3: input/lower reference   ADC3				l · · ·			
GND J1: 13 J2: 1, 2  INT1 J1: 6 INT0 J2: 14  INT0 J2: 14  INT1 J1: 6 INT0 J2: 14  INT0 J2: 14  INT1 J1: 6 INT0 J2: 14  INT0 J2: 15  INT0 J2: 16  INT0 J2: 18  INT				·			
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GND				· ·			
INT1 J1: 6 I/O Interrupt: The signals are level triggered. When in power down mode, the ZDB5101 Z-Wave Development Board's MCU can be woken by asserting the interrupt signal.  P[0.0-0.0], P[1.0-1.7] Appendix A for I/O pin number P[3.0-3.1] P[3.4-3.7]  MISO1¹ J1: 10 I/O Master only SPI - Master-In-Slave-Out, and prog interface.  MOSI1¹ J1: 14 I/O Master only SPI - Master Out Slave In, and prog interface.  PWM J1: 3 I Puse Width Modulator Output: Used for frequency variation applications.  RESET_N J1: 15 I Reset: Active low reset. The ZM5101 Z-Wave SiP Module has an integrated Power-On-Reset and Brown-out detection circuitry.  RXD0 J1: 18 I UART Receive Data: Supports up to 230.4kbaud.  SCK1¹ J1: 12 I/O Master only SPI - SPI Clock, and SPI clock for prog interface.  TRIAC J1: 5 O TRIAC Control: A triac control a triac on the Application Module like light dimmer modules etc.  TXD0 J1: 16 O UART Transmit Data: Supports up to 230.4kbaud.  ZEROX J1: 1 Power OTP programmable voltage  TXD1 J2: 16 O UART Transmit Data: Supports up to 230.4kbaud.  MISO0 J1: 2 I/O Master or slave SPI. Master-In-Slave-Out SPI interface.  MOSI0 J1: 8 I/O Master or slave SPI. Master Out Slave In SPI interface.  MOSI0 J1: 19 I/O Master or slave SPI. SPI Clock  RXD1 J2: 18 I UART Receive Data: Supports up to 230.4kbaud.  USB-DM J1: 9 I/O USB differential input/output	2712			, ,			
INT1 INT0 J1: 6 J2: 14 I/O Interrupt: The signals are level triggered. When in power down mode, the ZDB5101 Z-Wave Development Board's MCU can be woken by asserting the interrupt signal.  P[0.0-0.0], Refer to Appendix A for IO pin number P[3.4-3.7]	GND		Power	Ground signal			
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P[1.0-1.7]	P[0 0-0 0]	Refer to	I/O	· · · ·			
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USB-DM J1: 9 I/O USB differential input/output			I/O	Master or slave SPI. SPI Clock			
	RXD1	J2: 18	l	UART Receive Data: Supports up to 230.4kbaud.			
USB-DP J1: 11 I/O USB differential input/output	USB-DM	J1: 9	I/O	USB differential input/output			
	USB-DP	J1: 11	I/O	USB differential input/output			

<sup>1.</sup> Please note that the SPI interface (MISO, MOSI and SCK) is not available for the Application SW in some Z-Wave protocol variants.

All signals in Table 2 except '+3.3V', 'VCC' and 'GND' are connected through a 1kohm resistor to the ZM5101 Z-Wave SiP Module (U1 in Appendix A).

#### 3.2 SPI Interfaces and NVM

SPI1 interface is used by the protocol in some Z-Wave protocol variants to store routing tables in an external NVM (EEPROM or Flash). The Application SW must <u>not</u> use the SPI1 interface while it is used by the protocol. Table 3 lists the available SW libraries and shows where the Application SW can use SPI1.

Table 3:	SW	Library	/ SPI	availability
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SW Library	External NVM used by Protocol
Routing Slave	No
Enhanced Slave	Yes
Controller	Yes
Static Controller	Yes
Installer	Yes
Bridge	Yes
Portable controller	Yes

P2.5 on ZM5101 Z-Wave SiP Module is the default NVM chip select pin. To assure proper control of the NVM chip select signal during reset and power-up, a pull up resistor on the P2.5 is implemented as shown in Figure 3.2.

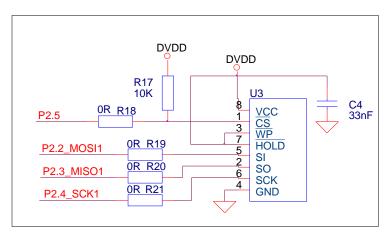


Figure 3.2: External NVM

The protocol data storage occupies only a part of the NVM memory. The required memory space depends on the used Z-Wave protocol variant. The Application SW can use the remaining memory space.

#### 3.3 EMC Noise Reduction

As default, a 1000R@100MHz Ferrite Bead is mounted between the Application Connector '+3.3V' and module '+3.3V' (L3 in Appendix A) to reduce noise from the Application Circuitry.

As default 1000R@100MHz Ferrite Beads are mounted in series with the TRIAC signal and the ZEROX signal (L4 and L5 in Appendix A) to reduce noise from triac circuitry if used for this purpose. Two zero ohm resistors can be mounted instead in applications where TRIAC and ZEROX is not used for power electronic control.

### 3.4 ZM5101 MCU Specification

Table 4: MCU Specifications

MCU	Description
MCU Type	Optimized 8-bit 8051 MCU core.
MCU speed	32 MHz
Flash Memory	128kbyte. Programmed through the SPI1, UART0, or USB interface.
SRAM	16kbyte
SRAM (CPU)	256byte
RAM (Low power)	128byte (optionally powered in low power state)
MTP Memory	64byte. Non Volatile Data Memory

### 3.5 RF Specification for ZDB5101 with SAW

Table 5: RF Specifications

RF Parameter	Description		
RF data rate	9.6kbps		
	40kbps		
	100kbps		
Modulation	Frequency Shift Keying (FSK): 9.6kbps and 40kbps		
	Gaussian Frequency Shift Keying (GFSK): 100kbps		
Frequency deviation	9.6kbps: Center frequency ± 20kHz		
	40kbps: Center frequency ± 20kHz		
	100kbps: Center frequency ± 29kHz		
Signal coding	9.6kbps Manchester Encoded		
	40kbps and 100kbps Non-Return to Zero		
Typical RF receiver sensitivity <sup>2</sup>	-103dBm @ 9.6kbps		
	-99dBm @ 40kbps		
<u>, , , , , , , , , , , , , , , , , , , </u>	-93dBm @ 100kbps		
Typical RF output power <sup>2</sup>	-26dBm to +4dBm		
Typical range <sup>1</sup>	Indoor > 40 meters line of sight, in unobstructed environment		
	Outdoor > 100 meters line of sight		
RF input/output impedance	50ohm @ respective E/U/H frequencies		
RF regulatory	ACMA Compliance		
	CE Compliance		
	FCC Compliance		
IC Compliance			
	MIC Compliance		

<sup>1.</sup> Test Conditions: ZDB5101 measured radiated with quarter-wavelength monopole antenna mounted on ZDP03A.

#### 3.6 Electrical Specification

The "Absolute Maximum Ratings" specifies the conditions in which the ZDB5101 Module is guaranteed not to be damaged but correct operations are not guaranteed. Exceeding the "Absolute Maximum Ratings" may destroy the ZDB5101 Module. See "DC Characteristics" for guaranteed operation limits.

<sup>2.</sup> Test Conditions: ZDB5101 measured conducted at output of SAW filter through on-board SMA.

#### 3.6.1 **Absolute Maximum Ratings**

Table 6: Absolute Maximum Ratings

Electrical	Value
Operating Temperature	-40°C to +85°C
Voltage on input pins	-0.3V to +3.6V
Minimum Operating Voltage ('+3.3V')	+2.3V
Maximum Operating Voltage ('+3.3V')	+3.6V

#### 3.6.2 **DC Characteristics**

The following DC characteristics are for the ZDB5101 Z-Wave Development Board. DC characteristics related to the ZM5101 are to be found in [1] and are not listed in this datasheet.

**Table 7:** DC Characteristics ( $T_A = 25^{\circ}C$ , '+3.3V' = 3.3V)

Symbol	Parameter	Condition	Min	Тур	Max	Units
'+3.3V'	Main Supply voltage (1)		2.7	3.3	3.6	V
R <sub>AC</sub>	Application Connector Serial Resistor	All signals	0.9	1.0	1.1	kΩ
I <sub>C</sub> <sup>(2)</sup>	Continuous Output Current	One GPIO	-8		8	mA
I <sub>CTOT</sub> <sup>(2)</sup>	Total continuous output source/sink current	All GPIO	-120		120	mA
I <sub>CC</sub>	Transmitting <sup>(3)</sup>	RFPOW Setting: 01 <sup>4</sup> RFPOW Setting: 63 <sup>4</sup>		28 45		mA
	Receiving <sup>(5)</sup>			32		mA
	Power Down <sup>(6)</sup>			2		μА
	Programming mode			15		mA
T <sub>OP</sub>	Operating Temperature		-40		85	°C
H <sub>OP</sub>	Operating Relative Humidity		8		80	%

- Minimum supply voltage depends on EEPROM/Flash selection. 2.7V is with flash M25PE10. (1) (2) (3) (4) (5)
- If serial 1k ohm resistor is replaced with 0 ohm resistor.
- The transceiver is in transmit mode with the MCU running. The ADC is off.
- Pout available at the SMA connector with SAW filter mounted on ZDB5101.
- The transceiver is in receive mode with the MCU running. The ADC is off.
- Sleep mode, IO ports are powered while MCU, SRAM's, RF transceiver, and ADC are shut down. The chip will wake on brown-out, an external reset pulse, external interrupt (if enabled) and Wake-up timer pulses. Power down current is depending on external memory chip type selected.

### 3.7 Module Outline

Table 8: Module Dimensions

Physical	Description
Dimension (H x W x D)	8 mm x 54 mm x 47 mm

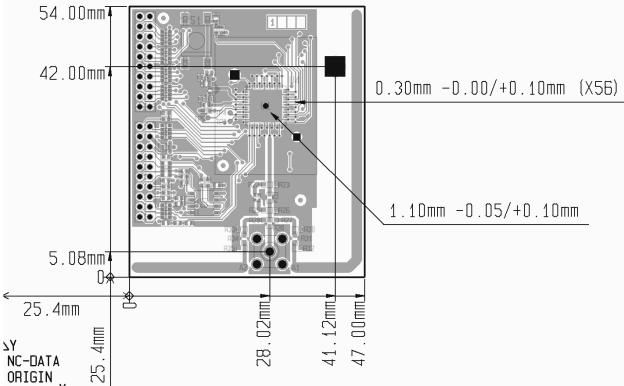


Figure 3.3: ZDB5101 Z-Wave Development Board PCB outline (Top View)

The Application Connector is a standard 2mm pitch 2x10 pin row. The pad hole is a Ø0.9mm plated hole. Metallic objects should be min 10mm from the PCB antenna when mounted on ZDP03A or in a customer based platform. This ensures a good radiation pattern from the antennas.

### 3.8 Z-Wave Module Component Placement

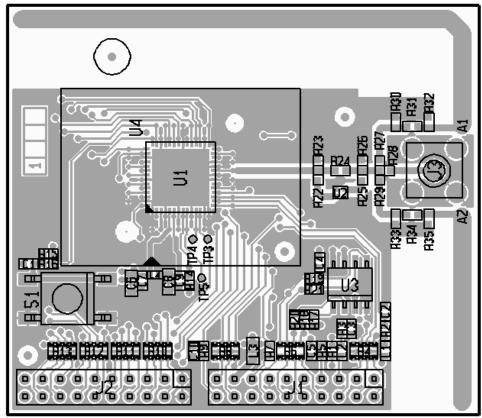


Figure 3.4: ZDB5101 Z-Wave Development Board Component Placement (Top View)

U1 is the ZM5101 Z-Wave SiP Module. U4 is the test socket, which can be mounted on the same PCB, and contain the ZM5101. A1 is the 900MHz antenna, A2 is a higher frequency antenna that is not used. J1 and J2 are application connectors interfacing either to the ZDP03A Z-Wave Development Platform or a customer designed PCB. J1 and J2 contain all GPIOs from the ZM5101 Z-Wave SiP Module.

### 3.9 Module Naming:

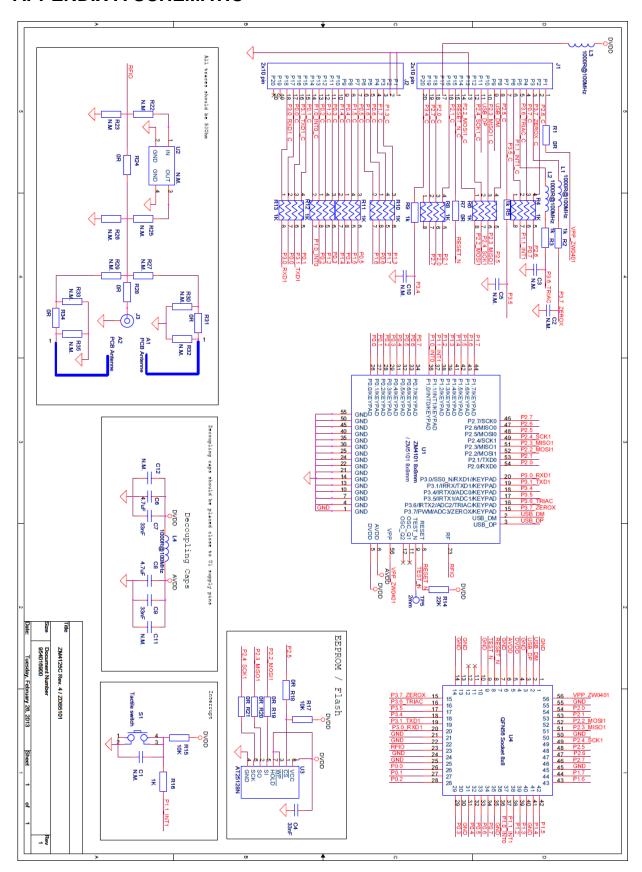
Sigma Designs use the following naming convention:

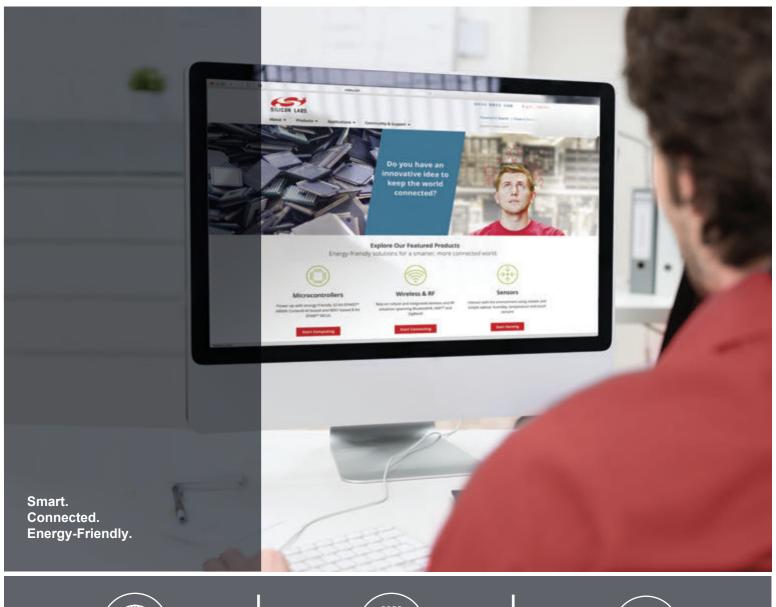
Z-Wave Module	Z-Wave Development Board
ZMGVSS	ZDBGVSS
ZM – Z-Wave Module	ZDB – Z-Wave Development Board
G – Z-Wave Generation	Mounted Module:
V – Module Variant	G – Z-Wave Generation
SS – Size in cm <sup>2</sup>	V – Module Variant
	SS – Size in cm <sup>2</sup>
e.g.: ZM5101	
	e.g.: ZDB5101

# 4 REFERENCES

- [1] DSH12625, Datasheet, "ZM5101"
- [2] DSH11243, Datasheet, "ZDP03A, Z-Wave Development Platform"
- [3] APL10045, Application Note, "Antennas for Short Range Devices"

# **APPENDIX A SCHEMATIC**









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