# EVAL6474PD

## Stepper motor driver mounting the L6474 in a high power PowerSO package

**Data brief**




## Description

The EVAL6474PD demonstration board is a microstepping motor driver. In combination with the STEVAL-PCC009V2 communication board and SPIN evaluation software, the board allows the user to investigate all the features of the L6474 device.

The 4-layer layout and the PowerSO package allow the highest thermal performance to be obtained.

The EVAL6474PD supports the daisy chain configuration making it suitable for the evaluation of the L6474 in multi motor applications.

## Features

- Voltage range from 8 V to 45 V
- Phase current up to 3 $A_{r.m.s.}$
- SPI with daisy chain feature
- Socket for external resonator or crystal
- FLAG LED indicator
- Suitable for use in combination with STEVAL-PCC009V2



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# Board description

**Table 1. EVAL6474PD specifications**

| Parameter | Value |
|---|---|
| Supply voltage (VS) | 8 to 45 V |
| Maximum output current (each phase) | 3 $A_{r.m.s.}$ |
| Logic supply voltage (VREG) | Externally supplied: 3.3 V<br>Internally supplied: 3 V typical |
| Logic interface voltage (VDD) | Externally supplied: 3.3 V or 5 V<br>Internally supplied: VREG |
| Low level logic input voltage | 0 V |
| High level logic input voltage | VDD(1) |
| Operating temperature | -25 to +125 °C |
| L6474PD thermal resistance junction to ambient | 12 °C/W typical |

1. All logic inputs are 5 V tolerant.

**Figure 1. Jumper and connector location**

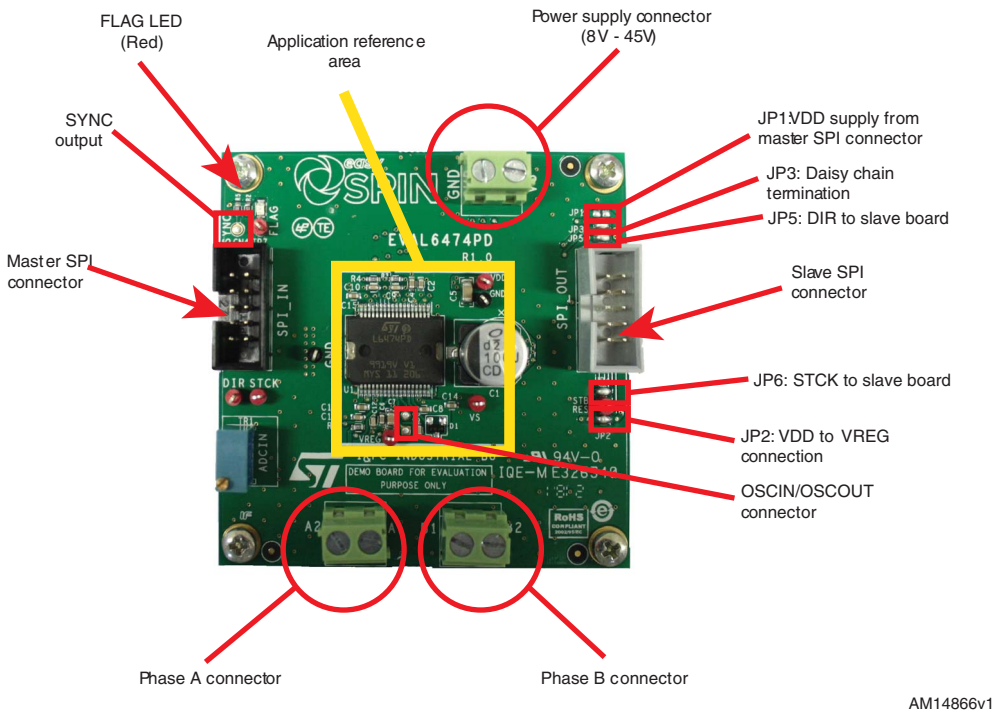


**Table 2. Jumper and connector description**

| Name | Type | Function |
|---|---|---|
| M1 | Power supply | Motor supply voltage |
| M2 | Power output | Bridge A outputs |
| M3 | Power output | Bridge B outputs |
| CN1 | SPI connector | Master SPI |
| CN2 | SPI connector | Slave SPI |
| CN3 | NM connector | OSCIN and OSCOUT pins |
| CN4 | NM connector | SYNC output |
| TP1 (VS) | Test point | Motor supply voltage test point |
| TP2 (VDD) | Test point | Logic interface supply voltage test point |
| TP6 (VREG) | Test point | Logic supply voltage/L6474 internal regulator test point |
| TP4 TP5 (GND) | Test point | Ground test point |
| TP8 (STCK) | Test point | Step-clock input test point |
| TP3 (DIR) | Test point | BUSY/SYNC output test point |
| TP9 (STBY/RES) | Test point | Standby/reset input test point |
| TP7(FLAG) | Test point | FLAG output test point |

**Table 3. Master SPI connector pinout (CN1)**

| Pin number | Type | Description |
|---|---|---|
| 1 | Open drain output | L6474 direction input |
| 2 | Open drain output | L6474 FLAG output |
| 3 | Ground | Ground |
| 4 | Supply | EXT_VDD (can be used as external logic power supply) |
| 5 | Digital output | SPI “Master In Slave Out” signal (connected to L6474 SDO output through daisy chain termination jumper JP2) |
| 6 | Digital input | SPI serial clock signal (connected to L6474 CK input) |
| 7 | Digital input | SPI “Master Out Slave In” signal (connected to L6474 SDI input) |
| 8 | Digital input | SPI slave select signal (connected to L6474 CS input) |
| 9 | Digital input | L6474 step-clock input |
| 10 | Digital input | L6474 standby/reset input |

**Table 4. Slave SPI connector pinout (CN2)**

| Pin number | Type | Description |
|---|---|---|
| 1 | Open drain output | L6474 direction input |
| 2 | Open drain output | L6474 FLAG output |
| 3 | Ground | Ground |
| 4 | Supply | EXT_VDD (can be used as external logic power supply) |
| 5 | Digital output | SPI “Master In Slave Out” signal (connected to pin 5 of J10) |
| 6 | Digital input | SPI serial clock signal (connected to L6474 CK input) |
| 7 | Digital input | SPI “Master Out Slave In” signal (connected to L6474 SDO output) |
| 8 | Digital input | SPI slave select signal (connected to L6474 CS input) |
| 9 | Digital input | L6474 step-clock input |
| 10 | Digital input | L6474 standby/reset input |

**Figure 2. EVAL6474PD schematic**

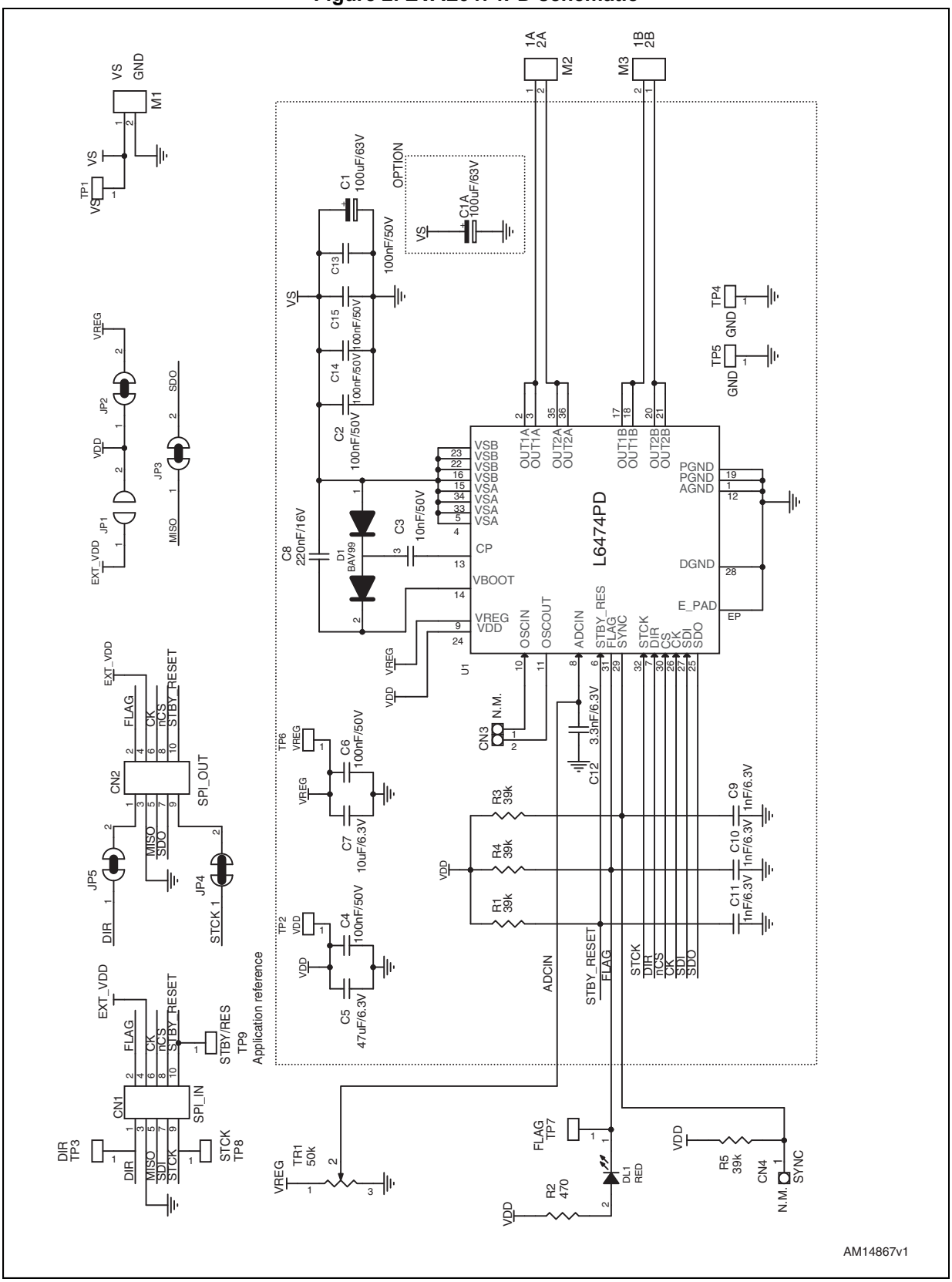


**Table 5. Bill of material**

| Index | Quantity | Reference | Value | Package |
|---|---|---|---|---|
| 1 | 1 | C1 | 220 nF/16 V | CAPC-0603 |
| 2 | 1 | C2 | 47 µF/6.3 V | CAPC-3216 |
| 3 | 1 | C3 | 100 nF/6.3 V | CAPC-0603 |
| 4 | 1 | C4 | 10 µF/4 V | CAPC-3216 |
| 5 | 1 | C5 | 100 nF/4 V | CAPC-0603 |
| 6 | 4 | C6, C7, C8, C10 | 100 nF/50 V | CAPC-0603 |
| 7 | 1 | CN1 | 10-pole polarized IDC male header 2.54 mm vertical black | CON-FLAT-5 x 2 - 180 M |
| 8 | 1 | CN2 | 10-pole polarized IDC male header 2.54 mm vertical gray | CON-FLAT-5 x 2 - 180 M |
| 9 | 1 | CN3 | N. M. | STRIP254P-M-2 |
| 10 | 1 | CN4 | N. M. | TPTH-RING-1MM |
| 11 | 1 | C1A | 100 µF/63 V | CAPE-R10HXX-P5 |
| 12 | 1 | C1 | 100 µF/63 V | CAPES-R10HXX |
| 13 | 6 | C2, C4, C6, C13, C14, C15 | 100 nF/50 V | CAPC-0603 |
| 14 | 1 | C3 | 10 nF/50 V | CAPC-0603 |
| 15 | 1 | C5 | 47 µF/6.3 V | CAPC-1206 |
| 16 | 1 | C7 | 10 µF/6.3 V | CAPC-0805 |
| 17 | 1 | C8 | 220 nF/16 V | CAPC-0603 |
| 18 | 3 | C9, C10, C11 | 1 nF/6.3 V | CAPC-0603 |
| 19 | 1 | C12 | 3.3 nF/6.3 V | CAPC-0603 |
| 20 | 1 | DL1 | LED red | LEDC-0805 |
| 21 | 1 | D1 | BAV99 | SOT-23 |
| 22 | 1 | JP1 | Jumper open | JP2SO |
| 23 | 4 | JP2, JP3, JP4, JP5 | Jumper closed | JP2SO |
| 24 | 3 | M1, M2, M3 | Screw connector 2 poles | MORSV-508-2P |

Figure 3. EVAL6474PD - layout (top layer)

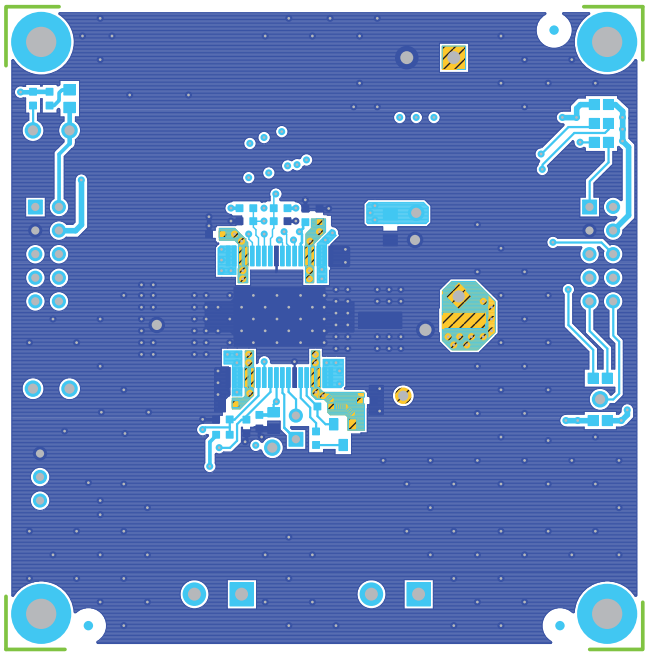



Figure 4. EVAL6474PD - layout (inner layer2)

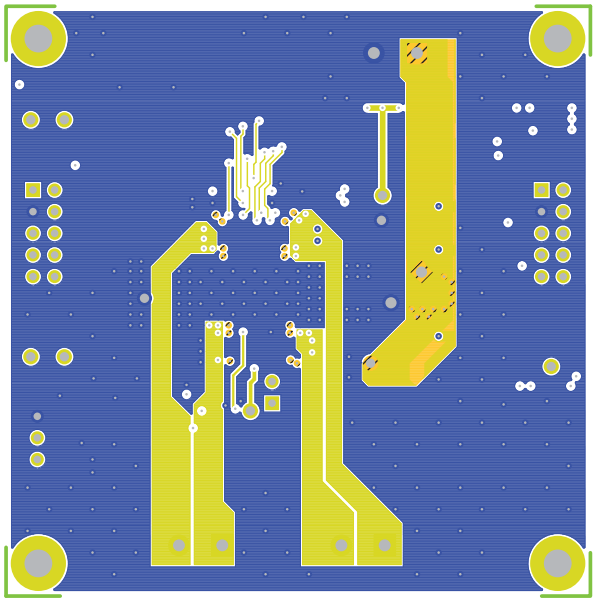


Figure 5. EVAL6474PD - layout (inner layer3)

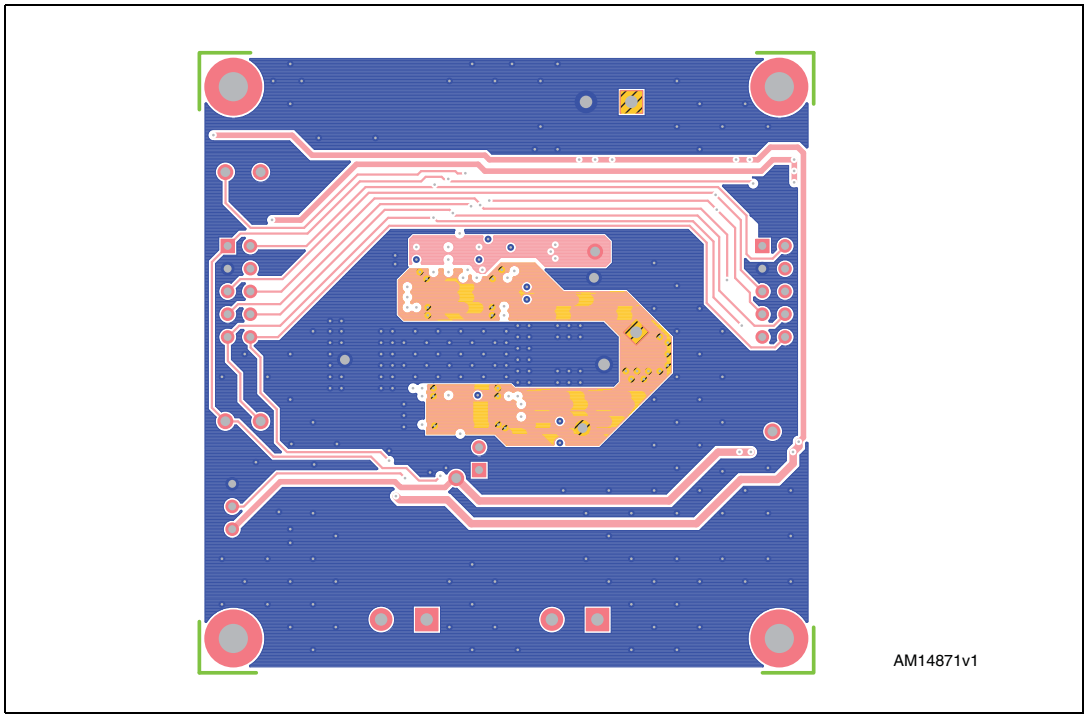
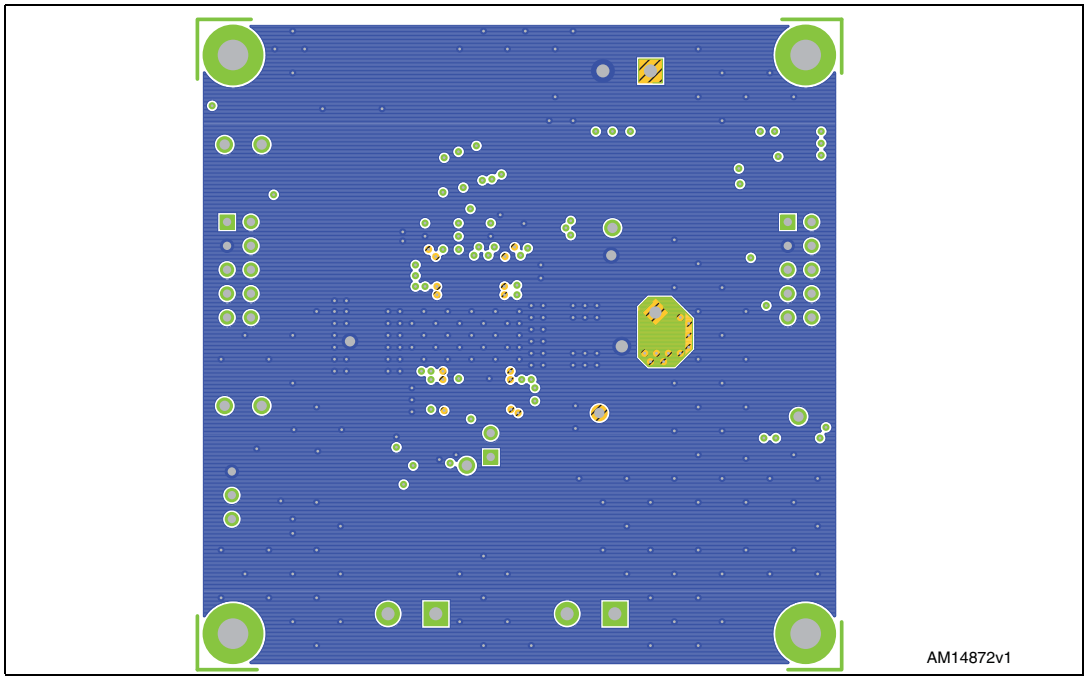
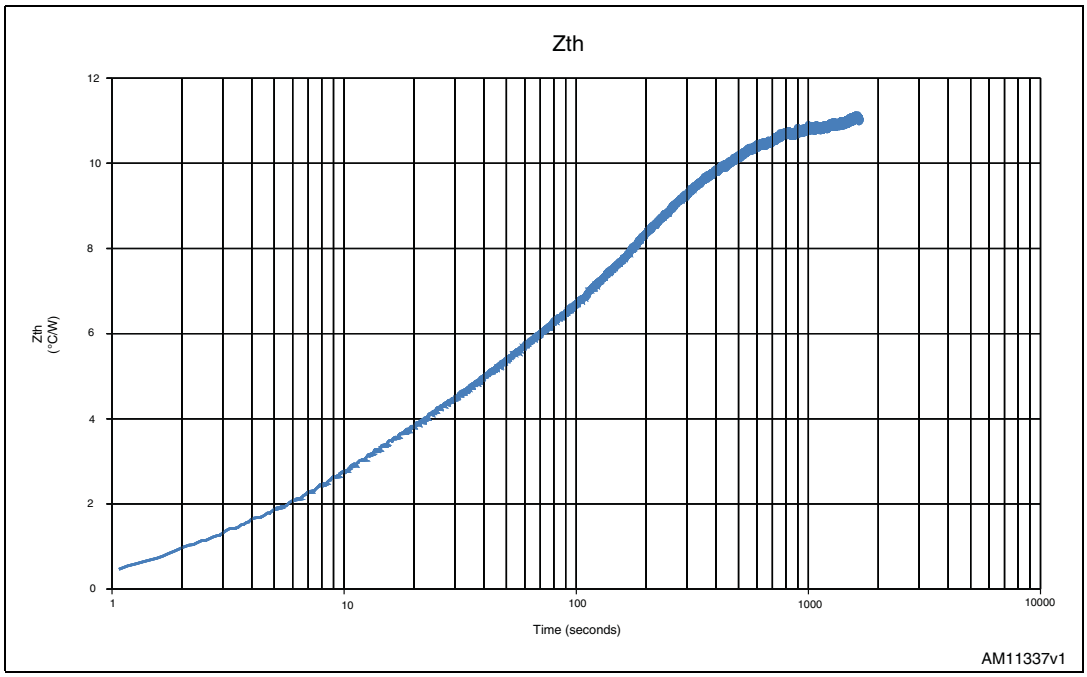



Figure 6. EVAL6474PD - layout (bottom layer3)



# Thermal data

**Figure 7. Thermal impedance graph**



# 1 Revision history

Table 6. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 07-Aug-2012 | 1 | Initial release. |
| 07-Sep-2012 | 2 | In cover page, dSPIN has been changed into easySPIN. |
| 19-Mar-2015 | 3 | Replaced easySPIN by SPIN in *Section : Description on page 1*.<br>Removed Figure 3. EVAL6474PD - silkscreen from page 7.<br>Updated *Figure 7: Thermal impedance graph on page 9* (replaced by new figure).<br>Minor modifications throughout document. |

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