SGM820
High-Accuracy Supervisory Circuit with Programmable Watchdog Timer

GENERAL DESCRIPTION

The SGM820 is a family of high-accuracy supervisory circuits with programmable watchdog timer. It provides various under-voltage threshold voltage options for 1.8V, 2.5V, 3V, 3.3V and 5V system rail voltage monitoring. Besides, the nRESET delay of the SGM820 has a high-precision delay timing. And combined with its accurate voltage monitoring hysteresis, the SGM820 is very suitable for strict tolerance systems.

The SGM820 has a programmable watchdog timer. Users can program the timeouts through an external capacitor or the default factory settings. In addition, users can disable the watchdog through logic pins to prevent accidental timeouts during development.

The SGM820 is available in Green TDFN-3×3-8L and TDFN-2×2-8L packages. It operates over an ambient temperature range of -40℃ to +125℃.

FEATURES

- **Precision Fixed Detection Options for 1.8V, 2.5V, 3V, 3.3V and 5V system Systems**
- **High-Accuracy Voltage Threshold (< 1%)**
- **Hysteresis Characteristics: 0.5% (TYP)**
- **Supply Voltage Range: 1.6V to 6.5V**
- **Ultra-Low Supply Current: 1.2μA (TYP)**
- **High-Accuracy Reset Delay**
- **nRESET Delay Time and Watchdog Active Time: 200ms (TYP)**
- **High-Accuracy User-Programmable Watchdog Timer:**
  - **Standard Version: SGM820A**
  - **Extended Version: SGM820B**
- **Watchdog Disable Function**
- **Available Manual Reset Input (nMR)**
- **Open-Drain nRESET Output**
- **Available in Green TDFN-3×3-8L and TDFN-2×2-8L Packages**

APPLICATIONS

Safety Applications
Precision Industrial System
Controllers
DSPs, FPGAs and ASICs

TYPICAL APPLICATION

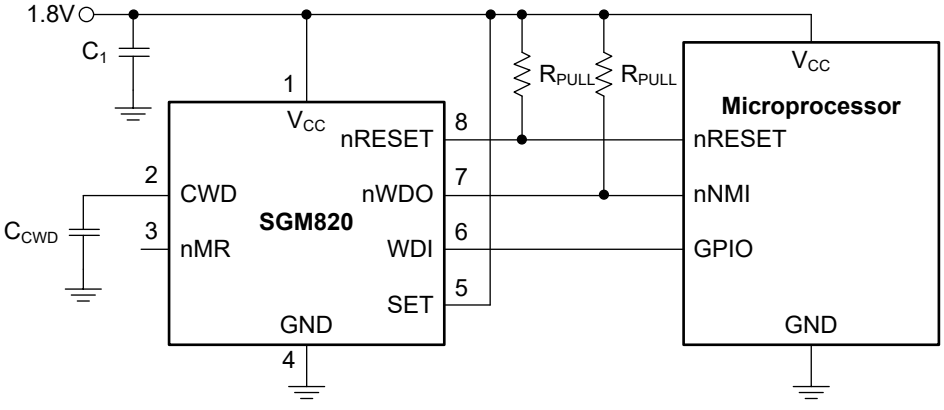


Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	UNDER-VOLTAGE THRESHOLD (V)	PACKAGE DESCRIPTION	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM820A-4.8	4.800	TDFN-3×3-8L	SGM820A-4.8XTDB8G/TR	SGM MKBDB XXXXX	Tape and Reel, 4000
	4.800	TDFN-2×2-8L	SGM820A-4.8XTDE8G/TR	MJ1 XXXX	Tape and Reel, 3000
SGM820B-4.8	4.800	TDFN-3×3-8L	SGM820B-4.8XTDB8G/TR	SGM ML5DB XXXXX	Tape and Reel, 4000
	4.800	TDFN-2×2-8L	SGM820B-4.8XTDE8G/TR	MJB XXXX	Tape and Reel, 3000
SGM820A-4.6	4.650	TDFN-3×3-8L	SGM820A-4.6XTDB8G/TR	SGM MKADB XXXXX	Tape and Reel, 4000
	4.650	TDFN-2×2-8L	SGM820A-4.6XTDE8G/TR	MJ0 XXXX	Tape and Reel, 3000
SGM820B-4.6	4.650	TDFN-3×3-8L	SGM820B-4.6XTDB8G/TR	SGM ML4DB XXXXX	Tape and Reel, 4000
	4.650	TDFN-2×2-8L	SGM820B-4.6XTDE8G/TR	MJA XXXX	Tape and Reel, 3000
SGM820A-3.1	3.168	TDFN-3×3-8L	SGM820A-3.1XTDB8G/TR	SGM MK9DB XXXXX	Tape and Reel, 4000
	3.168	TDFN-2×2-8L	SGM820A-3.1XTDE8G/TR	MIF XXXX	Tape and Reel, 3000
SGM820B-3.1	3.168	TDFN-3×3-8L	SGM820B-3.1XTDB8G/TR	SGM ML3DB XXXXX	Tape and Reel, 4000
	3.168	TDFN-2×2-8L	SGM820B-3.1XTDE8G/TR	MJ9 XXXX	Tape and Reel, 3000
SGM820A-3.0	3.069	TDFN-3×3-8L	SGM820A-3.0XTDB8G/TR	SGM MK8DB XXXXX	Tape and Reel, 4000
	3.069	TDFN-2×2-8L	SGM820A-3.0XTDE8G/TR	MIE XXXX	Tape and Reel, 3000
SGM820B-3.0	3.069	TDFN-3×3-8L	SGM820B-3.0XTDB8G/TR	SGM ML2DB XXXXX	Tape and Reel, 4000
	3.069	TDFN-2×2-8L	SGM820B-3.0XTDE8G/TR	MJ8 XXXX	Tape and Reel, 3000
SGM820A-2.8	2.880	TDFN-3×3-8L	SGM820A-2.8XTDB8G/TR	SGM MK7DB XXXXX	Tape and Reel, 4000
	2.880	TDFN-2×2-8L	SGM820A-2.8XTDE8G/TR	MID XXXX	Tape and Reel, 3000
SGM820B-2.8	2.880	TDFN-3×3-8L	SGM820B-2.8XTDB8G/TR	SGM ML1DB XXXXX	Tape and Reel, 4000
	2.880	TDFN-2×2-8L	SGM820B-2.8XTDE8G/TR	MJ7 XXXX	Tape and Reel, 3000

PACKAGE/ORDERING INFORMATION (continued)

MODEL	UNDER-VOLTAGE THRESHOLD (V)	PACKAGE DESCRIPTION	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM820A-2.7	2.790	TDFN-3×3-8L	SGM820A-2.7XTDB8G/TR	SGM MK6DB XXXXX	Tape and Reel, 4000
	2.790	TDFN-2×2-8L	SGM820A-2.7XTDE8G/TR	MIC XXXX	Tape and Reel, 3000
SGM820B-2.7	2.790	TDFN-3×3-8L	SGM820B-2.7XTDB8G/TR	SGM ML0DB XXXXX	Tape and Reel, 4000
	2.790	TDFN-2×2-8L	SGM820B-2.7XTDE8G/TR	MJ6 XXXX	Tape and Reel, 3000
SGM820A-2.4	2.400	TDFN-3×3-8L	SGM820A-2.4XTDB8G/TR	SGM MK5DB XXXXX	Tape and Reel, 4000
	2.400	TDFN-2×2-8L	SGM820A-2.4XTDE8G/TR	MIB XXXX	Tape and Reel, 3000
SGM820B-2.4	2.400	TDFN-3×3-8L	SGM820B-2.4XTDB8G/TR	SGM MKFDB XXXXX	Tape and Reel, 4000
	2.400	TDFN-2×2-8L	SGM820B-2.4XTDE8G/TR	MJ5 XXXX	Tape and Reel, 3000
SGM820A-2.3	2.325	TDFN-3×3-8L	SGM820A-2.3XTDB8G/TR	SGM MK4DB XXXXX	Tape and Reel, 4000
	2.325	TDFN-2×2-8L	SGM820A-2.3XTDE8G/TR	MI9 XXXX	Tape and Reel, 3000
SGM820B-2.3	2.325	TDFN-3×3-8L	SGM820B-2.3XTDB8G/TR	SGM MKEDB XXXXX	Tape and Reel, 4000
	2.325	TDFN-2×2-8L	SGM820B-2.3XTDE8G/TR	MJ4 XXXX	Tape and Reel, 3000
SGM820A-1.7	1.728	TDFN-3×3-8L	SGM820A-1.7XTDB8G/TR	SGM MK2DB XXXXX	Tape and Reel, 4000
	1.728	TDFN-2×2-8L	SGM820A-1.7XTDE8G/TR	MI7 XXXX	Tape and Reel, 3000
SGM820B-1.7	1.728	TDFN-3×3-8L	SGM820B-1.7XTDB8G/TR	SGM MKDDB XXXXX	Tape and Reel, 4000
	1.728	TDFN-2×2-8L	SGM820B-1.7XTDE8G/TR	MJ3 XXXX	Tape and Reel, 3000
SGM820A-1.6	1.674	TDFN-3×3-8L	SGM820A-1.6XTDB8G/TR	SGM MK1DB XXXXX	Tape and Reel, 4000
	1.674	TDFN-2×2-8L	SGM820A-1.6XTDE8G/TR	MI6 XXXX	Tape and Reel, 3000
SGM820B-1.6	1.674	TDFN-3×3-8L	SGM820B-1.6XTDB8G/TR	SGM MKCDB XXXXX	Tape and Reel, 4000
	1.674	TDFN-2×2-8L	SGM820B-1.6XTDE8G/TR	MJ2 XXXX	Tape and Reel, 3000

NOTES:

SGM820A-X provide standard user-programming watchdog timeout: $t_{WD\_standard}$ (ms) = 3.33 × C_{CWD} (nF) + 0.28 (ms)

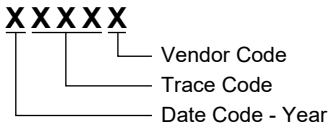
SGM820B-X provide extended user-programming watchdog timeout: $t_{WD\_extended}$ (ms) = 78.3 × C_{CWD} (nF) + 51 (ms)

PACKAGE/ORDERING INFORMATION (continued)

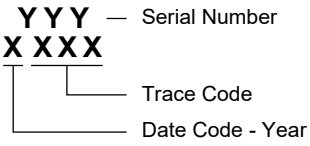
MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XXXX = Date Code and Trace Code.

TDFN-3×3-8L



TDFN-2×2-8L



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{CC} ..... -0.3V to 7V
Output Voltage Range
nRESET, nWDO .....-0.3V to 7V
Voltage Ranges
SET, WDI, nMR.....-0.3V to 7V
CWD.....-0.3V to V_{CC} + 0.3V
Output Pin Current
nRESET, nWDO ..... ±20mA
Input Current (All Pins) ..... ±20mA
Package Thermal Resistance
TDFN-3×3-8L, θ_{JA} .....60.6℃/W
TDFN-3×3-8L, θ_{JB} .....34.9℃/W
TDFN-3×3-8L, $\theta_{JC(TOP)}$.....66.7℃/W
TDFN-3×3-GL, $\theta_{JC(BOT)}$.....21.9℃/W
TDFN-2×2-8L, θ_{JA} .....89.7℃/W
TDFN-2×2-8L, θ_{JB} .....53.4℃/W
TDFN-2×2-8L, $\theta_{JC(TOP)}$.....103.5℃/W
TDFN-2×2-8L, $\theta_{JC(BOT)}$.....22.3℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Pin Voltage, V_{CC}.....1.6V to 6.5V
SET Pin Voltage, V_{SET}.....0V to 6.5V
Watchdog Timing Capacitor, C_{CWD}..... 0.1nF to 1000nF (1)
Pull-Up Resistor to V_{CC}, CWD.....9kΩ to 11kΩ
Pull-Up Resistor, nRESET and nWDO, R_{PULL}.....
.....1kΩ to 100kΩ
nRESET Pin Current, I_{nRESET} 10mA
Watchdog Output Current, I_{nWDO}..... 10mA
Junction Temperature Range ..... -40℃ to +125℃
Ambient Temperature Range ..... -40℃ to +125℃

NOTE:
1. It is recommended to use the standard timing with a C_{CWD} capacitor from 0.1nF to 1000nF, and it offers t_{WD_TYP} from 0.613ms to 3.33s accordingly. If using extended timing, it offers t_{WD_TYP} from 58.83ms to 78.35s accordingly.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

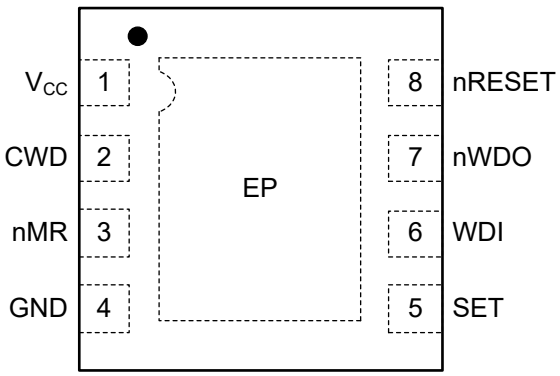
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS

(TOP VIEW)



TDFN-3×3-8L/TDFN-2×2-8L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	V_{CC}	I	Supply Voltage Pin. It is recommended to place a 0.1μF ceramic capacitor close to this pin.
2	CWD	I	Programmable Watchdog Timeout Input Pin. Connecting the CWD pin to GND via a capacitor to set the adjustable watchdog timeout. Connecting the CWD pin to V_{CC} via a 10kΩ resistor or leaving it unconnected to select two different kinds of the preset watchdog timeout.
3	nMR	I	Manual Reset Input Pin. It is an active-low reset input with internal pull-up current.
4	GND	G	Ground.
5	SET	I	Logic Input Pin. Connecting the SET pin to GND will disable the watchdog timer. If nRESET is deaseerted, the wactchdog can be enabled when SET is high.
6	WDI	I	Watchdog Input Pin. The WDI falling edge must appear within the timeout (t_{WD}) period. When nWDO or nRESET is low and the watchdog is disabled, WDI will be ignored. Note that this pin cannot be left floating.
7	nWDO	O	Watchdog Open-Drain Output Pin. It is recommended to connect a resistor from 1kΩ to 100kΩ to the rail. If the watchdog timeout occurs, the nWDO goes low for an nRESET timeout delay (t_{RST}).
8	nRESET	O	Active-Low Open-Drain Reset Output Pin. It is recommended to connect a resistor from 1kΩ to 100kΩ to the rail. nRESET remains low if V_{CC} is below the under-voltage threshold (V_{ITN}). And it goes high when V_{CC} exceeds V_{ITN} + V_{HYS} after nRESET delay time (t_{RST}).
Exposed Pad	EP	G	Exposed Pad. This pad is not connected to internal circuit.

NOTE: I: Input, O: Output, G: Ground.

ELECTRICAL CHARACTERISTICS

(V_{ITN} + V_{HYS} ≤ V_{CC} ≤ 6.5V, Full = -40℃ to +125℃, the open-drain pull-up resistors are 10kΩ for each output, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
General Characteristics							
Power Supply Voltage	V_{CC} (1) (2)		Full	1.6		6.5	V
Supply Current	I_{CC}		Full		1.2	3.3	μA
Reset Function							
Power-On Reset Voltage	V_{POR} (1)	I_{nRESET} = 15μA, $V_{OL(MAX)}$ = 0.25V	Full			0.8	V
Under-Voltage Threshold	V_{ITN}	SGM820A/B-4.8, V_{CC} falling	Full	4.757	4.800	4.843	V
		SGM820A/B-4.6, V_{CC} falling	Full	4.608	4.650	4.692	
		SGM820A/B-3.1, V_{CC} falling	Full	3.139	3.168	3.197	
		SGM820A/B-3.0, V_{CC} falling	Full	3.041	3.069	3.097	
		SGM820A/B-2.8, V_{CC} falling	Full	2.854	2.880	2.906	
		SGM820A/B-2.7, V_{CC} falling	Full	2.765	2.790	2.815	
		SGM820A/B-2.4, V_{CC} falling	Full	2.377	2.400	2.423	
		SGM820A/B-2.3, V_{CC} falling	Full	2.303	2.325	2.347	
		SGM820A/B-1.7, V_{CC} falling	Full	1.711	1.728	1.745	
		SGM820A/B-1.6, V_{CC} falling	Full	1.658	1.674	1.690	
Hysteresis Voltage	V_{HYS}	V_{CC} rising	Full	0.15% × V_{ITN}	0.50% × V_{ITN}	0.85% × V_{ITN}	V
nMR Pin Internal Pull-Up Current	I_{nMR}	V_{nMR} = 0V	Full	520	620	720	nA
Watchdog Function							
CWD Pin Charging Current	I_{CWD}	CWD = 0.5V	Full	337	375	413	nA
CWD Pin Threshold Voltage	V_{CWD}		Full	1.180	1.210	1.245	V
nRESET, nWDO Output Low	V_{OL}	V_{CC} = 5V, I_{SINK} = 3mA	Full			0.4	V
nRESET, nWDO Output Leakage Current, Open-Drain	I_D	V_{CC} = V_{ITN} + V_{HYS}, V_{nRESET} = V_{nWDO} = 6.5V	Full			1	μA
Low-Level Input Voltage of nMR	V_{IL_nMR}		Full			0.25	V
High-Level Input Voltage of nMR	V_{IH_nMR}		Full	0.8			V
Low-Level Input Voltage of SET	V_{IL_SET}		Full			0.25	V
High-Level Input Voltage of SET	V_{IH_SET}		Full	0.8			V
Low-Level Input Voltage of WDI	V_{IL_WDI}		Full			0.3 × V_{CC}	V
High-Level Input Voltage of WDI	V_{IH_WDI}		Full	0.8 × V_{CC}			V

NOTES:
1. When V_{CC} is lower than V_{POR}, nRESET and nWDO are not defined.
2. During power-on, V_{CC} must be 1.6V (MIN) for at least 400μs before nRESET correlates with V_{CC}.

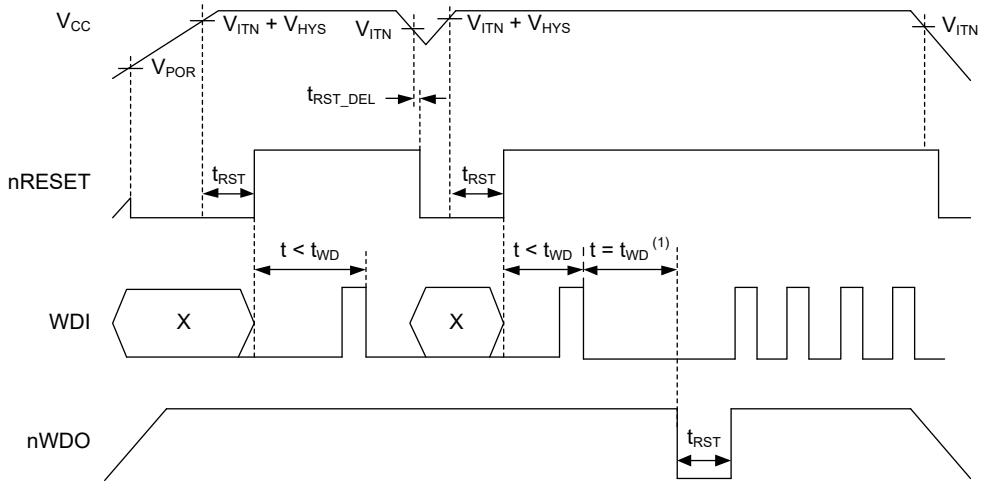
TIMING REQUIREMENTS

(At T_A = +25℃, V_{ITN} + V_{HYS} ≤ V_{CC} ≤ 6.5V, Full = -40℃ to +125℃, the open-drain pull-up resistors are 10kΩ for each output, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
General							
CWD Pin Evaluation Period	t_{INIT}		+25℃		390		μs
Minimum nMR Pin Pulse Duration			+25℃		1		μs
Reset Function							
nRESET Timeout Period	t_{RST}		Full	170	200	230	ms
V_{CC} to nRESET Delay	t_{RST_DEL}	V_{CC} = (V_{ITN} + V_{HYS}) × (1 + 2.5%) to V_{ITN} × (1 - 2.5%)	+25℃		90		μs
nMR to nRESET Delay	t_{MR_DEL}		+25℃		700		ns
Watchdog Function							
Watchdog Timeout (1)	t_{WD}	CWD = NC, SET = 0 (2)	Watchdog disabled				
		CWD = NC, SET = 1 (2)	Full	1360	1600	1840	ms
		CWD = 10kΩ to V_{CC}, SET = 0 (2)	Watchdog disabled				
		CWD = 10kΩ to V_{CC}, SET = 1 (2)	Full	170	200	230	ms
Set-Up Time Required for Device to Respond to Changes on WDI after Being Enabled	t_{WD_SETUP}		+25℃		140		μs
Minimum WDI, nMR Pin Pulse Duration			+25℃		50		ns
WDI to nWDO Delay	t_{WD_DEL}		+25℃		100		ns

NOTES:
1. The fixed watchdog timing covers both standard version and extended version.
2. SET = 0 means V_{SET} < V_{IL_SET}; SET = 1 means V_{SET} > V_{IH_SET}.

TIMING DIAGRAM



NOTE:
1. See Figure 3 for WDI timing requirements.

Figure 2. Timing Diagram

TIMING DIAGRAM (continued)

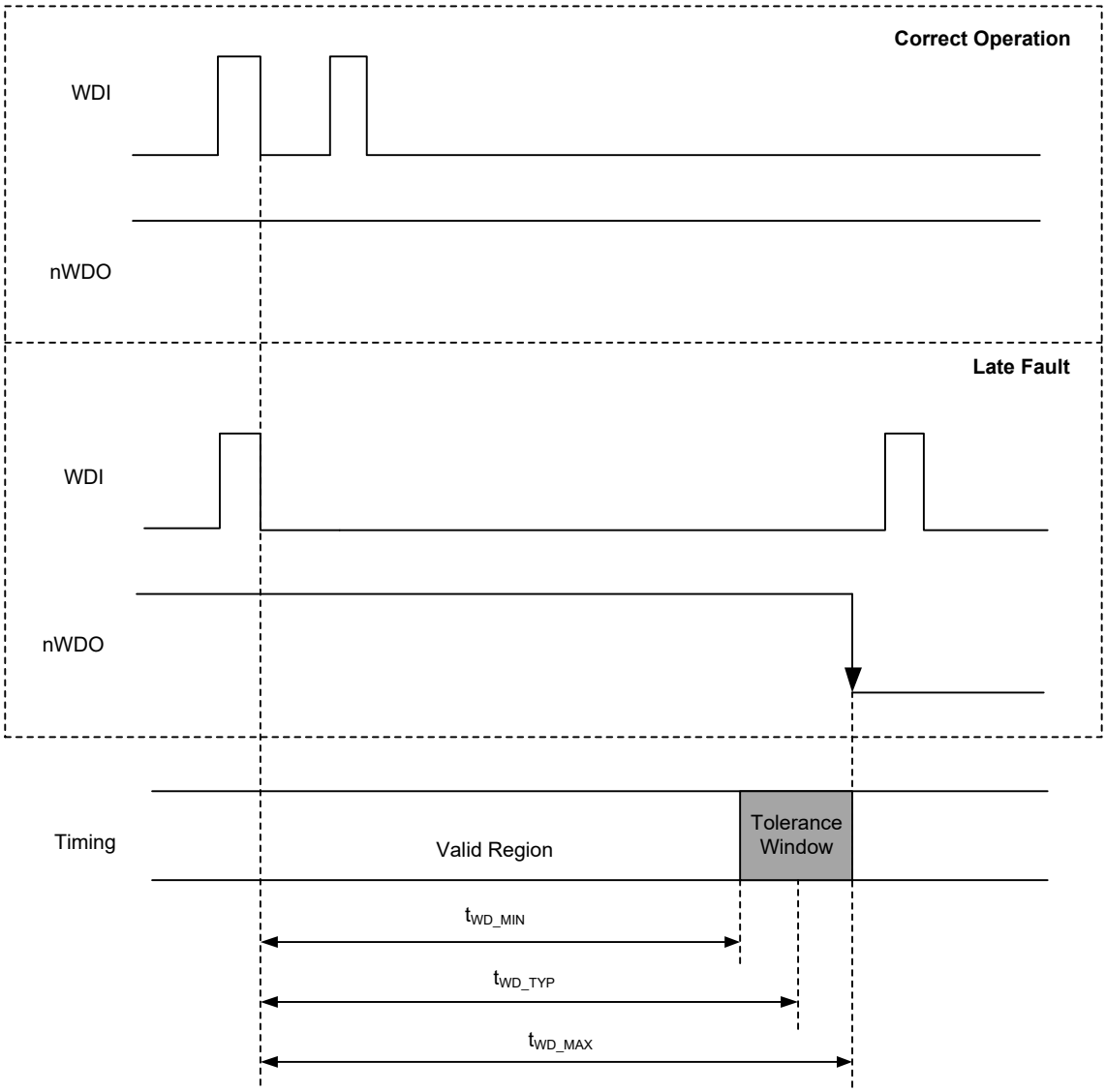
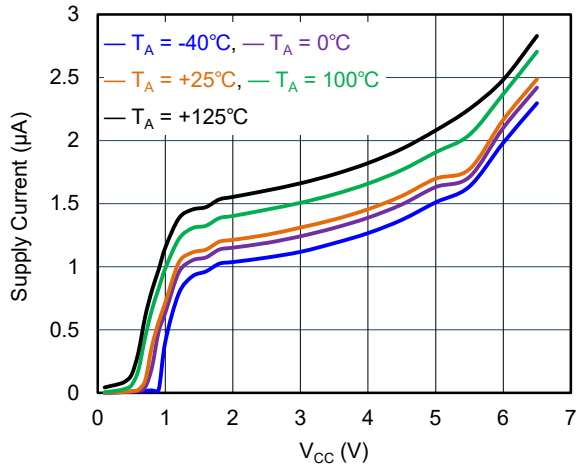


Figure 3. Watchdog Timing Diagram

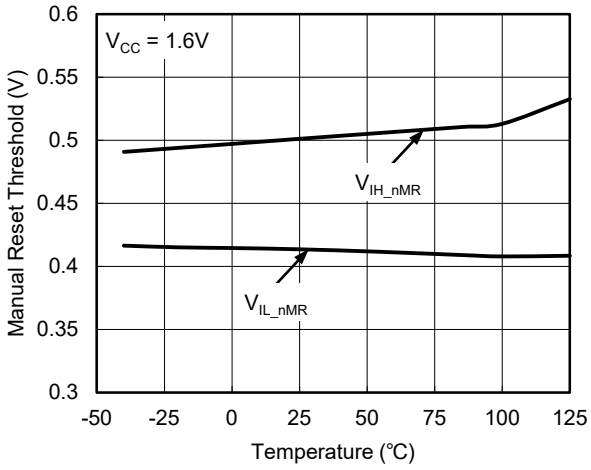
TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = +25℃, 1.6V ≤ V_{CC} ≤ 6.5V, unless otherwise noted.

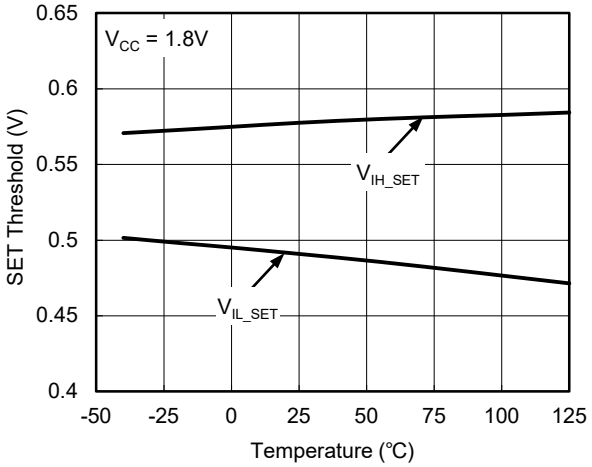
Supply Current vs. Supply Voltage



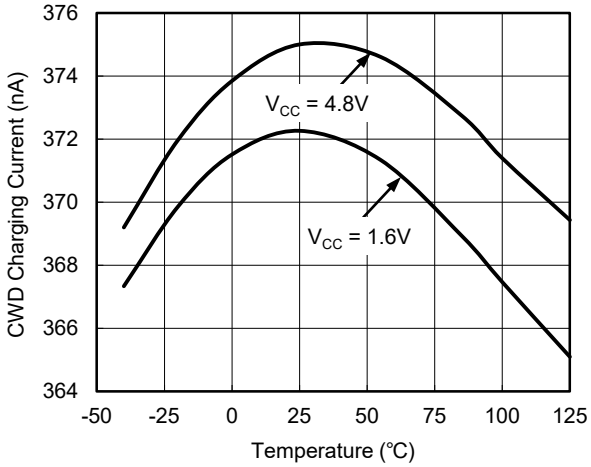
nMR Threshold vs. Temperature



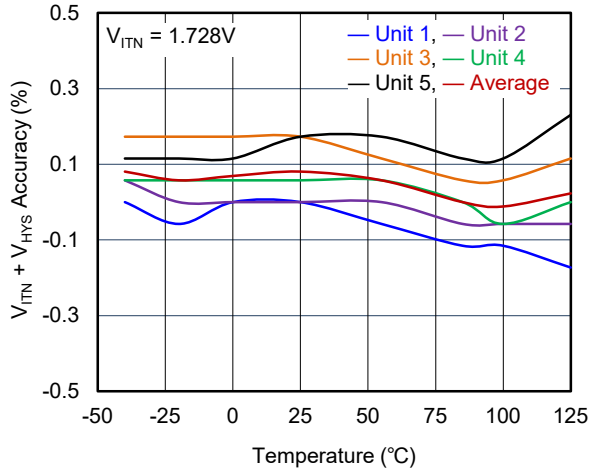
SET Threshold vs. Temperature



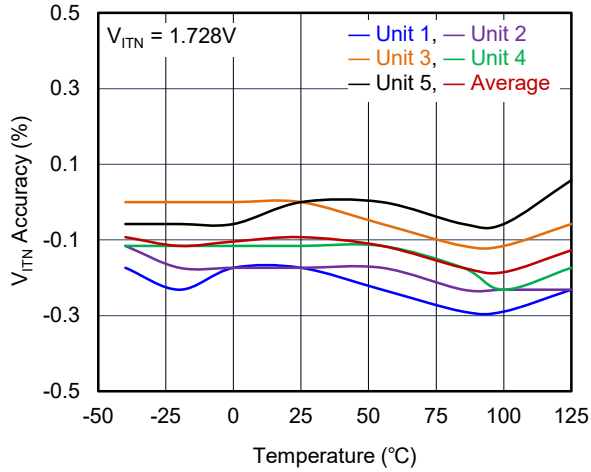
CWD Charging Current vs. Temperature



V_{ITN} + V_{HYS} Accuracy vs. Temperature



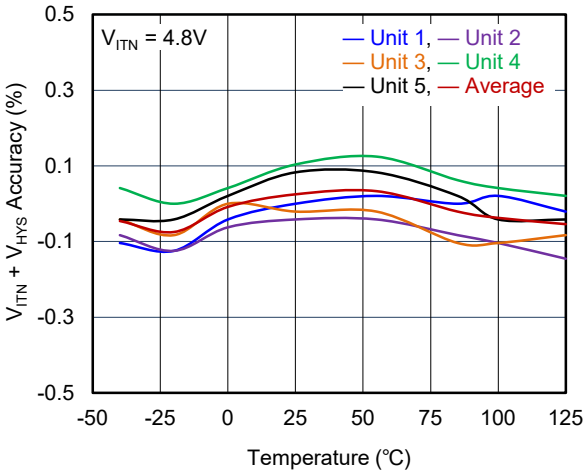
V_{ITN} Accuracy vs. Temperature



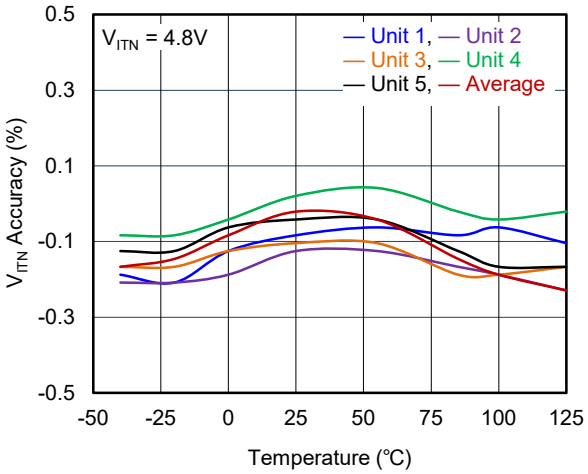
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, 1.6V ≤ V_{CC} ≤ 6.5V, unless otherwise noted.

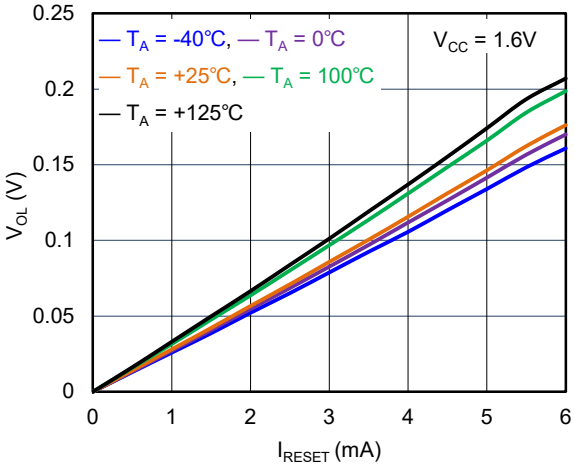
V_{ITN} + V_{HYS} Accuracy vs. Temperature



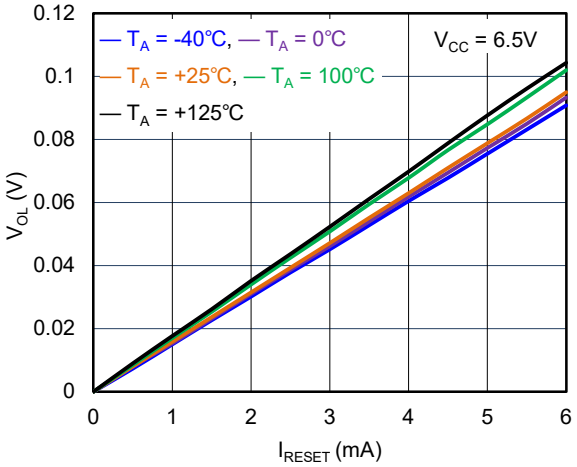
V_{ITN} Accuracy vs. Temperature



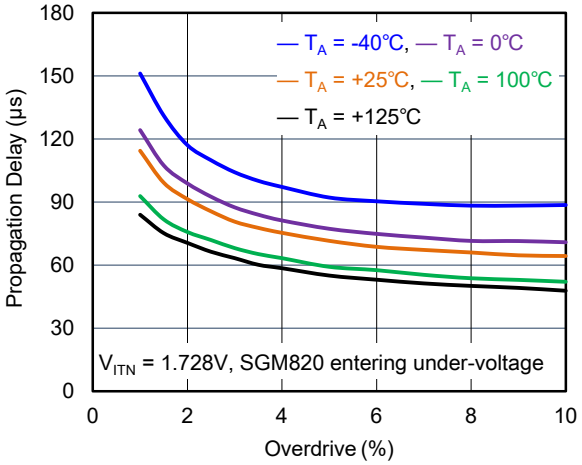
Low-Level nRESET Voltage vs. nRESET Current



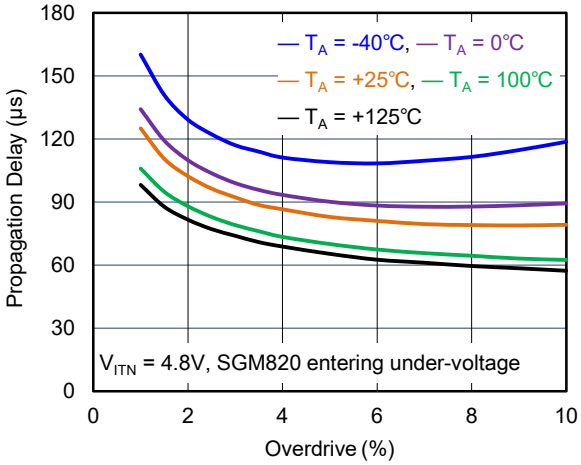
Low-Level nRESET Voltage vs. nRESET Current



Propagation Delay vs. Overdrive



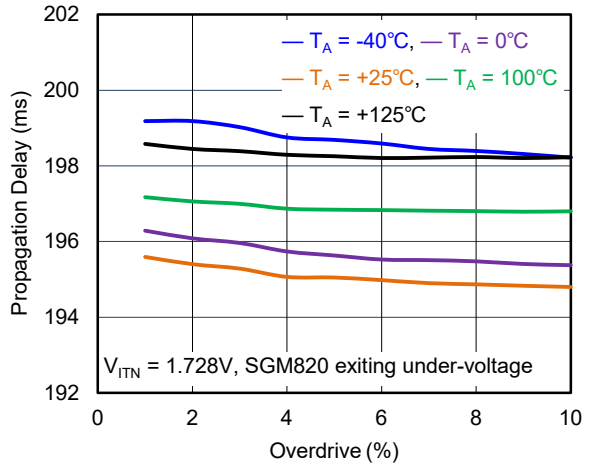
Propagation Delay vs. Overdrive



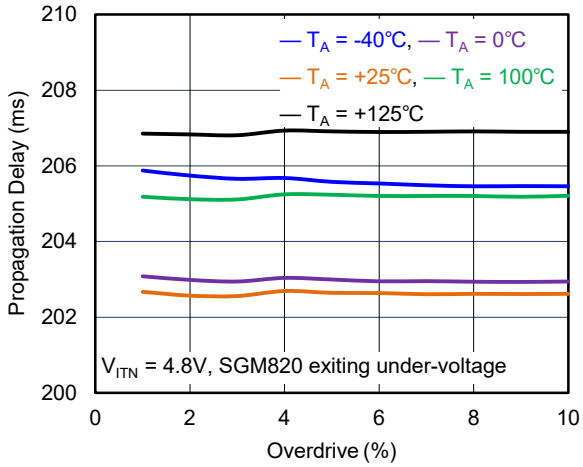
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, 1.6V ≤ V_{CC} ≤ 6.5V, unless otherwise noted.

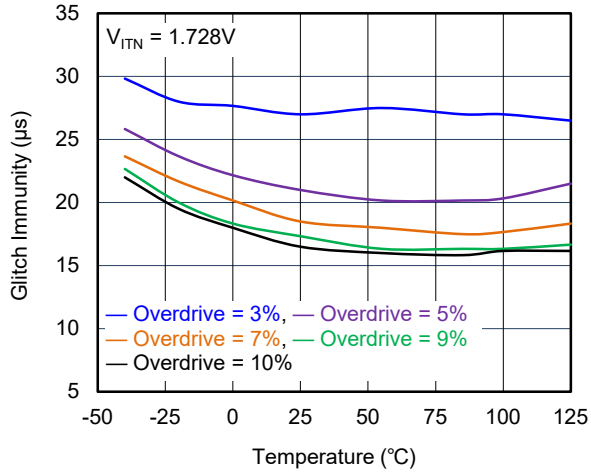
Propagation Delay (t_{RST}) vs. Overdrive



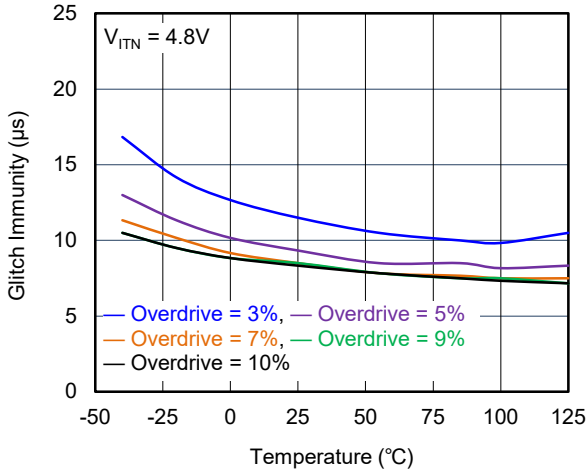
Propagation Delay (t_{RST}) vs. Overdrive



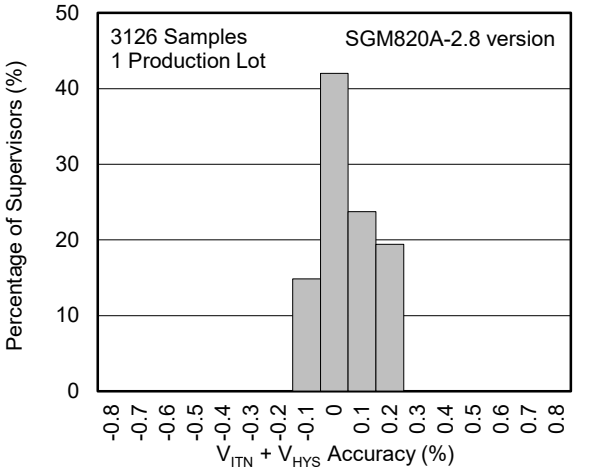
High-to-Low Glitch Immunity vs. Temperature



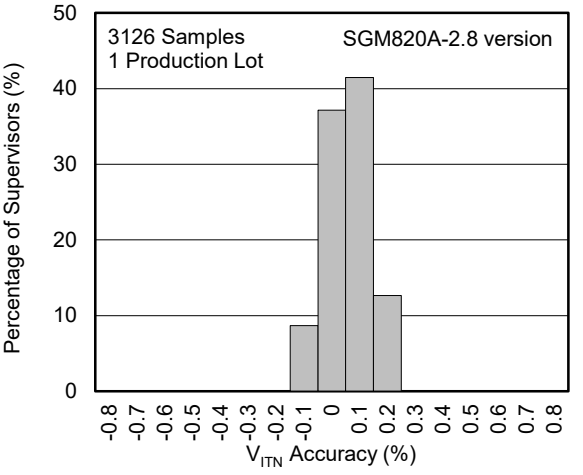
High-to-Low Glitch Immunity vs. Temperature



V_{ITN} + V_{HYS} Accuracy Histogram

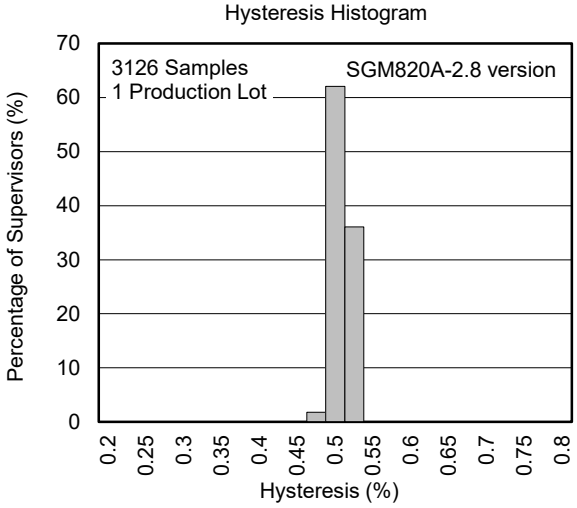


V_{ITN} Accuracy Histogram



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, 1.6V ≤ V_{CC} ≤ 6.5V, unless otherwise noted.



FUNCTIONAL BLOCK DIAGRAM

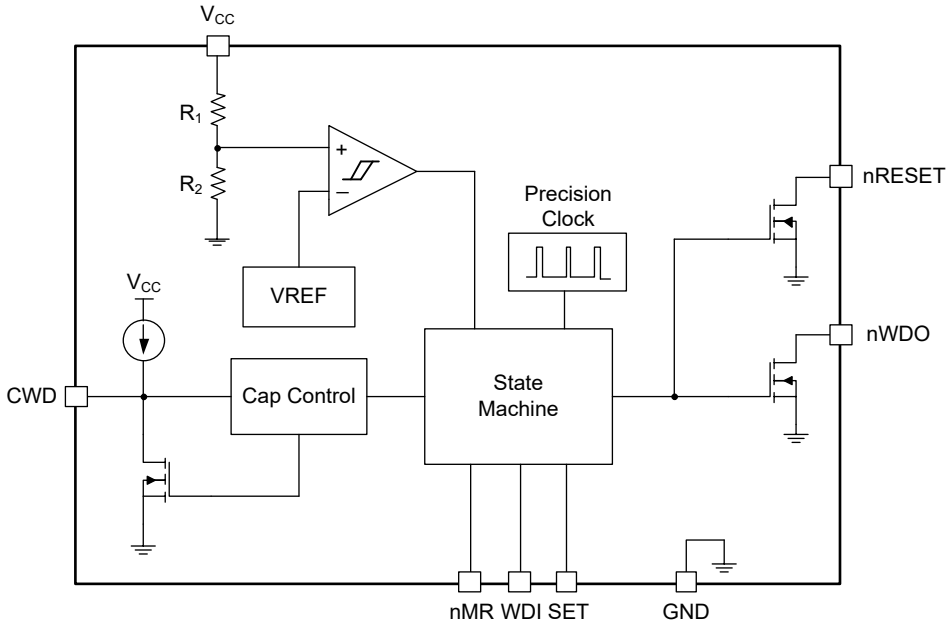


Figure 4. SGM820 Block Diagram

DETAILED DESCRIPTION

Overview

The SGM820 is a high-precision voltage supervisor, integrated with an accurate watchdog timer in the specified temperature range of -40℃ to +125℃. Besides, it ensures an accurate hysteresis on the threshold, which makes it very suitable for systems that need small tolerance. And two options are provided to set the watchdog timing: a standard version and an extended one.

nRESET

The nRESET is an open-drain output pin, and users should connect the nRESET pin to V_{CC} or another voltage rail through a pull-up resistor of 1kΩ to 100kΩ. Once V_{CC} falls below the under-voltage threshold (V_{ITN}), the nRESET is asserted to be low. And if V_{CC} exceeds V_{ITN} + V_{HYS}, the nRESET will keep low for a specified reset delay time (t_{RST}). And then, the nRESET pin goes high with the pull-up resistor. Users should carefully consider the factors such as capacitive loading, logic low output voltage (V_{OL}), leakage current (I_D) and the current through the nRESET pin (I_{nRESET}) to select appropriate resistance values. It ensures that the high and low output voltage values meet the requirements of subsequent applications.

Manual Reset (nMR)

The manual reset input (nMR) is logic low effective, and it can be used to initiate a reset by a processor or some other logic circuits. The nRESET is deasserted after t_{RST} if nMR becomes high and V_{CC} is above V_{ITN} + V_{HYS}. Knowing that the nMR pin is pulled up internally, connect nMR to V_{CC} or just leave it floating once it is unnecessary to control it externally.

Under-Voltage Detection

The SGM820 provides various under-voltage threshold voltage options for 1.8V, 2.5V, 3V, 3.3V and 5V system rail voltage monitoring. As is shown in Figure 5, when V_{CC} is below V_{ITN}, the nRESET is asserted and remains low. And when V_{CC} is higher than V_{ITN} + V_{HYS}, the nRESET deasserts after t_{RST}.

The hysteresis of the built-in comparator can immune some noise of the system. However, it is strongly recommended to place a bypass capacitor of 0.1μF to 100nF near the V_{CC} pin to immune the transient voltage and ensure stable operation.

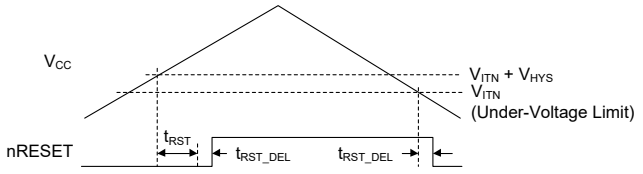


Figure 5. Under-Voltage Detection

Watchdog Mode

Details about the principles of the watchdog mode are provided in this part.

CWD

Through the CWD pin, users can obtain a high-precision and preset watchdog timing in factory or a programmed one. There are three options of the SGM820 to configure the watchdog timer. Keep CWD pin floating or pull up a 10kΩ resistor to V_{CC} to set two different factory-programmed timers. Connect a capacitor between the CWD pin and GND to achieve an adjustable timer. Every time when V_{CC} exceeds the V_{ITN} + V_{HYS}, the device checks the CWD configuration state within t_{INIT} (about 390μs, TYP). During this time, an internal state machine is used to check the CWD pin state and lock it out until nRESET is asserted or powered off.

Watchdog Input (WDI)

The WDI pin is the falling-edge triggered watchdog timer input pin. The WDI pulse should be sent out within t_{WD_MIN}, and the pulse of WDI should be at least larger than 50ns to ensure that the pulse can be detected by the device. If a valid WDI is received, the nWDO remains deasserted. If not, the nWDO is asserted to be low.

The WDI is a logic input pin and it cannot be left floating. Users should drive WDI to either V_{CC} or GND to avoid the increasing current of the supply current. When nRESET is asserted, the watchdog function is disabled and any signals cannot be recognized by the device. When nRESET is deasserted, the device operates normally and the WDI signals can be recognized. Figure 6 shows that a valid WDI pulse can prevent nWDO from being triggered low.

DETAILED DESCRIPTION (continued)

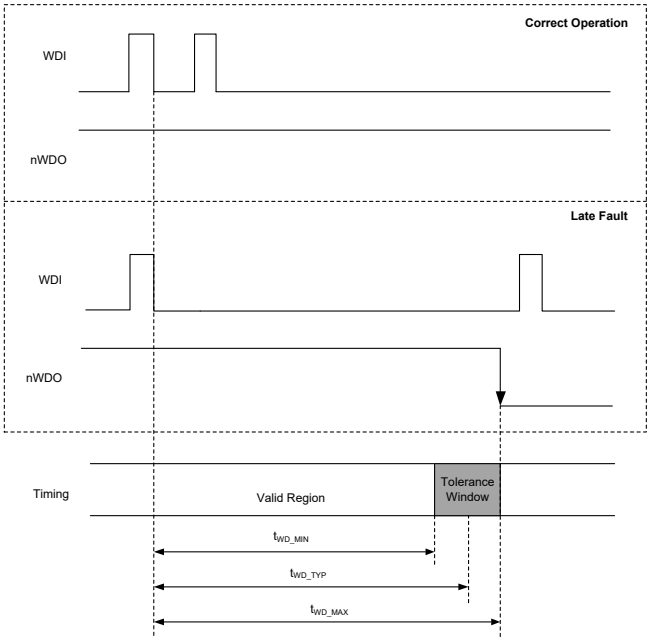


Figure 6. Watchdog Timing Diagram

Watchdog Output (nWDO)

The nWDO is the independent watchdog output pin, and it can issue a fault flag in the watchdog timing with no need to trigger an nRESET signal, which is always used to reset the whole system. When nRESET is deasserted, the nWDO keeps normal operation and it asserts to be low for t_{RST} if no valid WDI is triggered within the valid watchdog timing region. And when the nRESET signal is asserted by some other reasons, the nWDO pin goes high if a resistor is connected to V_{CC} or another rail. When the nRESET signal is deasserted again, the watchdog timer returns back to normal operation.

SET

The watchdog timer can be enabled or disabled by the SET pin. When the SET pin is connected to GND, the watchdog timer is disabled and signals in WDI are not recognized. Once the watchdog timer is disabled, connect WDI to V_{CC} or GND to prevent any increase of I_{CC}. When the SET pin is set to logic high, and if nRESET is not asserted, the watchdog operates properly. The SET pin is permitted to continuously change the value. However, as shown in Figure 7, there is a 140μs (TYP) time for the set-up of watchdog if the watchdog runs from disabled to enabled. During this period, no response can be detected on WDI by the watchdog.

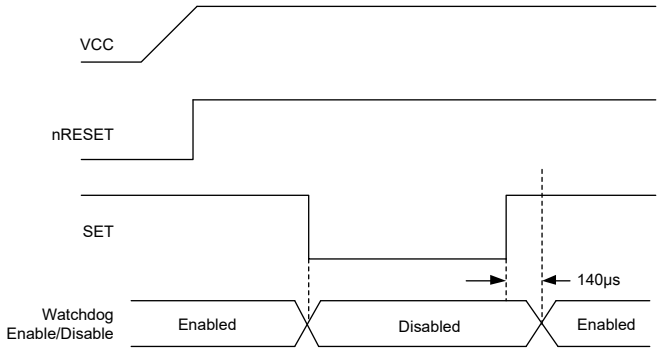


Figure 7. Enabling and Disabling the Watchdog

Device Functional Modes

The functional modes of the SGM820 are shown in Table 1.

Table 1. Device Functional Modes

V_{CC}	WDI	nWDO	nRESET
$V_{CC} < V_{POR}$	—	—	Undefined
$V_{POR} \le V_{CC} < V_{CC\_MIN}$	Ignored	H	L
$V_{CC\_MIN} \le V_{CC} \le V_{ITN} + V_{HYS}$ (1)	Ignored	H	L
$V_{CC} > V_{ITN}$ (2)	$t_{PULSE} < t_{WD\_MIN}$ (3)	H	H
$V_{CC} > V_{ITN}$ (2)	$t_{PULSE} > t_{WD\_MIN}$ (3)	L	H

NOTES:

1. Only valid before V_{CC} exceeds $V_{ITN} + V_{HYS}$.
2. Only valid after V_{CC} exceeds $V_{ITN} + V_{HYS}$.
3. t_{PULSE} is the time between two falling edges on WDI.

V_{CC} is below V_{POR} ($V_{CC} < V_{POR}$)

When V_{CC} is below V_{POR}, the nRESET is not defined, which can be either logic high or logic low. At this time, the state of nRESET is greatly determined by the load floating across the nRESET pin.

Between Power-On-Reset and V_{CC_MIN} ($V_{POR} \le V_{CC} < V_{CC\_MIN}$)

When $V_{POR} \le V_{CC} < V_{CC\_MIN}$, the nRESET signal is asserted to logic low and the nWDO will turn into a high-impedance state regardless of the WDI signal.

Normal Operation ($V_{CC} \ge V_{CC\_MIN}$)

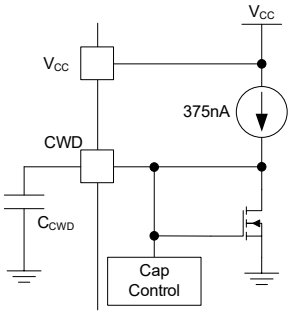
When V_{CC} is above or equal to V_{CC_MIN}, the nRESET signal is determined by V_{CC}. When the nRESET is asserted, the nWDO turns to a high-impedance state and then the nWDO is pulled high through the pull-up resistor.

APPLICATION INFORMATION

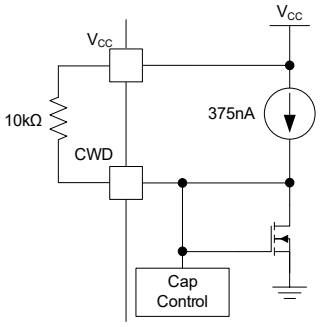
According to the eventual application requirements, the way to properly implement the device will be detailedly described in the following.

CWD Functionality

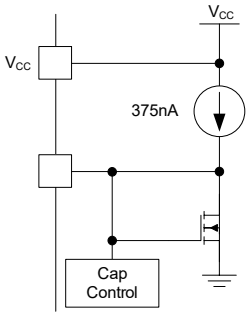
Figure 8 shows the schematic circuits of three options of the SGM820 to configure the watchdog timer. If connecting a 10kΩ pull-up resistor between CWD and V_{CC} or leave CWD floating (high-impedance), the factory-set watchdog timeouts are enabled, which can be seen from Table 2. Connect the capacitor between CWD and GND to set watchdog timing period using Equation 1 and 2.



a) User-Programmable Capacitor to GND



b) 10kΩ Resistor to VCC



c) CWD Unconnected

Figure 8. CWD Charging Circuit

Factory-Set Timing Options

As listed in Table 2, if the factory-set timing options are used, the CWD pin must be left floating or pull a 10kΩ resistor to V_{CC}.

Table 2. Factory-Set Watchdog Timing

Input		Standard and Extended Timing WDT (t_{WD})		
CWD	SET	MIN	TYP	MAX
NC	0	Watchdog disabled		
NC	1	1360ms	1600ms	1840ms
10kΩ to V_{CC}	0	Watchdog disabled		
10kΩ to V_{CC}	1	170ms	200ms	230ms

Adjustable Capacitor Timing

Capacitor timing can be adjusted by connecting the capacitor to the CWD pin, then a constant-current source of 375nA (TYP) begins to charge C_{CWD} until V_{CWD} = 1.210V (TYP). The watchdog timeout of SGM820 can be calculated as Equations 1 and 2, where C_{CWD} is in nF and t_{WD} is in ms.

For standard versions:

$$t_{WD\_standard}\,(ms) = 3.33 \times C_{CWD}\,(nF) + 0.28\,(ms) \quad (1)$$

For extended versions:

$$t_{WD\_extended}\,(ms) = 78.3 \times C_{CWD}\,(nF) + 51\,(ms) \quad (2)$$

The capacitors C_{CWD} used for design and test of the SGM820 should be between 100pF and 1μF. And Equations 1 and 2 are only accurate for ideal capacitors. Once the capacitor tolerances are considered, the obtained watchdog timeout may vary from the preset value. It is recommended using ceramic capacitors with C0G dielectric material to achieve higher accuracy. When a C_{CWD} capacitor is used, use Equation 1 to set t_{WD} for standard timing and use Equation 2 to set t_{WD} for extended timing.

APPLICATION INFORMATION (continued)

Overdrive Voltage

Enabling the nRESET depends on the following two factors. One factor is that the V_{CC} amplitude is above the trip point (ΔV_1 and ΔV_2), and the other factor is that the time length that the voltage is above the trip point (t_1 and t_2).

When V_{CC} is lower than the trip point for a long time, then the nRESET is asserted and the output is pulled low. When V_{CC} is just a few nanosecond lower than the trip point, the nRESET does not assert and the output continues to be high. Alter the time length that asserts the nRESET by increasing the proportion where V_{CC} is lower than the trip point. For example, when V_{CC} is 10% lower than the trip point, the comparator responds much faster and the nRESET is asserted much quicker than when just below the trip point voltage. Calculation of the percentage overdrive is shown in Equation 3.

$$\text{Overdrive} = |(V_{CC}/V_{ITX} - 1) \times 100\%| \quad (3)$$

Where V_{ITX} is the trip point voltage of the threshold. If V_{CC} is higher than the positive threshold, use V_{ITN} + V_{HYS} as V_{ITX}. If V_{CC} is lower than the under-voltage threshold, then V_{ITN} is considered. In Figure 9, t_1 and t_2 represent the period of time that V_{CC} is above or below the threshold, separately. And the propagation delay versus overdrive for V_{ITN} and V_{ITN} + V_{HYS} is illustrated as well.

Due to the overdrive voltage curve, the SGM820 is less sensitive to short positive or negative variations on V_{CC}.

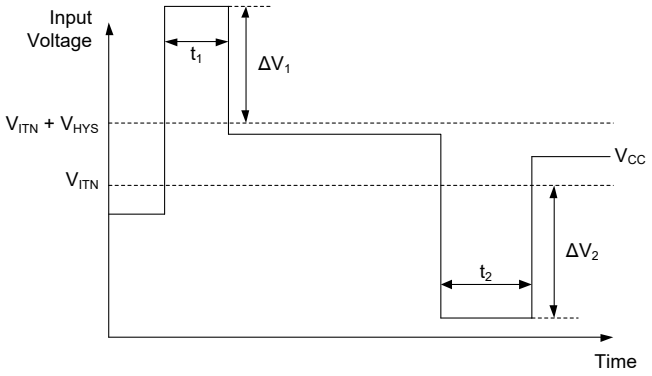


Figure 9. Overdrive Voltage

Power Supply Recommendations

The devices operate with a wide input range from 1.6V to 6.5V. A 0.1μF ceramic capacitor is recommended between the V_{CC} and GND pin to reduce the input supply noise.

REVISION HISTORY

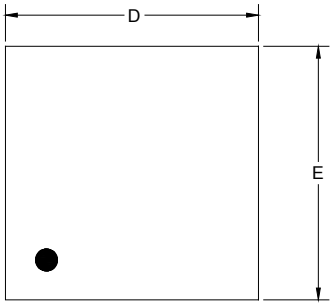
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

NOVEMBER 2024 – REV.A to REV.A.1	Page
Updated General Description section	1
Added Package Thermal Resistance information	4
Updated Detail Description section	13, 14
Updated Application Information section	15, 16

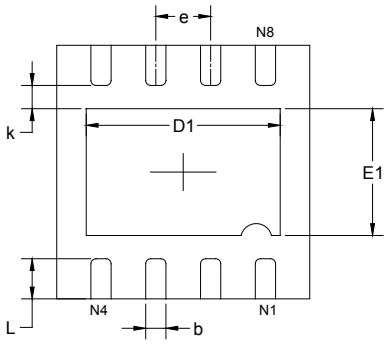
Changes from Original (JULY 2019) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

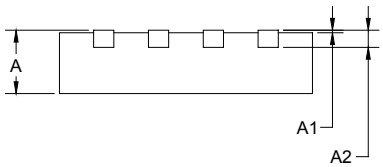
TDFN-3×3-8L



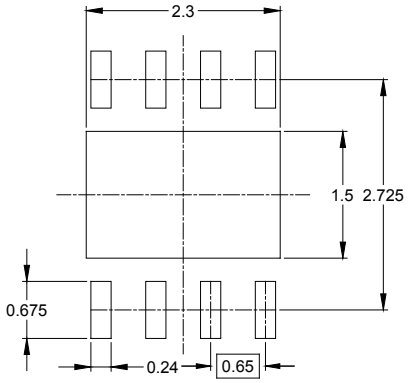
TOP VIEW



BOTTOM VIEW



SIDE VIEW

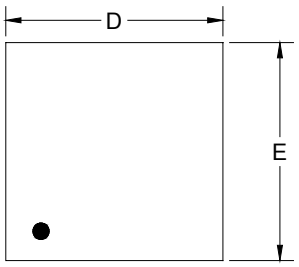


RECOMMENDED LAND PATTERN (Unit: mm)

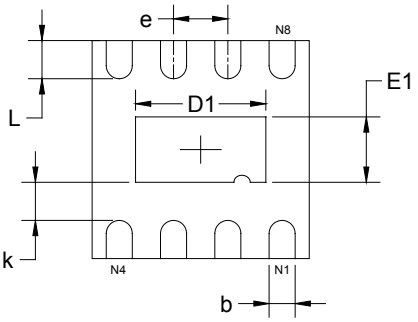
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	2.200	2.400	0.087	0.094
E	2.900	3.100	0.114	0.122
E1	1.400	1.600	0.055	0.063
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.650 TYP		0.026 TYP	
L	0.375	0.575	0.015	0.023

PACKAGE OUTLINE DIMENSIONS

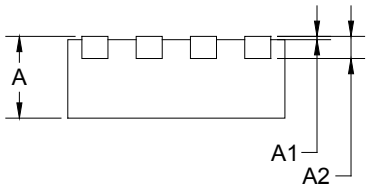
TDFN-2×2-8L



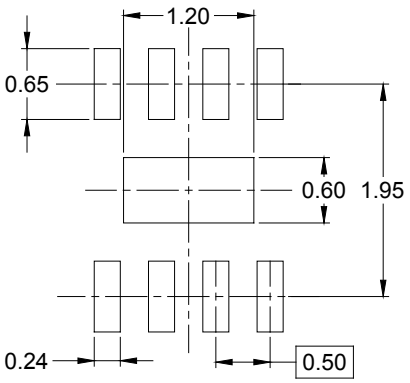
TOP VIEW



BOTTOM VIEW



SIDE VIEW

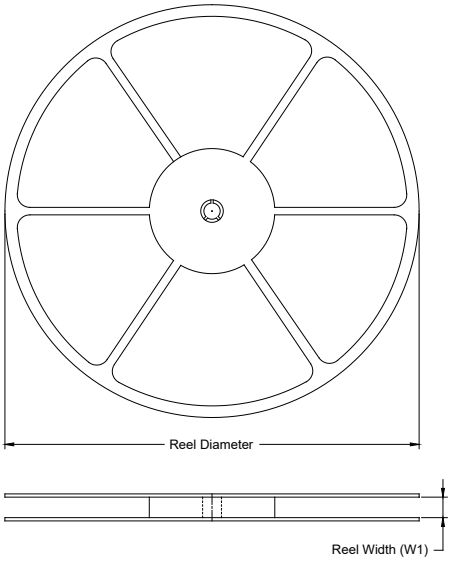


RECOMMENDED LAND PATTERN (Unit: mm)

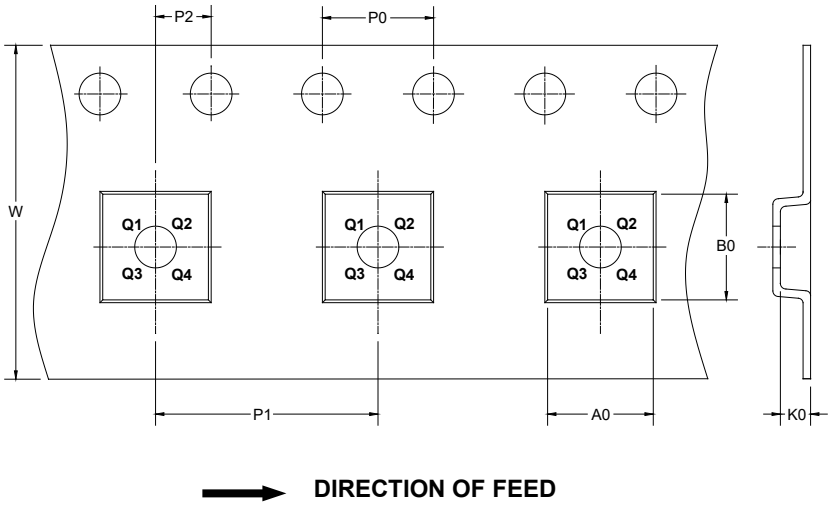
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	1.900	2.100	0.075	0.083
D1	1.100	1.300	0.043	0.051
E	1.900	2.100	0.075	0.083
E1	0.500	0.700	0.020	0.028
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.250	0.450	0.010	0.018

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



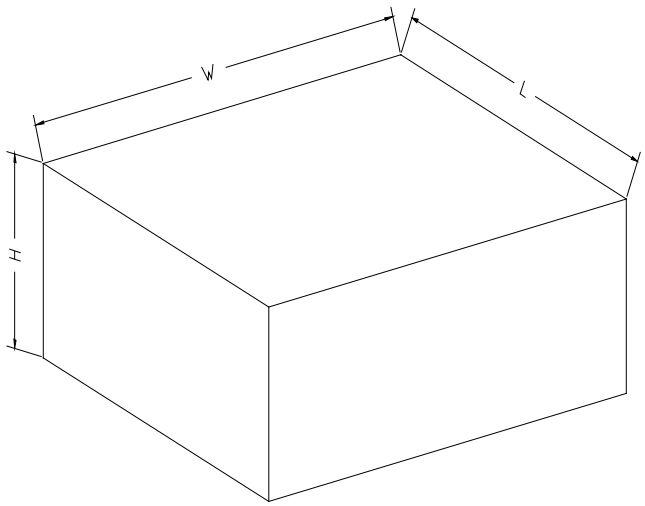
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-3×3-8L	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1
TDFN-2×2-8L	7″	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002