GS3590

Bidirectional 3G-SDI Re-timing Adaptive Cable Equalizer/Cable Driver

Key Features

- Single bidirectional 75Ω cable interface with on-chip termination
- SMPTE ST 424, ST 292-1 and ST 259 compliant input/output
- Multi-standard operation from 1Mb/s to 2.97Gb/s
- Supports re-timing for DVB-ASI at 270Mb/s and MADI at 125Mb/s
- 3D Input Signal Eye Monitor
- PRBS Generator and Checker
- Automatic cable equalization. Typical equalized cable lengths of Belden 1694A cable:
  - 160m at 2.97Gb/s
  - 240m at 1.485Gb/s
  - 400m at 270Mb/s
- **Cable Equalizer Mode Features:**
  - Manual or automatic power-down on loss of signal
  - Programmable carrier detect with squelch threshold adjustment
  - Manual and automatic Cable Equalizer bypass
- **Cable Driver Mode Features:**
  - Wide swing control
  - Pre-emphasis to compensate for significant insertion loss between device output and BNC
  - Manual or automatic power-down on loss of signal
  - Manual or automatic Mute or Disable on LOS
- **Trace Equalizer Features:**
  - Integrated 100Ω, differential input termination
  - Manual or automatic power-down on loss of signal
  - Adjustable carrier detect threshold
  - DC-coupling from 1.2V to 2.5V CML logic
  - Trace Equalization to compensate for up to 60" FR4 at 2.97Gb/s
  - Automatic input offset compensation
- **Trace Driver Features:**
  - Integrated 100Ω, differential output termination
  - DC-coupling from 1.2V to 2.5V CML logic
  - Trace Driver data output pre-emphasis to compensate for up to 60" FR4 at 2.97Gb/s
  - Manual or automatic Mute or Disable on LOS
- **CDR features:**
  - Manual or automatic rate modes
  - Manual or automatic Re-timer Bypass
  - Wide-range Loop Bandwidth control
  - Re-timing at the following data rates: 125Mb/s, 270Mb/s, 1.485Gb/s, and 2.97Gb/s. This includes the f/1.001 rates.
- **Additional Features:**
  - Single 1.8V power supply for analogue and digital core
  - 2.5V for Cable Driver output supply
  - 1.2V, 1.8V, or 2.5V for Trace Driver output supply
  - GSPI serial control and monitoring interface
  - Four configurable GPIO pins for control or status monitoring
  - Wide operating temperature range: -40°C to +85°C
  - Small 6mm x 4mm 40-pin QFN
  - Pb-free/Halogen-free/RoHS & WEEE compliant package
  - Pin compatible with the GS12090

Applications

SMPTE ST 424, SMPTE ST 292, SMPTE ST 259 interfaces requiring switching between cable equalizing or cable driving functionality. Typical applications: Cameras, Switchers, Distribution Amplifiers and Routers.

Description

The GS3590 is a low-power, configurable multi-rate re-timing Cable Equalizer/Cable Driver supporting rates up to 3G-SDI. It can be configured to equalize or drive signals over 75Ω coaxial cable. It includes DC restoration to compensate for the DC content of SMPTE pathological test patterns. Since the GS3590 is a re-timing device, extremely low output jitter is achievable even at extended cable/trace lengths.

The integrated Eye Monitor provides non-disruptive mission mode analysis of the post-equalized input signal. The 256x128 resolution scan matrix allows accurate signal analysis to speed-up prototyping and enable field analysis.

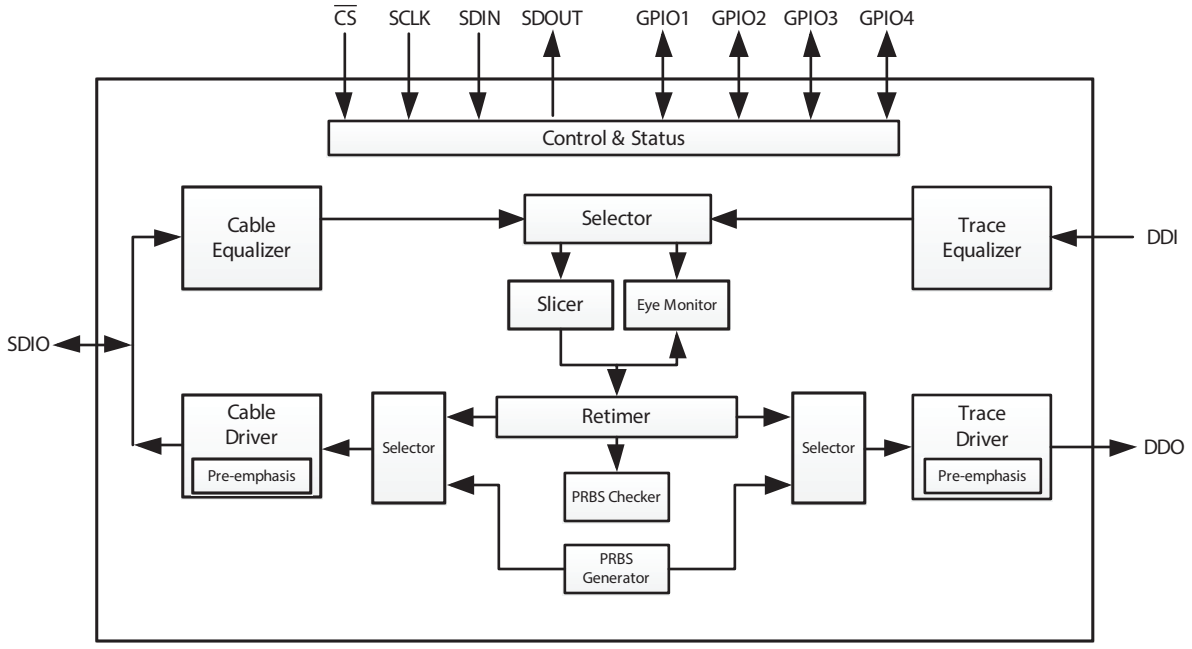
Built-in macros enable customizable cross section analysis and quick horizontal and vertical eye opening measurements.

With high phase consistency between scans and configurable space and time thresholds, algorithms can be deployed in the field to analyse long-term signal quality variation (Bathtub Plot) to reduce costly system installation debug time for intermittent errors.

Each output has highly configurable pre-emphasis and swing controls to compensate for long trace and connector losses.

Additionally, automatic and user selectable output slew rate control is provided for the Cable Equalizer output.

The GS3590 is pin compatible with the GS12090 Bidirectional 12G-SDI Re-timing Adaptive Cable Equalizer/Cable Driver.



GS3590 Functional Block Diagram

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
6	041068	—	July 2018	Updated Section 4.2.3.1, Section 4.10.5.6, Section 4.8.6.2 and Section 5.
5	040329	—	January 2018	Updated Table 2-2,Table 2-3, Section 4.2.1, Section 4.3.2 and Section 5.
4	038524	—	September 2017	Updated values in Table 2-2 and Table 2-3.
3	037845	—	July 2017	Added Section 4.8.3.
2	037327	—	June 2017	Updated Section 4.10.13, and added Section 4.10.12.
1	034374	—	December 2016	Updates as described in the GS3590 Errata (PDS-061458, ECO-034375).
0	033713	—	October 2016	New Document.

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1. Pin Out

1.1 GS3590 Pin Assignment

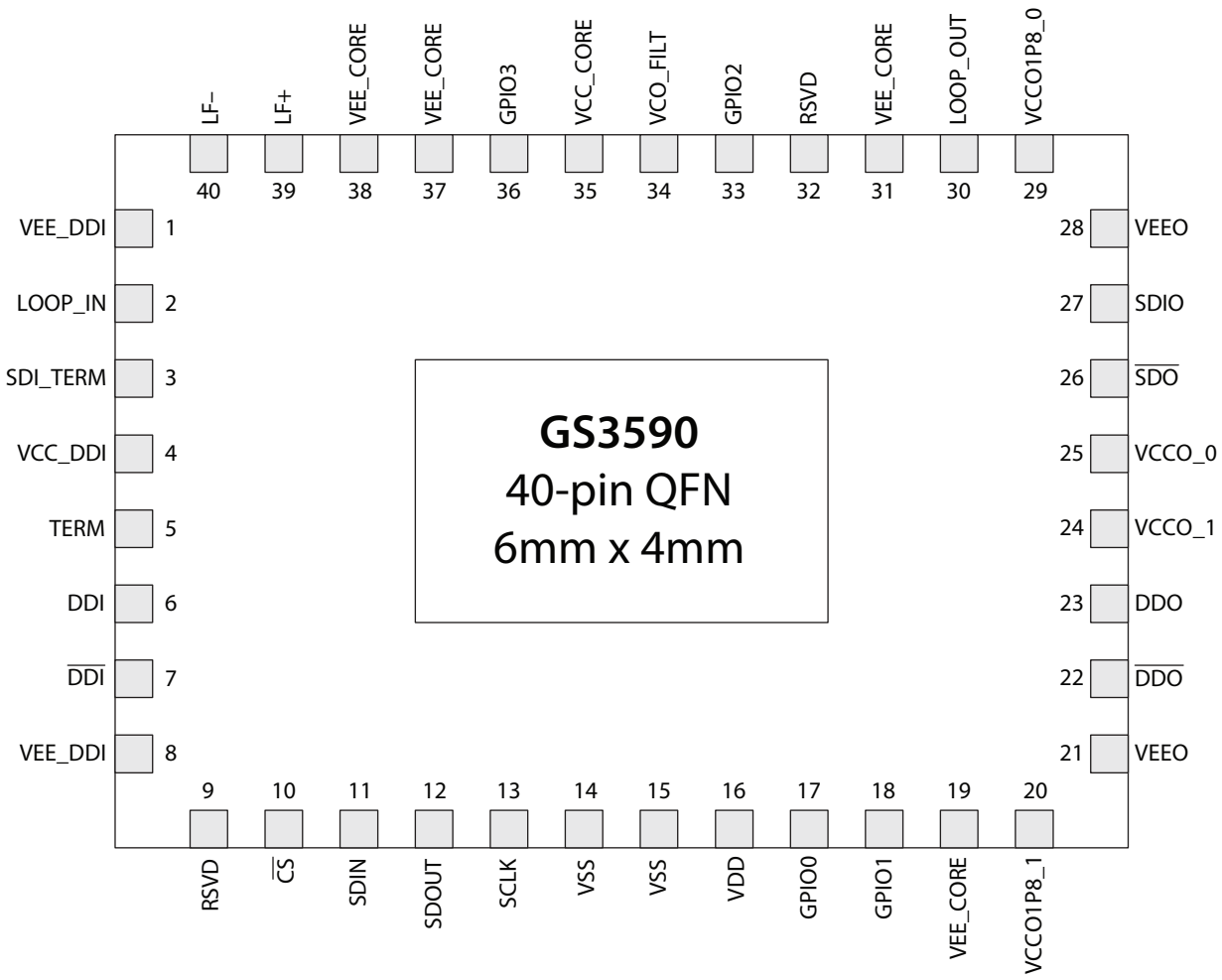


Figure 1-1: GS3590 Pin Assignment

1.2 GS3590 Pin Descriptions

Table 1-1: GS3590 Pin Descriptions

Pin Number	Name	Type	Description
1, 8	VEE_DDI	Power	Most negative power supply connection for the Cable Equalizer and Trace Equalizer. Connect to ground.
2	LOOP_IN	Input	Single-ended CML input with internal 75Ω termination. Connect to LOOP_OUT (pin 30) through a capacitor (see Section 6.1 Typical Application Circuit for recommended values).
3	SDI_TERM	—	Input Common Mode termination. Decouple to ground (see Section 6.1 Typical Application Circuit for recommended values).
4	VCC_DDI	Power	Most positive power supply connection for the Trace and Cable Equalizer. Connect to 1.8V.
5	TERM	—	Input Common Mode termination. Decouple to ground (see Section 6.1 Typical Application Circuit for recommended values).
6, 7	DDI, $\overline{\text{DDI}}$	Input	Serial digital differential input. Differential CML input with internal 100Ω termination.
9, 32	RSVD	—	These pins may be left floating. Please contact your Semtech FAE for additional information on circuit compatibility with the GS3590.
10	$\overline{\text{CS}}$	Digital Input	Chip Select input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-up. Active-low input. Refer to Section 4.10.1 for more details.
11	SDIN	Digital Input	Serial digital data input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-down. Refer to Section 4.10.2 for more details.
12	SDOUT	Digital Output	Serial digital data output for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS output. Refer to Section 4.10.3 for more details.
13	SCLK	Digital Input	Burst-mode clock input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-down. Refer to Section 4.10.4 for more details.
14, 15	VSS	Power	Most negative power supply for digital core logic. Connect to ground.
16	VDD	Power	Most positive power supply connection for digital core logic. Connect to 1.8V.

Table 1-1: GS3590 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
17	GPIO0	Digital Input/Output	Multi-function Control/Status Input/Output 0. Default function: Direction = Output Signal = High indicates LOS (Loss of Signal, inverse of Carrier Detect) Pin is 1.8V CMOS I/O, please refer to GPIO0_CFG for more information on how to configure GPIO0.
18	GPIO1	Digital Input/Output	Multi-function Control/Status Input/Output 1. Default function: Direction = Output Signal = High indicates PLL is locked Pin is 1.8V CMOS I/O, please refer to GPIO1_CFG for more information on how to configure GPIO1.
19, 31, 37, 38	VEE_CORE	Power	Most negative power supply connection for the analogue core. Connect to ground.
20	VCCO1P8_1	Power	Most positive power supply connection for Trace Driver pre-driver. Connect to 1.8V.
21, 28	VEEO	Power	Most negative power supply connection for the output drivers. Connect to ground.
22, 23	$\overline{\text{DDO}}$, DDO	Output	Differential CML output with two internal 50Ω pull-ups. In cable equalizer mode, the data signal or PRBS Generator can be selected for this output.
24	VCCO_1	Power	Most positive power supply connection for the DDO/ $\overline{\text{DDO}}$ output driver. Connect to 1.2V – 2.5V.
25	VCCO_0	Power	Most positive power supply connection for the SDIO/$\overline{\text{SDO}}$ output driver. Connect to 2.5V.
26	$\overline{\text{SDO}}$	Output	Single-ended CML output buffer with internal 75Ω pull-up. Decouple to ground (see Section 6.1 Typical Application Circuit for recommended values).
27	SDIO	Output	Single-ended bidirectional CML buffer with internal 75Ω pull-up. In cable driver mode, the data signal or PRBS Generator can be selected for this output.
29	VCCO1P8_0	Power	Most positive power supply connection for Cable Driver pre-driver. Connect to 1.8V.
30	LOOP_OUT	Output	Single-ended CML output. Connect to LOOP_IN (pin 2) through a capacitor (see Section 6.1 Typical Application Circuit for recommended values).

Table 1-1: GS3590 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
33	GPIO2	Digital Input/Output	Multi-function Control/Status Input/Output 2. Default function: Direction = Input Signal = Set HIGH to put device in sleep Pin is 1.8V CMOS I/O, please refer to GPIO2_CFG for more information on how to configure GPIO2.
34	VCO_FILT	Passive	VCO filter capacitor connection. Decouple to ground. See Section 6.1 Typical Application Circuit for recommended values.
35	VCC_CORE	Power	Most positive power supply connection for the analogue core. Connect to 1.8V.
36	GPIO3	Digital Input/Output	Multi-function Control/Status Input/Output 3. Default function: Direction = Input Signal = Set HIGH to put device in cable driver mode Pin is 1.8V CMOS I/O, please refer to GPIO3_CFG for more information on how to configure GPIO3.
39	LF+	Passive	Loop filter capacitor connection. Connect to pin 40 through a capacitor (see Section 6.1 Typical Application Circuit for recommended values).
40	LF-	Passive	Loop filter capacitor connection. Connect to pin 39 through a capacitor (see Section 6.1 Typical Application Circuit for recommended values).
Tab	—	—	Central paddle can be connected to ground or left unconnected. Its purpose is to provide increased mechanical stability. It is not required for thermal dissipation. It is not recommended to connect the device ground pins to the central paddle.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter		Value
Supply Voltage—Core (V_{CC_DDI}, V_{CC_CORE}, V_{DD})		-0.5V to +2.2V
Supply Voltage—Output Driver	V_{CCO_0}	-0.5V to +2.8V
	V_{CCO_1}	-0.5V to +2.8V
Input ESD Voltage (any pin)		3kV HBM
Storage Temperature Range (T_S)		-50°C to +125°C
Input Voltage Range (SDIO)		-0.3 to (V_{CCO_0} + 0.3)V
Input Voltage Range (GPIO2, GPIO3)		-0.3 to (V_{CC_CORE} + 0.3)V
Input Voltage Range ($\overline{CS}$, SDIN, SCLK, VSS, VDD, GPIO0, GPIO1)		-0.3 to (V_{DD} +0.3)V
Solder Reflow Temperature		260°C

Note: Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation outside of the ranges shown in the AC/DC electrical characteristics tables is not guaranteed.

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Bi-Directional Characteristics (Applicable to Both Modes)							
Supply Voltage	V_{CC_DDI}, V_{CC_CORE}, V_{DD}	—	1.71	1.8	1.89	V	—
DDI Input and DDO Output Termination		Differential	—	100	—	Ω	—
SDIO Bi-directional Termination		Between SDIO and GND	—	75	—	Ω	—
$\overline{SDO}$ Output Termination		Between $\overline{SDO}$ and GND	—	75	—	Ω	—
Supply Current—Analogue Core	I_{CC_CORE}	CDR Unlocked During Rate Search	—	182	—	mA	—
		PRBS Generator Enabled	—	119	—	mA	2, 3
		PRBS Checker Enabled	—	60	—	mA	2
		Eye Monitor Enabled	—	54	—	mA	2
Supply Current—Digital Logic	I_{DD}	—	—	16	20	mA	—
Input Voltage—Digital Pins ($\overline{CS}$, SDIN, SCLK, GPIO[0:1])	V_{IH}	—	0.65* VDD	—	VDD	V	—
	V_{IL}	—	0	—	0.35* VDD	V	—
Input Voltage—Digital Pins (GPIO[2:3])	V_{IH}	—	0.65* VCC_CORE	—	VCC_CORE	V	—
	V_{IL}	—	0	—	0.35* VCC_CORE	V	—
Output Voltage—Digital Pins (SDOUT, GPIO[0:1])	V_{OH}	I_{OH} = -5mA	VDD - 0.45	—	—	V	—
	V_{OL}	I_{OL} = +5mA	—	—	0.45	V	—
Output Voltage—Digital Pins (GPIO[2:3])	V_{OH}	I_{OH} = -5mA	VCC_CORE - 0.45	—	—	V	—
	V_{OL}	I_{OL} = +5mA	—	—	0.45	V	—
Cable Equalizer Mode Characteristics							
Supply Voltage—Trace Driver	V_{CCO_1}		1.14	1.2	1.26	V	—
			1.71	1.8	1.89	V	—
			2.38	2.5	2.63	V	—

Table 2-2: DC Electrical Characteristics (Continued)

T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Power	P_D	V_{CCO_1} = 1.2V, Output Swing = 400mV$_{ppd}$, DDO/$\overline{DDO}$ enabled	—	430	—	mW	1
		V_{CCO_1} = 1.8V, Output Swing = 400mV$_{ppd}$, DDO/$\overline{DDO}$ enabled	—	440	—	mW	1
		V_{CCO_1} = 1.8V, Output Swing = 800mV$_{ppd}$, DDO/$\overline{DDO}$ enabled	—	455	—	mW	1
		V_{CCO_1} = 2.5V, Output Swing = 400mV$_{ppd}$, DDO/$\overline{DDO}$ enabled	—	445	—	mW	1
		V_{CCO_1} = 2.5V, Output Swing = 800mV$_{ppd}$, DDO/$\overline{DDO}$ enabled	—	470	—	mW	1
Supply Current—Trace Driver	I_{CCO_1}	V_{CCO_1} = 1.2V, Output Swing = 400mV$_{ppd}$	—	10	17	mA	1
		V_{CCO_1} = 1.8V, Output Swing = 400mV$_{ppd}$	—	10	17	mA	1
		V_{CCO_1} = 1.8V, Output Swing = 800mV$_{ppd}$	—	20	30	mA	1
		V_{CCO_1} = 2.5V, Output Swing = 400mV$_{ppd}$	—	10	17	mA	1
		V_{CCO_1} = 2.5V, Output Swing = 800mV$_{ppd}$	—	20	30	mA	1
Supply Current — Trace Driver Pre Driver	$I_{CCO_1P8_1}$	Output Swing = 800mV$_{pp}$	—	25	32	mA	—
Supply Current — V_{CCO_0}	I_{CCO_0}	V_{CCO_0} = 2.5V, Output Swing = 800mV$_{ppd}$	—	13	18	mA	—
Supply Current— Cable Equalizer	I_{CC_SDI}	—	—	55	75	mA	—
Supply Current— Analogue Core	I_{CC_CORE}	CDR Locked to Rate	—	125	161	mA	—
DDO Output Common Mode Voltage	V_{CMOUT}	—	—	V_{CCO_1} - $\Delta V_{DDO}/2$	—	V	—

Table 2-2: DC Electrical Characteristics (Continued)

T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Cable Driver Mode Characteristics							
Supply Voltage — Cable Driver	V_{CCO_0}	—	2.38	2.5	2.63	V	—
Power	P_D	V_{CCO_0} = 2.5V, Output Swing = 800mV$_{pp}$, DDO/$\overline{DDO}$ disabled	—	375	—	mW	1
		V_{CCO_0} = 2.5V, Output Swing = 800mV$_{pp}$ with max pre-emphasis, DDO/$\overline{DDO}$ disabled	—	390	—	mW	—
Supply Current— Cable Driver	I_{CCO_0}	V_{CCO_0} = 2.5V, Output Swing = 800mV$_{pp}$	—	25	36	mA	1
		V_{CCO_0} = 2.5V, Output Swing = 800mV$_{pp}$, with max pre-emphasis	—	30	38	mA	—
Supply Current — Cable Driver Pre Driver	I_{CCO1P8_0}	Output Swing = 800mV$_{pp}$	—	20	30	mA	—
Supply Current— Analogue Core	I_{CC_CORE}	CDR Locked to Rate	—	120	164	mA	—
Supply Current — Trace Equalizer	I_{CC_DDI}	—	—	20	32	mA	—
DDI Input Common Mode Voltage	V_{CMIN}	—	0.94	—	2.525	V	4
SDO Output Common Mode Voltage	V_{CMOUT}	Single Ended	—	V_{CCO_0} - $V_{SDO}/2$	—		—
Sleep Mode							
Sleep		Cable Equalizer mode	—	80	—	mW	—
Sleep		Cable Driver mode	—	45	—	mW	—

Notes:

1. Pre-emphasis is disabled.
2. Current listed is an increase to I_{CC_CORE} when stated condition is true.
3. Selected clock source = VCO free running.
4. 0.94V is when the trace equalizer is DC coupled to upstream driver running from 1.2V supply, and 2.525V is when trace equalizer is DC coupled to upstream driver running from 2.5V supply.

2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

V_{CC_DDI}, V_{CC_CORE}, V_{DD} = +1.8V ±5% and V_{CCO_0}, V_{CCO_1} = +2.5V ±5%, T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Bi-Directional Characteristics (Applicable to Both Modes)							
Serial Input Data Rate	DR_{DDI}, DR_{SDIO}	—	0.001	—	2.97	Gb/s	12
Return Loss		5MHz to 1.485GHz	—	—	-17	dB	1
		1.485GHz to 2.97GHz	—	—	-12	dB	1
PLL Loop Bandwidth (for 0.2UI jitter and 50% edge density)	$BW_{LOOP(125Mb/s)}$	Setting 0.0625x	—	5	—	kHz	5
		Setting 0.125x	—	10	—	kHz	5
		Setting 0.25x	—	19	—	kHz	5
		Setting 0.5x (Default)	—	38	—	kHz	5
		Setting 1.0x	—	75	—	kHz	5
	$BW_{LOOP(270Mb/s)}$	Setting 0.0625x	—	10	—	kHz	5
		Setting 0.125x	—	20	—	kHz	5
		Setting 0.25x	—	40	—	kHz	5
		Setting 0.5x	—	80	—	kHz	5
		Setting 1.0x (Default)	—	158	—	kHz	5
	$BW_{LOOP(1.485Gb/s)}$	Setting 0.0625x	—	55	—	kHz	5
		Setting 0.125x	—	110	—	kHz	5
		Setting 0.25x	—	220	—	kHz	5
		Setting 0.5x (Default)	—	438	—	kHz	5
		Setting 1.0x	—	875	—	kHz	5
	$BW_{LOOP(2.97Gb/s)}$	Setting 0.0625x	—	110	—	kHz	5
		Setting 0.125x	—	220	—	kHz	5
		Setting 0.25x	—	440	—	kHz	5
		Setting 0.5x (Default)	—	0.88	—	MHz	5
		Setting 1.0x	—	1.75	—	MHz	5
Cable Equalizer Mode Characteristics							
BNC Input Voltage Swing	V_{SDIO}	—	720	800	880	mV_{pp}	3
Differential Output Voltage Swing	ΔV_{DDO}	200mV	150	200	250	mV_{ppd}	7
		800mV	600	800	1000	mV_{ppd}	8
DDO, $\overline{DDO}$, Rise/Fall Time	$t_{riseDDO}$, $t_{fallDDO}$	All rates	—	—	40	ps	11
DDO Mismatch in Rise/Fall Time		—	—	—	8	ps	11
DDO Duty Cycle Distortion DDO, $\overline{DDO}$		—	—	—	10	ps	—
PLL Lock Time — Asynchronous	t_{ALOCK}	—	—	75	—	ms	6

Table 2-3: AC Electrical Characteristics (Continued)

V_{CC_DDI}, V_{CC_CORE}, V_{DD} = +1.8V ±5% and V_{CCO_0}, V_{CCO_1} = +2.5V ±5%, T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
PLL Lock Time — Synchronous	t_{SLOCK}	SD	—	—	10	µs	6
		HD/3G	—	—	2	µs	6
Serial Data Output Jitter (DDO)	$t_{OJ(125Mb/s)}$	Belden 1694A: 400m	—	0.02	0.1	UI	2
	$t_{OJ(270Mb/s)}$	Belden 1694A: 400m	—	0.02	0.1	UI	2
	$t_{OJ(1.485Gb/s)}$	Belden 1694A: 240m	—	0.02	0.1	UI	2
	$t_{OJ(2.97Gb/s)}$	Belden 1694A: 160m	—	0.04	0.1	UI	2
Cable Driver Mode Characteristics							
Differential Input Voltage Swing	ΔV_{DDI}	—	200	—	800	mV_{ppd}	13
BNC Output Voltage Swing	V_{SDIO}, $V_{\overline{SDO}}$	Single Ended	720	800	880	mV_{pp}	4
Loss Compensation (Input Trace Equalization)		3G	—	60	—	Inches	9
		HD	—	60	—	Inches	9
		SD	—	60	—	Inches	9
		MADI	—	60	—	Inches	9
Intrinsic Input Jitter Tolerance	IIJT	MADI/SD/HD/3G	0.8	0.95	—	UI	—
PLL Lock Time— Asynchronous	t_{ALOCK}	All rates enabled, except MADI.	—	—	16.7	ms	6
		All rates enabled.	—	—	32	ms	6
PLL Lock Time—Synchronous	t_{SLOCK}	SD	—	—	10	µs	6
		HD/3G	—	—	5	µs	6
SDIO, $\overline{SDO}$ Rise/Fall Time	$t_{riseSDIO}$, $t_{fallSDIO}$	SD/MADI	400	—	1000	ps	—
		HD/3G	—	—	70	ps	—
		Bypass	—	—	40	ps	—
SDIO Mismatch in Rise/Fall Time		SD/MADI	—	—	100	ps	—
		HD/3G	—	—	20	ps	—
SDIO Eye Cross Shift (SDIO, $\overline{SDO}$)		SD/MADI	—	—	5	%	—
		HD/3G	—	—	8	%	—
SDIO Overshoot		—	—	—	10	%	—

Table 2-3: AC Electrical Characteristics (Continued)

V_{CC_DDI}, V_{CC_CORE}, V_{DD} = +1.8V ±5% and V_{CCO_0}, V_{CCO_1} = +2.5V ±5%, T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Data Output Jitter (SDIO)	$t_{OJ(125Mb/s)}$	BW = default, Pattern = PRBS	—	0.015	0.08	UI	2, 10
	$t_{OJ(270Mb/s)}$		—	0.035	0.08	UI	2, 10
	$t_{OJ(1.485Gb/s)}$		—	0.025	0.08	UI	2, 10
	$t_{OJ(2.97Gb/s)}$		—	0.04	0.08	UI	2, 10
	$t_{OJ(Bypass)}$		—	0.1	0.2	UI	2, 10

Notes:

1. Values achieved with Semtech evaluation board and connector.
2. Measured using a clean input source.
3. Default value for CFG_EQ_INPUT_LAUNCH_SWING_COMP parameter in control register 0x18. The default parameter value is 80_d (50_h).
4. Default Cable Driver swing Setting.
5. Please see for the full range of loop bandwidth settings.
6. Please see Section 4.4.3.1 for the further definition on Synchronous and Asynchronous Lock Time.
7. Output driver setting of 8.
8. Output driver setting of 36.
9. Trace insertion loss was measured with FR4 material using 7 mil strip-line traces using a PRBS23 signal.
10. Measured under minimal trace loss conditions.
11. Rise/fall time was measured between 80% and 20%.
12. When in Cable Equalizer Mode, the rise/fall time of signals at the source should not be more than 62ns.
13. Stated minimum and maximum voltages represent voltage levels at input pins.

3. Input/Output Circuits

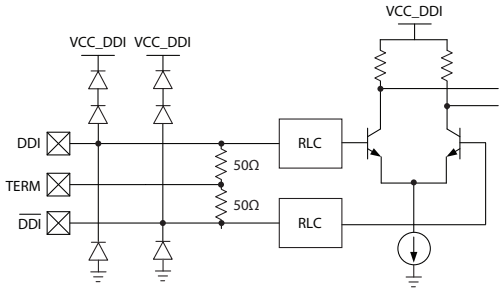


Figure 3-1: DDI, $\overline{\text{DDI}}$

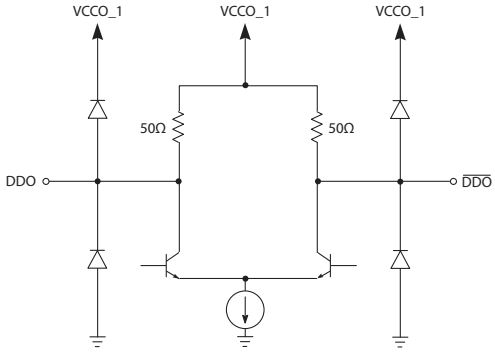


Figure 3-2: DDO/$\overline{\text{DDO}}$

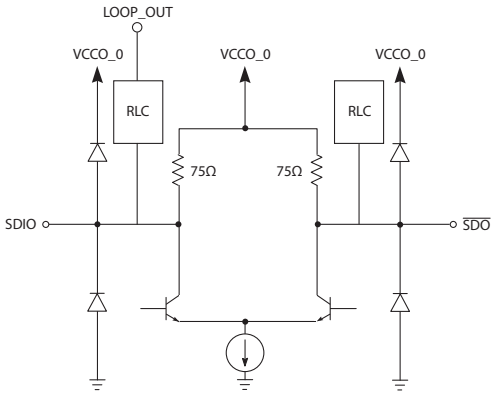


Figure 3-3: SDIO, $\overline{\text{SDO}}$

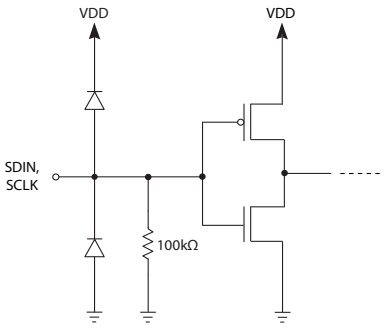


Figure 3-4: SDIN, SCLK

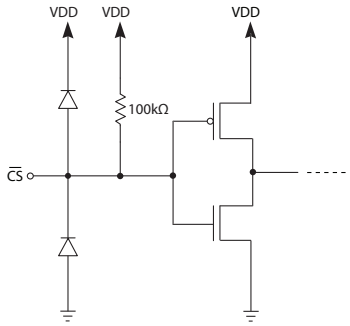


Figure 3-5: Chip Select ($\overline{CS}$)

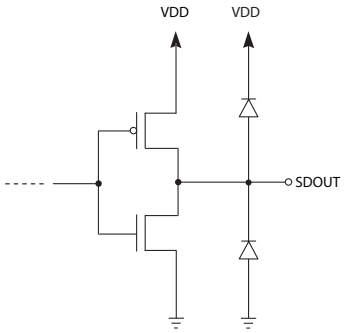


Figure 3-6: SDOUT

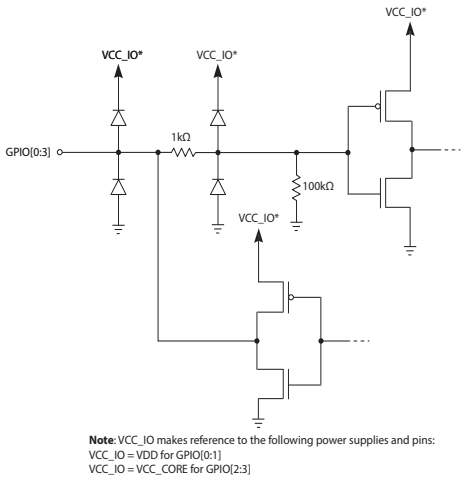


Figure 3-7: GPIO[0:3]

4. Detailed Description

4.1 Device Description

The GS3590 features a 75Ω internally-terminated bidirectional SDIO port, which can be set as SMPTE-compliant Cable Driver, or Cable Equalizer. In addition to the SDIO port, there is a 100Ω differential Trace Driver to transmit the incoming SDI signal to the system and a 100Ω differential Trace Equalizer to receive the outgoing signal from the system. The bidirectional mode can be controlled through the host interface, or the *GPIO* pin. The Cable Driver has amplitude and pre-emphasis control to compensate for significant insertion loss between device output and BNC. The Trace Driver also has amplitude and pre-emphasis control which can compensate for 15dB of insertion loss at 1.485GHz. The pre-emphasis control is two-dimensional in both the Cable Driver and Trace Driver, where both pre-emphasis pulse amplitude and width adjustments can be made to help optimize for interconnect mismatches such as vias and connectors. The Trace Equalizer has boost control, which can compensate for 17dB of insertion loss at 1.485GHz.

4.1.1 Bidirectional Mode Control

The bidirectional mode of the GS3590 can be controlled through the GPIO or the host interface.

By default the device is in pin control mode and *GPIO3* is the control input pin. To put the device in Cable Equalizer Mode drive this pin LOW. To put the device in Cable Driver Mode drive this pin HIGH.

In addition to GPIO control, the host can set the direction mode through the host interface using the **CTRL_DIRECTION_SEL_MODE** and **CTRL_DIRECTION_SEL** parameters in register 0x14. To use the host interface to control the direction mode, first choose host interface select mode by writing 1_b to **CTRL_DIRECTION_SEL_MODE** (default = 0_b pin mode). Once the device is in host interface select mode, the host can put the device in cable equalizer mode by writing 0_b to the **CTRL_DIRECTION_SEL** control parameter (default = 1_b cable driver mode).

4.1.2 Sleep Mode

To enable low-power operation, the GS3590 has Manual and Automatic Sleep Mode control.

The default mode is Automatic Sleep Mode on LOS (Loss Of Signal). The device can also be manually put into Sleep Mode. When the device is in Sleep Mode, all the core blocks are powered-down, except the host interface and carrier detect circuits. The SDIO Cable Driver output buffer is always disabled (powered-down) in sleep mode, while the DDO Trace Driver can be disabled or muted.

The **CTRL_AUTO_SLEEP** and **CTRL_MANUAL_SLEEP** parameters in register 0x3, control the sleep mode of the device. The default value of the **CTRL_AUTO_SLEEP** parameter is 1_b (Auto Sleep). While in Auto Sleep Mode, the **CTRL_MANUAL_SLEEP** parameter has no effect. To enable host control of the sleep mode, set the **CTRL_AUTO_SLEEP** parameter to 0_b for Manual Sleep Control. To prevent the device from entering sleep, set the **CTRL_MANUAL_SLEEP** parameter to 0_b (not sleep). To manually configure the device to sleep, set the **CTRL_MANUAL_SLEEP** parameter to 1_b (sleep).

The device can also be manually made to sleep through the *GPIO* pins. The default *GPIO* pin to control sleep is *GPIO2* (pin 33). Drive this pin HIGH to make the device sleep.

Section 4.7 describes the PRBS Generator function. If the device's PRBS Generator is intended to be used without a valid input signal, the device should be manually set to not sleep as described above. Without a valid input signal, an LOS status will be generated and the device will enter sleep mode and the PRBS block will be disabled. For a description of LOS thresholds and settings, see Section 4.2.3 and Section 4.3.2.

4.2 Cable Equalizer

When the GS3590 is operating in Cable Equalizer Mode, it can automatically adjust its gain to equalize and restore SMPTE-compliant signals received over different lengths of coaxial cable having loss characteristics similar to Belden 8281 or 1694A. With the default settings, the device will automatically equalize MADI at 125Mb/s and most common SMPTE compliant signals between SD at 270Mb/s and 3G-SDI at 2.97Gb/s and bypass signals below 125Mb/s.

The GS3590 features programmable Launch Swing Compensation, Squelch Threshold Adjust, and Bypass, all of which can be set through the device's host interface.

The equalized or bypassed signal is then routed to the serial digital re-timer (CDR) block.

Note: Section 4.2 to Section 4.2.3.2 are only applicable to the Cable Equalizer input (SDIO).

4.2.1 Cable Equalizer Bypass

With the default settings, the device will automatically bypass signals below 125Mb/s. During cable equalizer bypass mode, the device supports low data rate and slow edge signals such as SMPTE310 and AES3id. The rise/fall times must not exceed 62ns. While in cable equalizer bypass mode, signals will not be re-timed by the CDR block.

To force the device to bypass the cable equalizer, DC restoration stage, and CDR, the following two methods can be used:

Host Interface Control:
Set the following parameters in register 17_h

- **CTRL_CEQ_AUTO_BYPASS** = 0
- **CTRL_CEQ_MANUAL_BYPASS** = 1

GPIO Control:

1. Configure a GPIO as an input by writing 0_h to the **CFG_GPIO<n>_OUTPUT_ENA**.
2. Configure the GPIO function as "cable equalizer bypass enable," by writing 84_h to **CFG_GPIO<n>_FUNCTION**.
3. Drive the selected GPIO pin HIGH.

Note: The <n> in the control parameter names refers to the GPIO pin number.

4.2.2 Upstream Launch Swing Compensation

The GS3590 Cable Equalizer has an automatic gain control circuit, that is optimized on the assumption that the Cable Driver in the upstream device is SMPTE-compliant and has a launch swing of $800mV_{pp}$ ±10%. When the source amplitude is known to be non-SMPTE compliant, a compensation adjustment can be made in the GS3590. The GS3590 can adjust for launch swings in the range of 250mV to 1V in approximately $50mV_{ppd}$ increments. Upstream launch swing compensation can be adjusted through the **CFG_EQ_INPUT_LAUNCH_SWING_COMP** parameter in control register 0x18. The default parameter value is 80_d (50_h), which corresponds to a nominal launch swing of $800mV_{ppd}$.

4.2.3 Carrier Detect, Squelch Control, and Loss of Signal

The GS3590 Cable Equalizer has highly-configurable carrier detection and squelching capability. The carrier detection can be made more robust against spurious signals and noise at the inputs and the squelch control can be configured and enabled to reduce false outputs to low level signals such as crosstalk.

The GS3590 reports two separate carrier detect parameters—**STAT_PRI_CD** and **STAT_SEC_CD**. They are described in Section 4.2.3.1 and Section 4.2.3.2 respectively.

Note: The parameters referred to within Section 4.2.3 to Section 4.2.3.2 are linked to their respective registers in Table 4-1.

4.2.3.1 Primary Carrier Detection (STAT_PRI_CD) Configuration

Primary carrier detection (**STAT_PRI_CD**) can be configured for higher stability by filtering-out longer transients or glitches. This can be achieved by increasing the sampling window over which the signal is sampled and the number of samples required to assert or de-assert it.

There are three configuration parameters that control assertion or de-assertion of **STAT_PRI_CD**:

- **CFG_CD_FILTER_SAMPLE_WIN**
- **CFG_FILTER_DEASSERT_CNT**
- **CFG_CD_FILTER_ASSERT_CNT**

See Figure 4-1 for a visual representation of the **STAT_PRI_CD** configuration parameters.

With the default values in place:

- An assertion (setting HIGH) of **STAT_PRI_CD** will take place after a valid signal is present for ~6.5ms
- A de-assertion (setting LOW) of **STAT_PRI_CD** will take place after loss of a valid signal for ~96µs

If the application requires any adjustment of the sampling window, assertion count, or de-assertion count, please consult the following equations to calculate the associated time to assert or de-assert **STAT_PRI_CD**.

STAT_PRI_CD de-assert time:

- ***(1.6µs) * (CFG_CD_FILTER_SAMPLE_WIN + 1) * CFG_CD_FILTER_DEASSERT_CNT***

STAT_PRI_CD assert time:

- ***(1.6µs) * (CFG_CD_FILTER_SAMPLE_WIN + 1) * CFG_CD_FILTER_ASSERT_CNT***

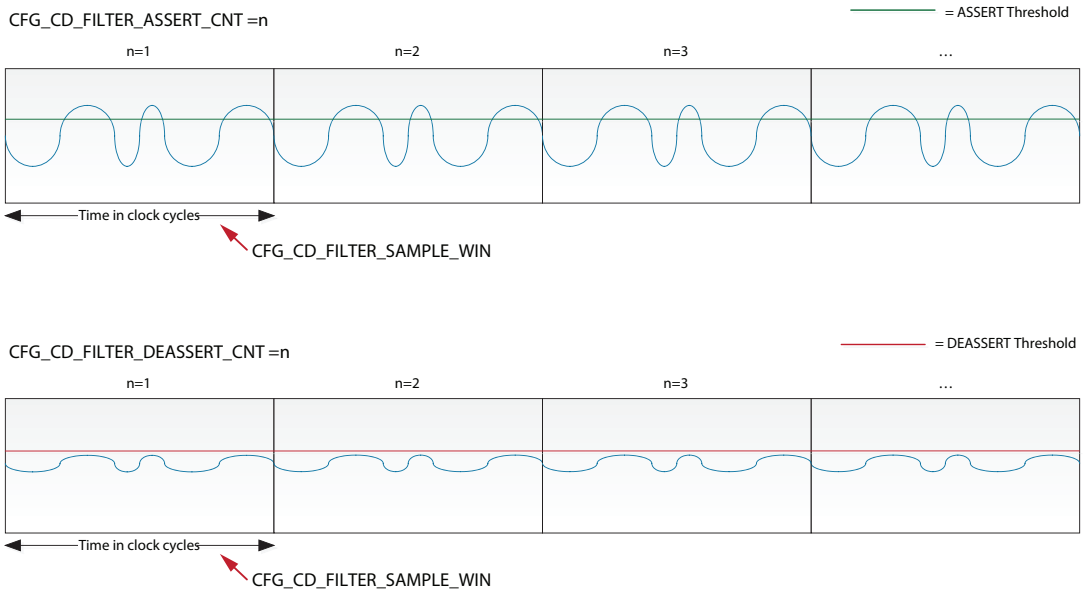


Figure 4-1: STAT_PRI_CD Configuration Parameters

4.2.3.2 Secondary Carrier Detection (STAT_SEC_CD) Configuration

The secondary carrier detection signal acts as an additional carrier detection which can be further filtered through squelch controls. It also serves as the control signal for Mute on LOS (Loss Of Signal) and Disable on LOS. Please refer to Section 4.8.6 to Section 4.8.6.3 for further information on this.

If the application requires the use of squelch settings, start by setting the following:

- **CFG_SEC_CD_INCL_CLI_SQUELCH** = 1

Once this parameter is set, the device will apply squelch based on the settings found within the following parameters:

- **CFG_CLI_SQUELCH_THRESHOLD**

- **CFG_CLI_SQUELCH_HYSTERESIS**

The device will use these parameters to determine squelch status and set that within **STAT_CLI_SQUELCH**. Based off of this, secondary carrier detection can be described as:

- **STAT_SEC_CD** = inverse of (**STAT_CLI_SQUELCH** & **STAT_PRI_CD**).

To help detail how the device determines the state of Squelch, we define the following variables:

- CLI = **STAT_CABLE_LEN_INDICATION**
- THR = **CFG_CLI_SQUELCH_THRESHOLD**
- HYS = **CFG_CLI_SQUELCH_HYSTERESIS**
- SQL = **STAT_CLI_SQUELCH**

The following rules define the state of SQL.
Note: If the cable equalizer is in bypass (**STAT_CEQ_BYPASS** = 1), the device will set SQL to 0.

- If CLI > (THR + HYS), the device will set SQL to 1, otherwise:
- If CLI < (THR - HYS), the device will set SQL to 0, otherwise:
- If CLI ≥ (THR - HYS) and CLI ≤ (THR + HYS), SQL remains unchanged.
- If SQL = 1, the device will not indicate lock and the trace driver state will be defined by output state control parameters settings, see Section 4.8.6 for more details.

Table 4-1: Cable Equalizer Status and Configuration Parameters

Register Address$_h$ and Name	Parameter Name	Parameter Description
15, CARR_ DET_CFG	CFG_SEC_CD_INCL_CLI_SQUELCH	Enables or disables squelch control.
16, SQUELCH_ PARAMETERS	CFG_CLI_SQUELCH_THRESHOLD	Used to tune the squelch threshold based on the tolerance requirements of the application.
	CFG_CLI_SQUELCH_HYSTERESIS	Used to tune the squelch hysteresis based on the tolerance requirements of the application.
20, CD_FILTER_ DELAYS_0	CFG_CD_FILTER_SAMPLE_WIN	Primary carrier detect sampling window size.
21, CD_FILTER_ DELAYS_1	CFG_CD_FILTER_DEASSERT_CNT	Primary carrier detect de-assertion count.
22, CD_FILTER_ DELAYS_2	CFG_CD_FILTER_ASSERT_CNT	Primary carrier detect assertion count.
84, STICKY_ COUNTS_0	STAT_CNT_PRI_CD_CHANGES	A counter showing the number of times the primary Carrier Detect signal changed.
	STAT_CNT_SEC_CD_CHANGES	A counter showing the number of times the secondary Carrier Detect signal changed.
86, CURRENT_ STATUS_0	STAT_CLI_SQUELCH	Cable equalizer Squelch status.

Table 4-1: Cable Equalizer Status and Configuration Parameters (Continued)

Register Address$_h$ and Name	Parameter Name	Parameter Description
87, CURRENT_ STATUS_1	STAT_PRI_CD	Primary filtered carrier detect of the analogue carrier detect signal.
	STAT_SEC_CD	Secondary filtered carrier detect of the analogue carrier detect signal.
88, EQ_GAIN_IND	STAT_CABLE_LEN_INDICATION	SDIO cable length indication when in cable equalizer mode.

4.3 Trace Equalizer

The GS3590 features a differential input buffer with 100Ω differential input termination, which includes a Trace Equalizer that can be configured to compensate for up to 60" of 7mil strip-line in FR4 at 2.97Gb/s.

The differential input signal can be either DC-coupled or AC-coupled, and is capable of operation with any binary coded signal between 1Mb/s and 2.97Gb/s.

The input circuit is compatible with industry standard CML differential transmitters when DC-coupled using industry standard 100Ω differential termination circuitry.

The Trace Equalizer includes an automatic input offset compensation circuit. This reduces offset-induced data jitter in the link due to asymmetric performance of DC-coupled upstream differential drivers. The input offset compensation circuit also improves the input sensitivity of the Trace Equalizer.

Note: When working with the Trace Equalizer, note the following:

- The parameters referred to within Section 4.3 to Section 4.3.2 are linked to their respective registers in Table 4-2. For a complete list of registers and functions, see Section 5.
- Section 4.3 to Section 4.3.2 are only applicable to the Trace Equalizer input (DDI).

4.3.1 Input Trace Equalizer

The Trace Equalizer can compensate for up to 17dB of insertion loss at 1.485GHz in 8 increments, which can be adjusted through the **CFG_TREQ0_BOOST** parameter in control register 0x1E. The default value of **CFG_TREQ0_BOOST** is (0_h), which corresponds to the minimum equalization boost level.

Please refer to Figure 4-2 for recommended boost setting.

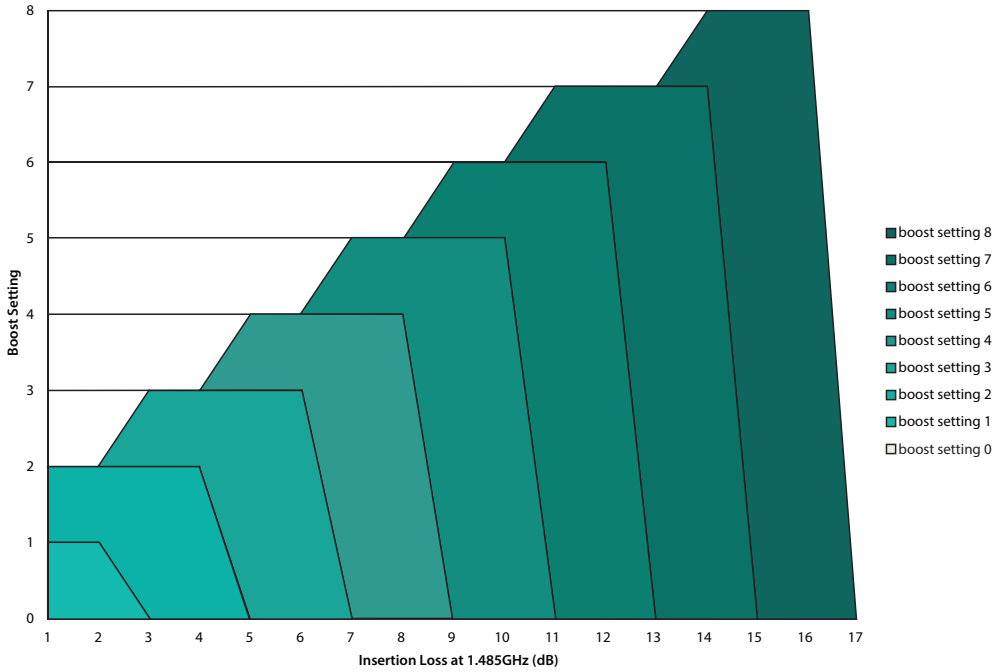


Figure 4-2: GS3590 Trace EQ Boost Setting Recommendation

By default at power up or after system reset, the trace equalizer is configured to compensate for up to 3" of 7mil strip-line in FR4 material at high-frequencies.

Note: If using input trace lengths longer than 5", use an upstream launch swing of ~ 800mV$_{ppd}$.

4.3.2 Carrier Detect, and Loss of Signal

The trace equalizer has a highly configurable Carrier Detection mechanism that allows the system designer to optimize the sensitivity and hysteresis of the Carrier Detection mechanism to meet specific system requirements.

Default settings should satisfy most applications; however, designers can modify the following three parameters to customize the trace equalizer's carrier detection for their application:

- **CFG_TREQ0_CD_BOOST**
- **CFG_TREQ0_CD_ASSERT_THRESH**
- **CFG_TRE0Q_CD_DEASSERT_THRESH**

The trace equalizer Carrier Detect is reported by status parameter **STAT_PRI_CD** in register 0x87.

The first CD control parameter is **CFG_TREQ0_CD_BOOST** in register 0x1E. This parameter determines the method and therefore the level of equalization to be used on the input signal routed to the Carrier Detection sub-block. The default value is 0_b, which maximizes the level of equalization. Alternatively, the designer can choose to have this signal equalized at the same level as the main signal routed to the CDR by setting **CFG_TREQ0_CD_BOOST** to 1_b. The setting of this parameter has no impact on the main signal routed to the CDR.

The last two CD control parameters can be found in register 0x1F. Parameters **CFG_TREQ0_CD_ASSERT_THRESH** and **CFG_TRE0Q_CD_DEASSERT_THRESH** set the Carrier Detect assert and de-assert thresholds to the input signal, which also defines the hysteresis of CD signal.

The default values of **CFG_TREQ0_CD_ASSERT_THRESH** and **CFG_TREQ0_CD_DEASSERT_THRESH** are 4_d and 3_d respectively. With the default settings, the minimum launch swing needed to assert the carrier detect is 200mV and it will be de-asserted when the signal level falls below 150mV.

The **STAT_PRI_CD** (Carrier Detect) parameter will be set to 0_b and the LOS will be set to 1_b whenever a new signal at the input does not exceed the assert threshold, or an existing signal falls below the de-assert threshold. The result is that the device will not indicate lock, and the outputs will mute (assuming Mute on LOS is left to its default value in the **CONTROL_OUTPUT_MUTE** register—0x49). See Section 4.8.6 for more details.

Given a differential input trace with 17dB of insertion loss at 1.485GHz and **CFG_TREQ_CD_BOOST** = 0_b, Figure 4-3 illustrates the relationship between launch swing voltage, and minimum threshold setting to assert or de-asset Carrier Detect at all rates up to threshold setting at 2.97Gb/s.

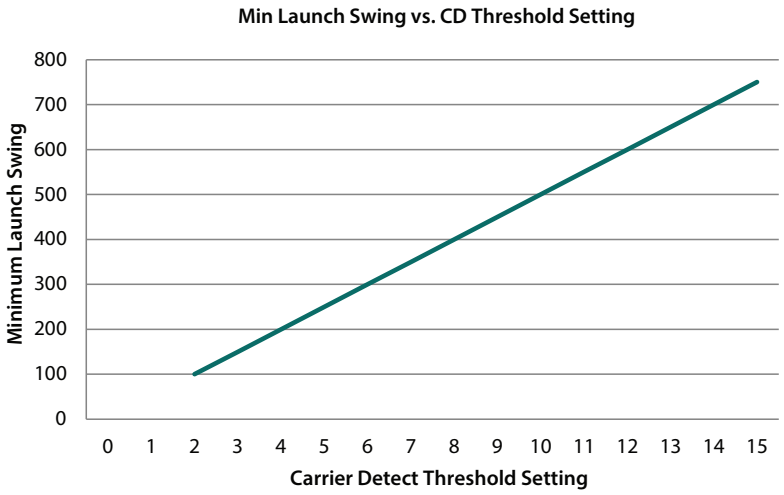


Figure 4-3: Input Voltage Vs. Carrier Detect Threshold Setting

Table 4-2: Trace Equalizer Status and Configuration Parameters

Register Address$_h$ and Name	Parameter Name	Description
84, STICKY_ COUNTS_0	STAT_CNT_PRI_CD_CHANGES	A counter showing the number of times the primary Carrier Detect signal changed.
87, CURRENT_ STATUS_1	STAT_PRI_CD	Primary filtered carrier detect of the analogue carrier detect signal.
1F, TREQ0_CD_ HYSTERESIS	CFG_TREQ0_CD_ASSERT_THRESH	Sets the Carrier Detect assert threshold.
	CFG_TREQ0_CD_DEASSERT_THRESH	Sets the Carrier Detect de-assert threshold.
1E, TREQ0_ INPUT_BOOST	CFG_TREQ0_BOOST	Sets the Trace Equalizer boost level.
	CFG_TREQ0_CD_BOOST	Selects the boost method of the CD signal.

4.4 Serial Digital Re-timer (CDR)

The GS3590 includes an integrated CDR, whose purpose is to lock to a valid incoming signal from the Cable Equalizer stage (when operating in cable equalizer mode) or the Trace Equalizer stage (when operating in cable driver mode) and produce a lower jitter signal at the Cable Driver or Trace Driver outputs. The CDR has the ability to lock to any of the following data rates: MADI (125Mb/s), SD-SDI (270Mb/s), HD-SDI (1.485Gb/s), and 3G-SDI (2.97Gb/s). This includes the f/1.001 rates.

The default settings of the re-timer block are optimal for most applications. However, the following controls allow the user to customize the behaviour of the re-timer: loop bandwidth control, Automatic and Manual Rate Detection.

Note: The parameters referred to within Section 4.4.1 to Section 4.4.2 are linked to their respective registers in Table 4-4: CDR Control and Status Parameters. For a complete list of registers and functions, please see Section 5.

4.4.1 PLL Loop Bandwidth Control

The ratio of output peak-to-peak jitter to input peak-to-peak jitter of the CDR can be represented by a low-pass jitter transfer function, with a bandwidth equal to the PLL loop bandwidth. Although the default loop bandwidth settings for the GS3590 CDR are ideal for most SDI signals, the GS3590 allows the user to adjust the loop bandwidth for each MADI and SMPTE-compliant rate.

Registers 0x0B through 0x0C contain the following parameters which allow the user to configure rate dependent loop bandwidth: **CFG_PLL_LBW_3G**, **CFG_PLL_LBW_HD**, **CFG_PLL_LBW_SD**, and **CFG_PLL_LBW_MADI**. The loop bandwidth settings are defined in terms of ratios of the nominal loop bandwidth. For each rate, where '1.0x' is the nominal loop bandwidth, the following ratios are available: 0.0625x, 0.125x, 0.25x, 0.5x, and 1.0x. Table 2-3 provides the specific loop bandwidths for each data rate and loop bandwidth setting. Lowering the loop bandwidth will lower the jitter amplitude above the loop bandwidth frequency. Although lower output jitter is desirable, the lower loop bandwidth may reduce the device's IJT to very high jitter that may be present outside the loop bandwidth.

4.4.2 Automatic and Manual Rate Detection

In Cable Equalizer mode, with the default rate detect settings, the CDR will automatically attempt to lock to any of following data rates: MADI (125Mb/s), SD-SDI (270Mb/s), HD-SDI (1.485Gb/s), and 3G-SDI (2.97Gb/s). This includes the f/1.001 rates.

In Cable Driver mode, with the default rate detect settings, the CDR will automatically attempt to lock to any of the following data rates: SD-SDI (270Mb/s), HD-SDI (1.485Gb/s), and 3G-SDI (2.97Gb/s). This includes the f/1.001 rates.

However, the CDR can be configured to only lock to a single rate, by setting the **CFG_AUTO_RATE_DETECT_ENA** and **CFG_MANUAL_RATE** parameters in register 0x06. In addition to **CFG_MANUAL_RATE**, when operating in cable driver mode and with automatic rate detection enabled (**CFG_AUTO_RATE_DETECT_ENA** = 1), specific rates can be excluded from the rate detect list through the **CFG_RATE_ENA_<r>** rate disable mask parameter in 0x06, where r is the rate to be disabled. For details on specific settings, please see Table 5-3: Control Register Descriptions, RATE_ DETECT_ MODE.

Note: The **CFG_RATE_ENA_<r>** parameter is only applicable to the trace equalizer input DDI in cable driver mode.

The **STAT_LOCK** parameter in register 0x86 will indicate that the CDR is locked when its value is 1_b and unlocked when its value is 0_b. The lock status can also be monitored externally on any *GPIO* pin, however it is the default mode for *GPIO1*, pin 18. The **STAT_DETECTED_RATE** parameter in register 0x87 will indicate the data rate at which the CDR is locked to. A value of 0_d in the **STAT_DETECTED_RATE** parameter indicates that the device is not locked, while values between 1_d and 4_d will indicate that the device is locked to one of the four available rates between MADI at 125Mb/s and 3G-SDI at 2.97Gb/s.

If the CDR cannot lock to any of the valid rates in automatic mode or the selected rate in manual mode, the signal can automatically be bypassed to the output. If the CDR does lock to the incoming signal, the re-timed and bypassed (if manual bypass control

enabled) signals are available at the appropriate output. See the Section 4.8 for more details.

Table 4-3: Detected Data Rates

STAT_DETECTED_ RATE [2:0]	Detected Data Rate
0	Unlocked
1	MADI (125Mb/s)
2	SD (270Mb/s)
3	HD (1.485Gb/s)
4	3G (2.97Gb/s)
5	Reserved
6	Reserved
7	Reserved

4.4.3 Lock Time

4.4.3.1 Synchronous and Asynchronous Lock Time

Synchronous lock time is defined as the time it takes the device to re-lock to an existing signal that has been momentarily interrupted or to a new signal of the same data rate as the previous signal which has been quickly switched in.

Asynchronous lock time is defined as the time it takes the device to lock when a signal is first applied to the serial digital inputs, or when the signal rate changes. The asynchronous and synchronous lock times are defined in Table 2-3.

Note: To ensure synchronous lock times are met, the maximum interruption time of the signal is 10µs for an SD-SDI signal. HD, and 3G signals must have a maximum interruption time of 6µs. The new signal, after interruption, must have the same frequency as the original signal but may have an arbitrary phase.

Table 4-4: CDR Control and Status Parameters

Register Address$_h$ and Name	Parameter Name	Description
06, RATE_DETECT_MODE	CFG_AUTO_RATE_DETECT_ENA	Enables or disables the automatic rate detection mode of the CDR.
	CFG_MANUAL_RATE	Select a single rate for CDR rate detection when CFG_AUTO_RATE_DETECT_ENA is 0_b.
	CFG_RATE_ENA_3G	3G auto rate detection enable
	CFG_RATE_ENA_HD	HD auto rate detection enable
	CFG_RATE_ENA_SD	SD auto rate detection enable
	CFG_RATE_ENA_MADI	MADI auto rate detection enable
0B, PLL_LOOP_BANDWIDTH_ 1	CFG_PLL_LBW_3G	Configures the Loop Bandwidth for 3G signals.
	CFG_PLL_LBW_HD	Configures the Loop Bandwidth for HD signals.
0C, PLL_LOOP_BANDWIDTH_ 2	CFG_PLL_LBW_SD	Configures the Loop Bandwidth for SD signals.
	CFG_PLL_LBW_MADI	Configures the Loop Bandwidth for MADI signals.
11, GPIO1_CFG	CFG_GPIO1_FUNCTION	Sets the function of GPIO1.
	CFG_GPIO1_OUTPUT_ ENA	Sets the GPIO pin as either an output or an input.
85, STICKY_COUNTS_1	STAT_CNT_PLL_LOCK_CHANGES	Counter showing the number of times the PLL lock status changed.
	STAT_CNT_RATE_CHANGES	Counter showing the number of times the PLL lock rate changed.
86, CURRENT_STATUS_0	STAT_LOCK	The status of the PLL. Locked, or unlocked.
87, CURRENT_STATUS_1	STAT_DETECTED_RATE	The rate at which the PLL is locked to.

4.5 PRBS Checker

The GS3590 includes an integrated PRBS Checker, which can error check a PRBS7 signal out of the trace or cable equalizer input blocks.

There are two modes of operation for the PRBS checker:

- Timed Mode: Used for precise measurements of up to ~3.34s
    - In Timed Mode, the host sets the measurement time and executes the checker operation. The device ends the PRBS error check measurement when the timer expires, and the host reads back the measurement status and error count
- Continuous Mode: Can be used for longer measurements but with less precision in the time interval
    - In Continuous Mode, the host controls the starts and stops of the PRBS error checking operation then reads back the measurement status and error count

Note: When working with the PRBS Checker, please note the following:

- The parameters referred to in Section 4.5 to Section 4.5.2 are briefly described and linked to their respective registers in Table 4-5
- The PRBS Generator and Checker can be active at the same time. However, the Generator can not be looped-back on itself for error checking

4.5.1 Timed PRBS Check Measurement Procedure

For applications where measurement times are ~3.34s or less, the timed PRBS check mode is the most suitable. Alternatively, to achieve precise timing for lower BER signals, the timed PRBS check measurement can be repeated by the host and the total measurement time and error count is determined by summing the individual measurements.

In timed mode, the host sets the total measurement time by setting the **CFG_PRBS_CHECK_PREDIVIDER** and the **CFG_PRBS_CHECK_MEAS_TIME** parameters to the required values to achieve the total measurement time required by the application.

To perform a timed PRBS measurement, please complete the following steps:

1. Set the appropriate settings within **CFG_PRBS_CHECK_PREDIVIDER** and **CFG_PRBS_CHECK_MEAS_TIME** to achieve the total measurement time required by the application. The TMT (Total Measurement Time) is determined by the following equation:

   TMT = **CFG_PRBS_CHECK_PREDIVIDER** * (**CFG_PRBS_CHECK_MEAS_TIME** *256+1) * (1/40MHz)

   Note: Using the default **CFG_PRBS_CHECK_PREDIVIDER** setting of 0 (pre-divider = 4) and **CFG_PRBS_CHECK_MEAS_TIME** setting of 3 (**MEAS_TIME** = 3), the TMT is ~77µs per measurement.
2. Follow the steps outlined in the flowchart found within Figure 4-4: Timed PRBS Check Flow.

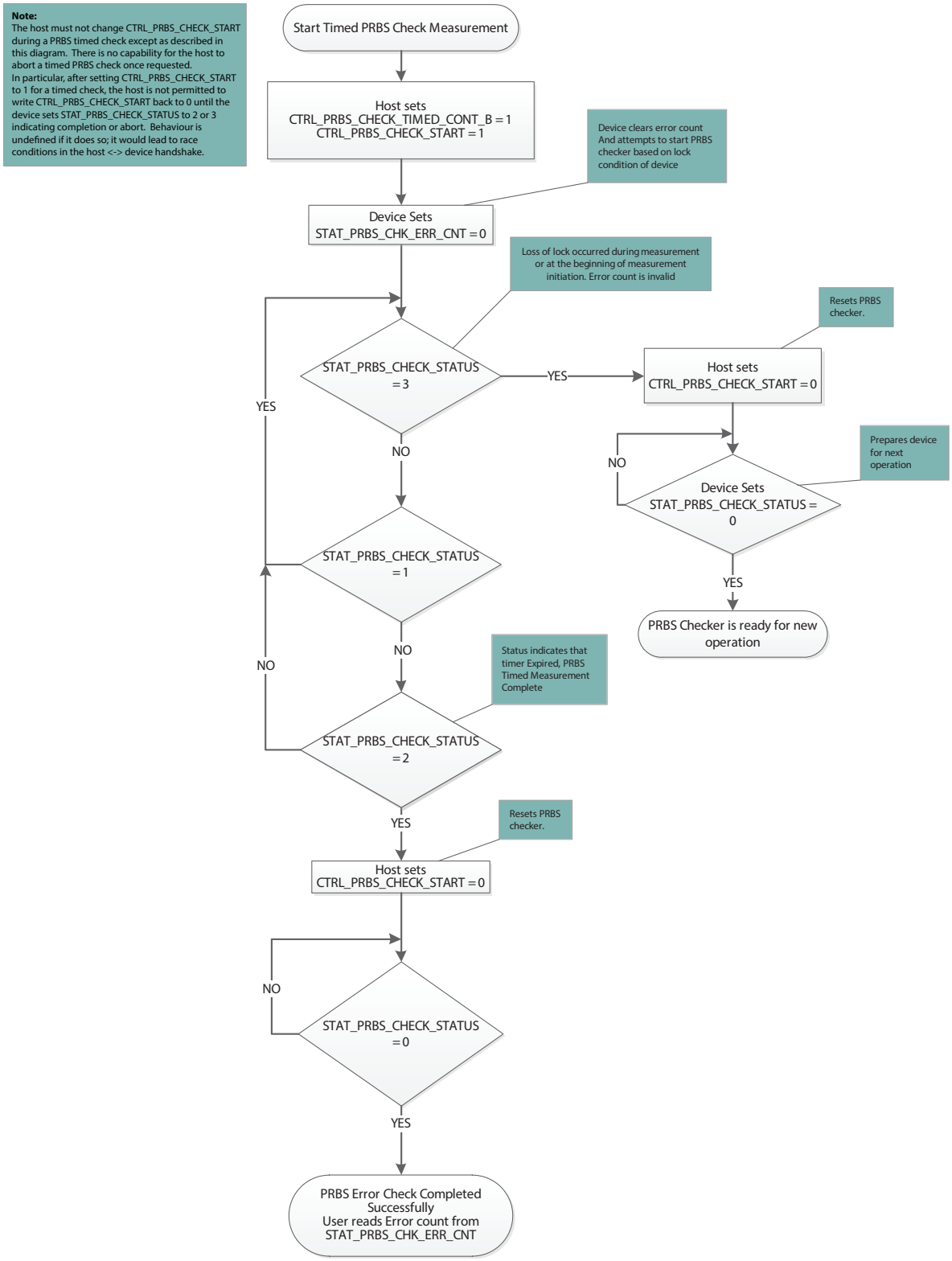


Figure 4-4: Timed PRBS Check Flow

4.5.2 Continuous PRBS Check Measurement Procedure

The maximum measurement time for a timed PRBS error measurement is ~3.35 seconds. For links with very low error rates, this time is insufficient to capture an adequate number of errors. For these situations, the continuous PRBS check measurement is more appropriate.

In continuous PRBS measurement mode, the measurement can run as long as required (assuming the device remains locked) to ensure the BER test level is met.

To perform a continuous PRBS measurement, please follow the steps outlined in the flowchart found within Figure 4-5: Continuous PRBS Flow Chart

Table 4-5: PRBS Checker Parameter Description

Register Address$_h$ and Name	Parameter Name	Parameter Description
50, PRBS_ CHK_CFG	CFG_PRBS_CHECK_PREDIVIDER	Selects pre-divider for PRBS check measurement timer.
	CFG_PRBS_CHECK_MEAS_TIME	Selects PRBS check measurement interval for timed measurements.
51, PRBS_CHK_ CTRL	CTRL_PRBS_CHECK_TIMED_CONT_B	Selects between timed and continuous type PRBS measurement.
	CTRL_PRBS_CHECK_START	Used to start and stop PRBS measurements.
89, PRBS_ CHK_ERR_CNT	STAT_PRBS_CHK_ERR_CNT	PRBS error count storage location.
8A, PRBS_ CHK_STATUS	STAT_PRBS_CHECK_STATUS	Status indication of PRBS checker.
	STAT_PRBS_CHECK_LAST_ABORT	Indication bit for PRBS successful completion or abort.

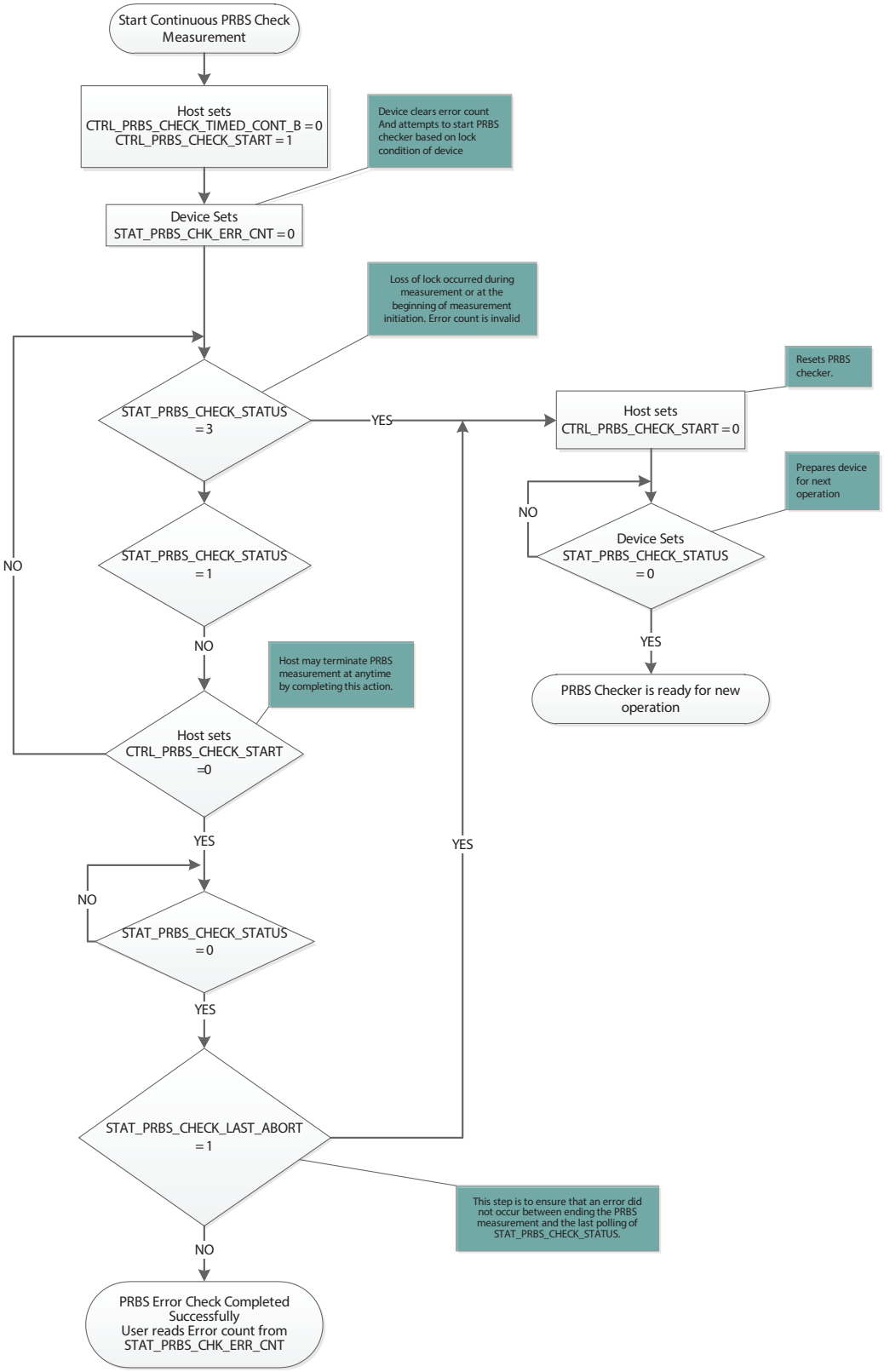


Figure 4-5: Continuous PRBS Flow Chart

4.6 Eye Monitor

The GS3590 includes an integrated Eye Monitor, which can scan the equalized signal from the trace or cable equalizer input blocks. The Eye Monitor is capable of performing a full 128h x 256v matrix-scan or simply a 4 coordinate shape-scan of the equalized signal (See Figure 4-6).

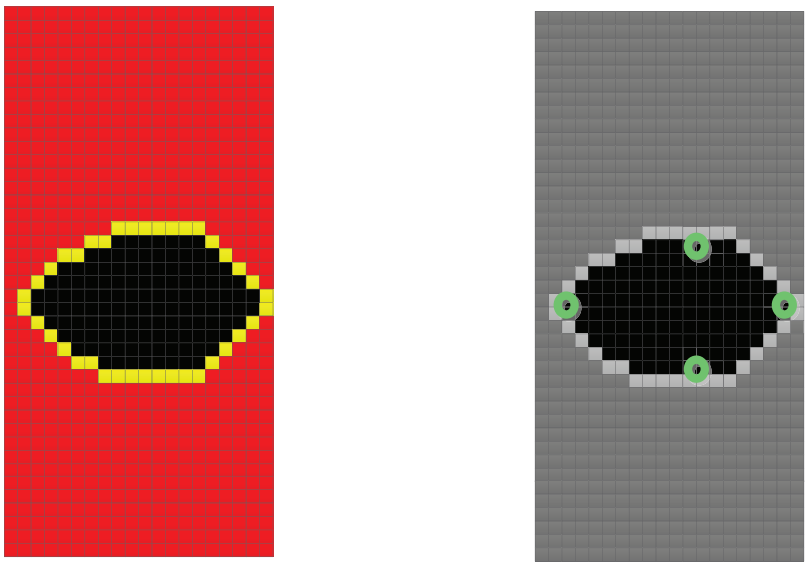


Figure 4-6: Full Matrix Scan (left) and 4-Point Shape Scan (right)

The Eye Monitor is highly-configurable, and the host can configure the offset, resolution, sample time, and error threshold parameters to control the depth and execution time of the scan. The Eye Monitor scans the signal from whichever of the trace or cable equalizer blocks is active for the current direction (see Section 4.1.1 for directional mode configuration). Similar to the PRBS Checker, the Eye Monitor is controlled through a 4-way handshake mechanism. The following sections outline the scan parameters and procedure to configure the eye scan area, error threshold, and run a shape or full scan.

4.6.1 Scan Matrix and Measurement Time

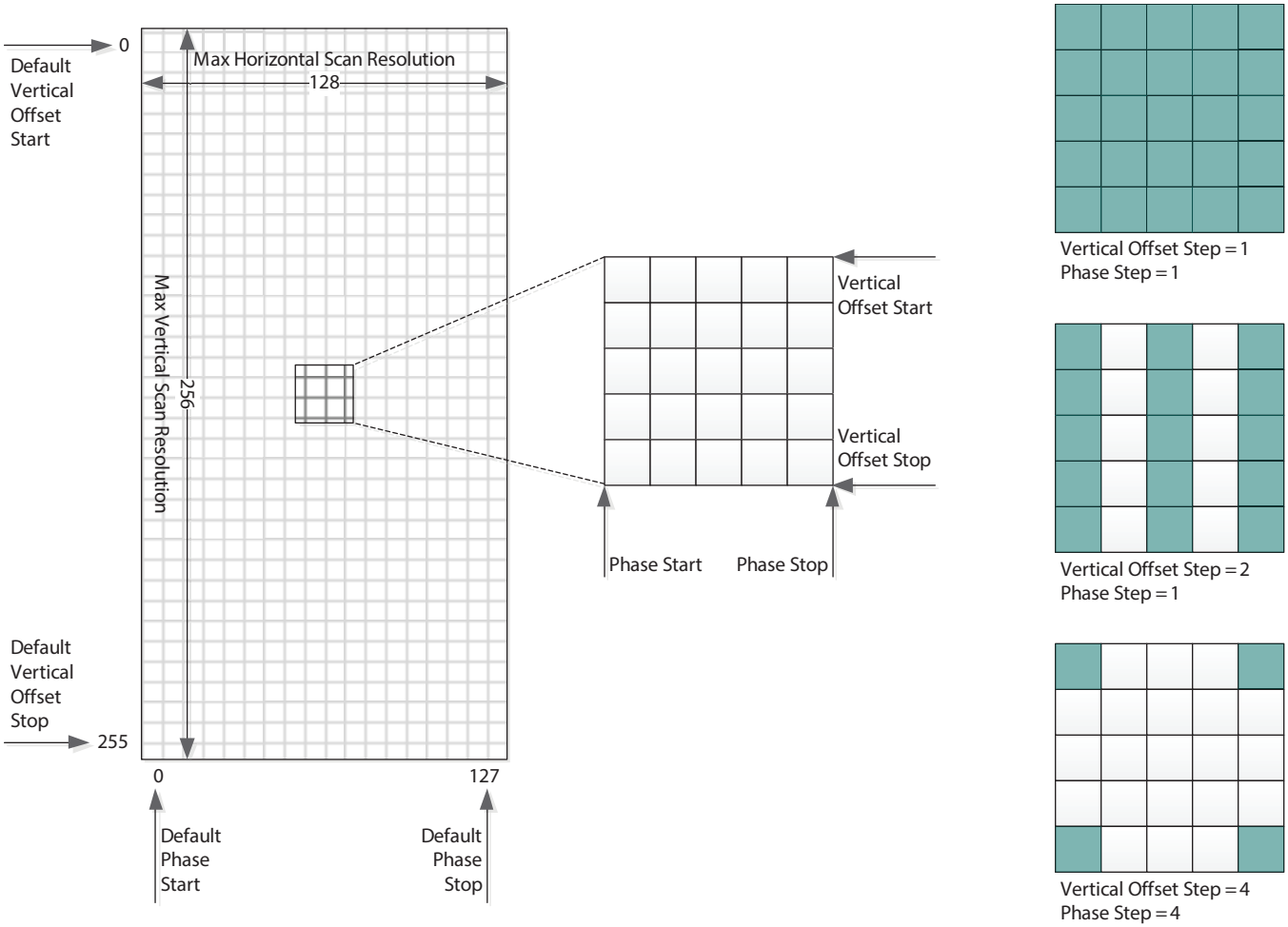


Figure 4-7: Eye Scan Matrix Parameters

Figure 4-7 shows a visual representation of the scan matrix and indicates the spatial parameters that determine the scan area and resolution. Running a scan using the default offset and step parameters, results in 32768 (128x256) samples. The number of samples and thus, the total scan time can be reduced to meet the needs of the application. The scan area can be reduced by reducing the span determined by the vertical and phase start and stop offsets. Or, the resolution can be reduced by increasing the step size between adjacent samples. On the right in Figure 4-7, there are three step settings used as examples, however there are a total of nine combinations possible. See Table 4-6 for the register addresses and parameter names of the spatial eye scan parameters.

For example, by increasing the vertical and phase step size to 4, the resolution is reduced to $(1/4)^2$, thus reducing the number of samples down to 2048 (32768x1/16).

The vertical and horizontal scan information is useful when adjusting pre-emphasis and equalization of a link. However, once this is accomplished, it may be sufficient to use the Eye Scanner to only monitor jitter by setting the offsets to simply slice the eye at the centre offset position, thus obtaining a simple 128 sample horizontal scan. A horizontal eye can be configured to run in just over a millisecond.

In addition to the spatial parameters, the sample time, and thus the bit error rate resolution for the eye scan can be adjusted; longer scans can detect finer bit error rates. However, this proportionally increases the total scan time. The sample time in microseconds is determined by a 32-bit time-out value split across two 16 bit registers. See Table 4-7 for the register addresses and parameter names of the time-out eye scan parameters.

For example, using the default spatial and temporal measurement scan parameters, the scan time is approximately 6.6 seconds (32768 x 2 x 100µs). However, by changing the vertical and horizontal step size to 4, the scan time can be reduced to 400ms (2048 x 2 x 100µs).

The error count information can be used as is to determine the minimum inner contour based on the measurement time. However, the basic data can be post processed to determine things like error rate, and error threshold. The following equations provide guidance for user post-processing:

Equation 4-1

$$\mathbf{error\ rate} = \frac{\mathbf{sample\ error\ count}}{\mathbf{sample\ time}}$$

Contour maps can be created by defining error rate thresholds, and grouping sampled points that fall between thresholds.

For example:

Equation 4-2

$$\frac{\mathbf{sample\ time}}{\mathbf{error\ rate\ threshold}\ 1} < \mathbf{sample\ error\ threshold} < \frac{\mathbf{sample\ time}}{\mathbf{error\ rate\ threshold}\ 2}$$

Some sampling scopes provide eye maps with BER contours; similar limited BER contour approximations can be obtained from the eye scan by using BER threshold groups.

For example:

Equation 4-3

$$\frac{\mathbf{sample\ time\ x\ data\ rate}}{\mathbf{error\ rate\ threshold}\ 1} < \mathbf{sample\ error\ threshold} < \frac{\mathbf{sample\ time\ x\ data\ rate}}{\mathbf{error\ rate\ threshold}\ 2}$$

Table 4-6: Spatial Scan Configuration Parameters

Register Address$_h$ and Name	Parameter Name	Description
5A, EYE_MON_ SCAN_CTRL_0	CTRL_EYE_PHASE_START	Horizontal phase start index
	CTRL_EYE_PHASE_STOP	Horizontal phase stop index
5B, EYE_MON_ SCAN_CTRL_1	CTRL_EYE_PHASE_STEP	Horizontal phase step size
	CTRL_EYE_VERT_OFFSET_START	Vertical offset start index
5C, EYE_MON_ SCAN_CTRL_2	CTRL_EYE_VERT_OFFSET_STOP	Vertical offset stop index
	CTRL_EYE_VERT_OFFSET_STEP	Vertical offset step size

4.6.2 Matrix-Scan and Shape-Scan Operation

The previous section described the parameters used to adjust the spatial and temporal eye scan settings. Each sample of the eye scan can record up to 65536 errors. A full eye scan would require 64KB (256 x 128 x 2 Bytes) of memory to store the data of a full scan. The Eye Monitor was implemented to use device resources more efficiently by segmenting a full scan into several partial scan segments. Each partial scans segment can contain up to 512B of scan data.

In the case of a full matrix-scan, there are 128 partial scan segments and each partial scan segment contains two complete scan lines (2 x 128 x 2B = 512B). In the case of a partial matrix-scan, each scan segment contains multiple partial scan lines including partial lines (see Figure 4-8).

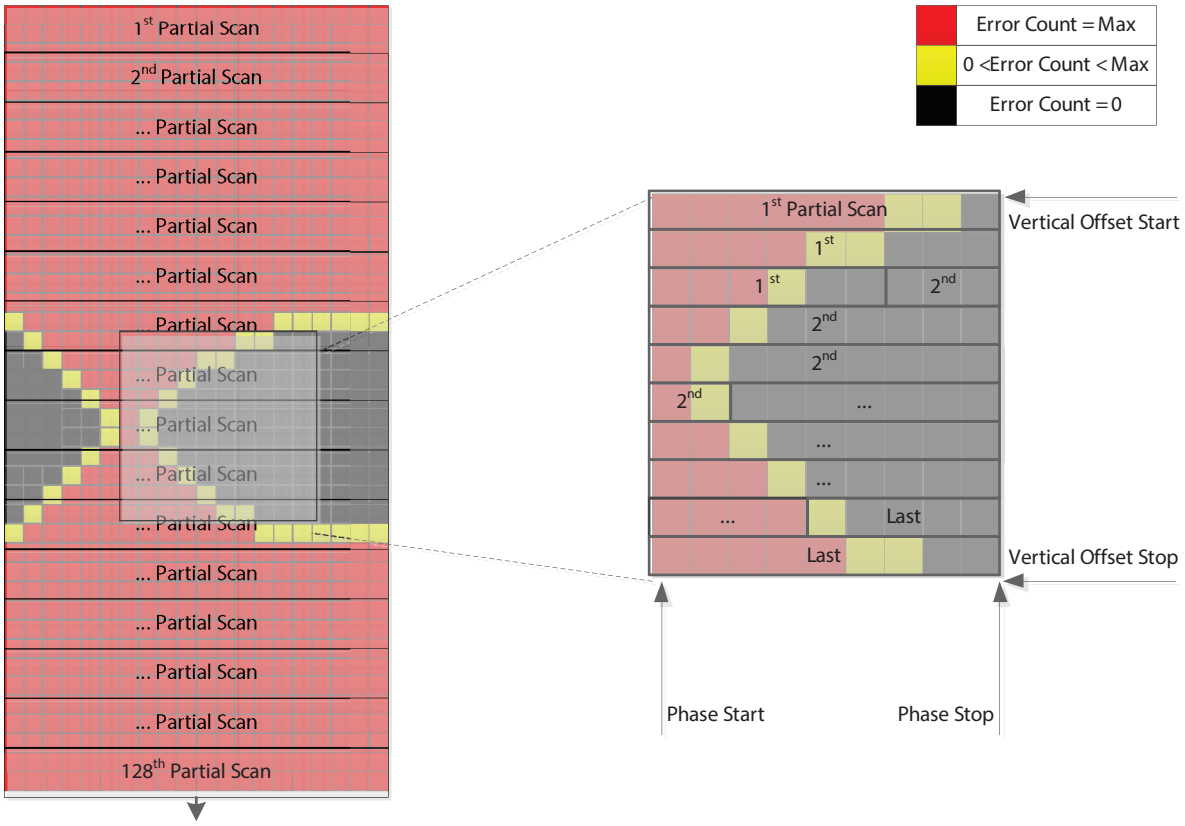


Figure 4-8: Full Matrix Scan (left) and Partial Matrix Scan (right)

Figure 4-7 illustrates an example of an eye scan, where the sampled eye data is not centred within the scan matrix. The eye scan data has an arbitrary centre phase relative to the centre of the matrix which is determined when the Eye Monitor is powered-up. While the Eye Monitor remains powered, subsequent scans will maintain the same relative phase allowing for consecutive scans to be compared for changes.

Although the scan data is not centred, a simple algorithm can be applied to the data to shift the eye data and extract the relevant information.

In addition to the matrix-scan, the Eye Monitor includes a built-in function called a shape-scan. The shape-scan returns four coordinates corresponding to the horizontal and vertical extremes of the inner eye (See Figure 4-9).

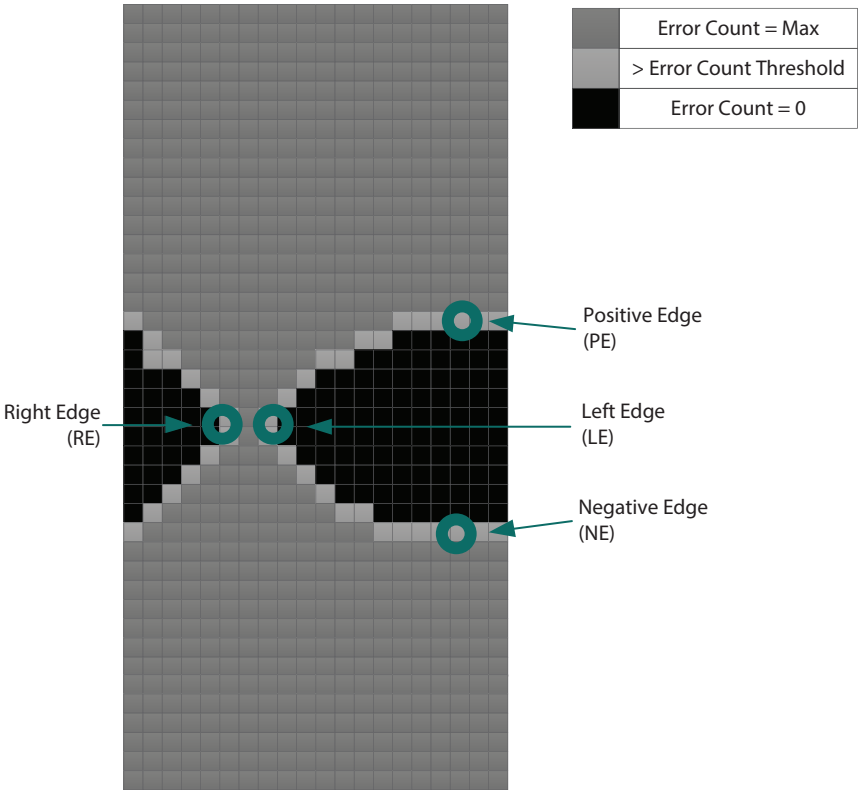


Figure 4-9: 4-Point Scan Coordinates Relative to the Eye

The four points obtained from the shape-scan can be used to quickly and easily calculate the eye height and width of the signal eye. The shape-scan alone will most likely meet the signal analysis requirements of most applications. Alternatively, the coordinates obtained from the shape-scan can be used to optimize the bounds of a partial matrix-scan. The four points returned from the shape-scan are determined by the error rate threshold set by the error threshold parameter and the time-out parameters previously discussed.

Table 4-7: Time-out Eye Scan Parameters

Register Address$_h$ and Name	Parameter Name	Description
56, EYE_MON_ INT_CFG_2	CFG_EYE_BER_THRESHOLD	Number of sample errors to determine fail
54, EYE_MON_ INT_CFG_0	CFG_EYE_MON_TIMEOUT_MS	MSB of measurement time in microseconds
55, EYE_MON_ INT_CFG_1	CFG_EYE_MON_TIMEOUT_LS	LSB of measurement time in microseconds

This section provides a step-by-step procedure to run a matrix and shape-scan. The shape-scan procedure is described first.

Shape-Scan Procedure:

1. Ensure the offset and step parameters described in Table 4-6 are set to their default values.
2. Configure the 4-point error rate threshold by setting each of the parameters listed in Table 4-7.
3. Configure the eye monitor to run a shape-scan by setting **CTRL_EYE_SHAPE_SCAN_B** to 1.
4. Start the scan and poll the scanner status register until the scan is complete. Please refer to the flow diagram in Figure 4-10.

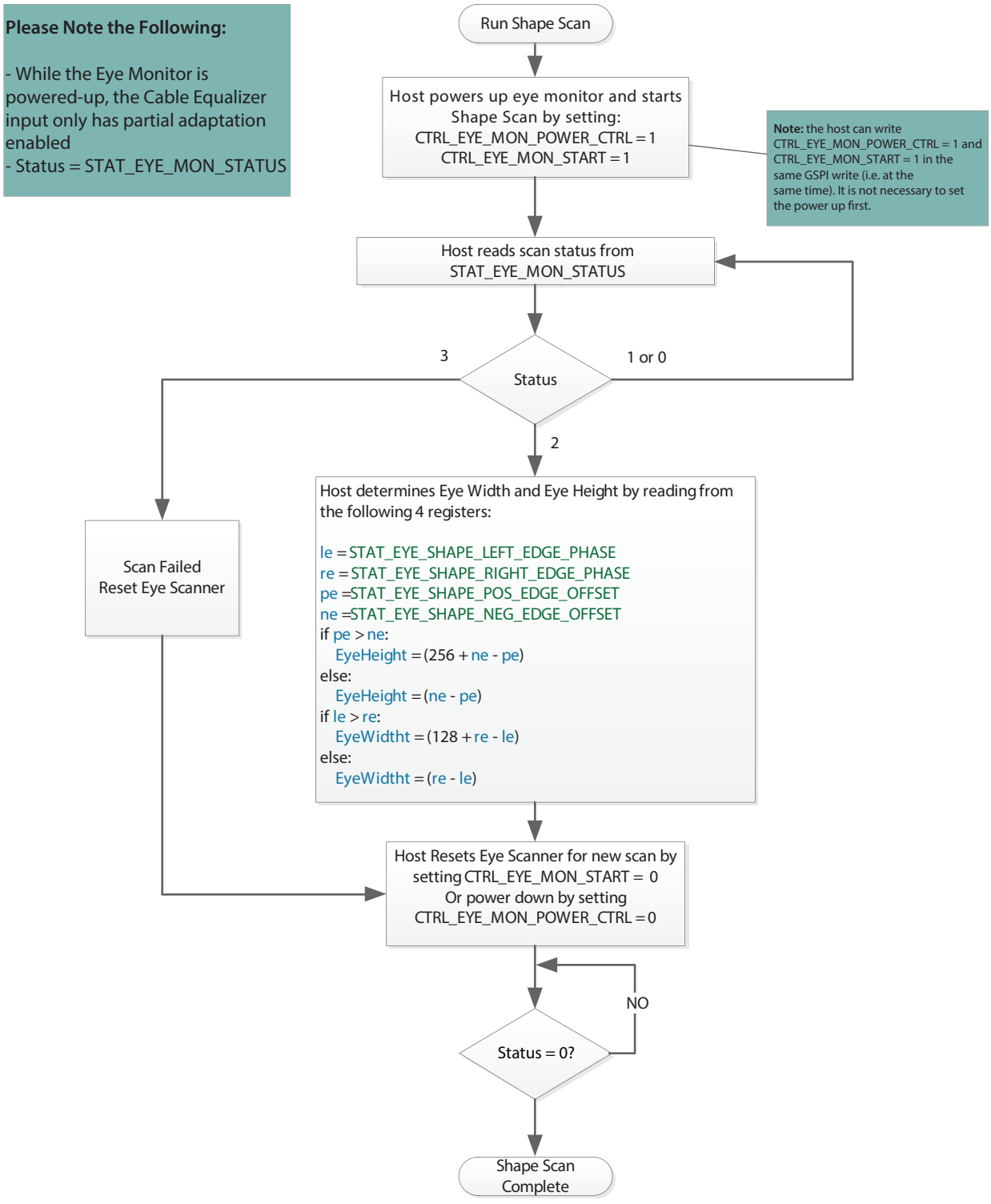


Figure 4-10: Shape-Scan Flow Diagram

Matrix-Scan Procedure:

1. Set the bounds of the matrix-scan with the offset and step parameters described in Table 4-6. The default value results in a full matrix-scan. Alternatively, the shape-scan can be executed and the coordinates returned can be used to minimize the scan time and data size of the scan.
2. Configure the 4-point error rate threshold by setting each of the parameters listed in Table 4-7.
3. Configure the eye monitor to run a matrix-scan by setting **CTRL_EYE_SHAPE_SCAN_B** to 0.
4. Start the scan and poll the scanner status register until the scan is complete. Refer to the flow diagram in Figure 4-11.

Read Eye Scan Buffer Procedure:

1. Host reads image size from **STAT_EYE_IMAGE_SIZE**.
   Note: The matrix-scan is composed of multiple partial scan segments. The size (in Bytes) of the last partial scan segment is stored in **STAT_EYE_IMAGE_SIZE**.
2. Host reads scan buffer data from register 0x6C00 to (0x6C00 + (size read from **STAT_EYE_IMAGE_SIZE**)/2).
   - Address 0x6C00 is the first header word corresponding to the last vertical offset position in the matrix that was read
   - Address 0x6C01 is the second header word corresponding to the image size. This value is a copy of the image size that was read from **STAT_EYE_IMAGE_SIZE**
   - Address 0x6C02 to (0x6C00 + (size read from **STAT_EYE_IMAGE_SIZE**)/2) is the eye scan data:
     - The image data is 2 bytes per sample point
     - Making reference to the Matrix shown in Figure 4-7, the eye scan data starting at 0x6C02 is stored in order from left to right, top to bottom, from the last stored vertical/horizontal position in the matrix
   - The number of samples contained in the scan buffer is equal to (size read from **STAT_EYE_IMAGE_SIZE** - 4)/2

Please Note the Following:

- While the Eye Monitor is powered-up, the Cable Equalizer input only has partial adaptation enabled

- Status = STAT_EYE_MON_STATUS

- Partial = STAT_EYE_SCAN_PARTIAL_OR_FULL

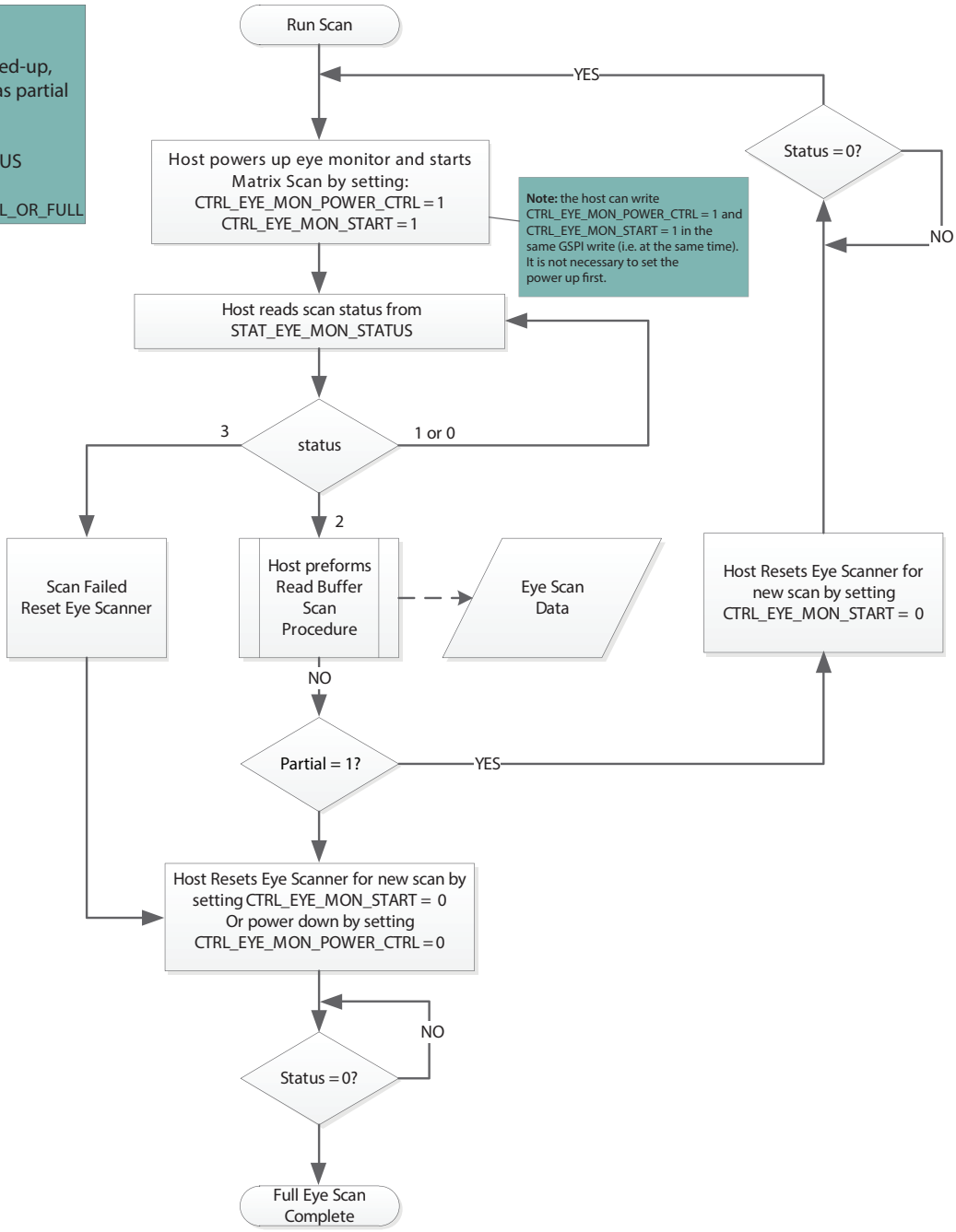


Figure 4-11: Matrix-Scan Flow Diagram

4.7 PRBS Generator

The GS3590 includes an integrated PRBS Generator which can produce a differential PRBS7 or a divided clock signal on *SDIO/$\overline{SDO}$* or *DDO/$\overline{DDO}$* for system testing.

Note: The parameters referred to within this section are briefly described and linked to their respective registers in Table 4-8.

- The PRBS Generator and Checker can be active at the same time. However, the Generator can not be looped-back on itself for error checking

Please consider the following before initializing the PRBS Generator for use:

- Ensure that the directional mode setting is set to utilize the appropriate output. Refer to Section 4.1.1 for more information:
  - Cable Driver Mode PRBS output = *SDIO/$\overline{SDO}$*
  - Cable Equalizer Mode PRBS output = *DDO/$\overline{DDO}$*
- If the application requires adjustment to the default output swing on either PRBS output, please see Section 4.8.4 for details on how to adjust these settings

To configure the PRBS Generator for use, please see the following steps:

1. Select the PRBS Generator as the source on the appropriate output:
   - To switch *DDO/$\overline{DDO}$* from data mode to PRBS generator mode, set **CTRL_OUTPUT1_SIGNAL_SEL** = 1
   - To switch *SDIO/$\overline{SDO}$* from data mode to PRBS generator mode, set **CTRL_OUTPUT0_SIGNAL_SEL** = 1
2. The default device settings are configured to power down the device on loss of input signal. If the PRBS Generator is to be used without a valid input signal, then the following automatic setting parameters must be disabled. This must be done to ensure device is powered up and the outputs are active for the PRBS Generator.

   The following settings are required for PRBS output on either output:

   - **CTRL_AUTO_SLEEP** = 0
   - **CTRL_MANUAL_SLEEP** = 0

   The following settings are required when DDO/$\overline{DDO}$ is selected as PRBS output:

   - **CTRL_OUTPUT1_AUTO_MUTE** = 0
   - **CTRL_OUTPUT1_MANUAL_MUTE** = 0
   - **CTRL_OUTPUT1_AUTO_DISABLE** = 0
   - **CTRL_OUTPUT1_MANUAL_DISABLE** = 0

   The following settings are required when SDIO/$\overline{SDO}$ is selected as PRBS output:

   - **CTRL_OUTPUT0_AUTO_MUTE** = 0
   - **CTRL_OUTPUT0_MANUAL_MUTE** = 0
   - **CTRL_OUTPUT0_AUTO_DISABLE** = 0
   - **CTRL_OUTPUT0_MANUAL_DISABLE** = 0
   - **CTRL_OUTPUT0_AUTO_SLEW** = 0

- Manually set the appropriate slew rate in **CTRL_OUTPUT0_MANUAL_SLEW** for the rate to be selected in **CTRL_PRBS_GEN_DATA_RATE**
  - 0 for SD and MADI
  - 1 for HD and 3G

3. Set the values within the following parameters which meet the needs of the application:
   - **CTRL_PRBS_GEN_SIGNAL_SELECT**
   - **CTRL_PRBS_GEN_CLK_SRC**
   - **CTRL_PRBS_GEN_DATA_RATE**
     - **Note:** If **CTRL_PRBS_GEN_CLK_SRC** was set to CDR recovered clock a valid signal that the CDR has locked to must be present for proper operation, and the PRBS Generator will match this data rate regardless of what rate **CTRL_PRBS_GEN_DATA_RATE** is set to
   - **CTRL_PRBS_GEN_CLK_DIVIDER**
   - **CTRL_PRBS_GEN_INVERT**
4. Start the Generator by setting **CTRL_PRBS_GEN_ENABLE** = 1.

To stop the Generator at any time, set **CTRL_PRBS_GEN_ENABLE** = 0. If the use of the PRBS Generator is complete, revert any settings made in steps 1, 2 and/or 4 to return to normal operation.

Table 4-8 provides a brief description of the parameters used to configure and enable the PRBS Generator. For a detailed description of each parameter, please reference the linked registers.

Table 4-8: PRBS Generator Parameter Descriptions

Register Address$_h$ and Name	Parameter Name	Parameter Description
3, CONTROL_ SLEEP	CTRL_AUTO_SLEEP	Set the device to auto or manual sleep
	CTRL_MANUAL_SLEEP	Manually set the sleep setting of the device when auto sleep mode is turned off
48, OUTPUT_ SIG_SELECT	CTRL_OUTPUT1_SIGNAL_SEL	Selects between data or PRBS Generator as the driver source for DDO/$\overline{\text{DDO}}$
	CTRL_OUTPUT0_SIGNAL_SEL	Selects between data or PRBS Generator as the driver source for SDIO/$\overline{\text{SDO}}$
49, CONTROL_ OUTPUT_ MUTE	CTRL_OUTPUT1_AUTO_MUTE	Select automatic or manual mute control for DD0/$\overline{\text{DDO}}$
	CTRL_OUTPUT1_MANUAL_MUTE	Manually set the mute control for DD0/$\overline{\text{DDO}}$ when auto mute mode is turned off
	CTRL_OUTPUT0_AUTO_MUTE	Select automatic or manual mute control for SDIO/$\overline{\text{SDO}}$
	CTRL_OUTPUT0_MANUAL_MUTE	Manually set the mute control of the SDIO/$\overline{\text{SDO}}$ when auto mute mode is turned off

Table 4-8: PRBS Generator Parameter Descriptions (Continued)

Register Address$_h$ and Name	Parameter Name	Parameter Description
4A, CONTROL_ OUTPUT_ DISABLE	CTRL_OUTPUT1_AUTO_DISABLE	Selects automatic or manual disable control for DD0/$\overline{\text{DDO}}$
	CTRL_OUTPUT1_MANUAL_DISABLE	Manually set the disable control of DD0/$\overline{\text{DDO}}$ when auto disable mode is turned off
	CTRL_OUTPUT0_AUTO_DISABLE	Selects automatic or manual disable control for SDIO/$\overline{\text{SDO}}$
	CTRL_OUTPUT0_MANUAL_DISABLE	Manually set the disable control of the SDIO/$\overline{\text{SDO}}$ when auto disable mode is turned off
4B, CONTROL_ OUTPUT_ SLEW	CTRL_OUTPUT0_AUTO_SLEW	Selects auto or manual slew rate selection for SDIO/$\overline{\text{SDO}}$
	CTRL_OUTPUT0_MANUAL_SLEW	Manually set the slew rate for SDIO/$\overline{\text{SDO}}$ when auto slew mode is turned off
52, PRBS_GEN_ CTRL	CTRL_PRBS_GEN_SIGNAL_SELECT	Selects between setting the output of the PRBS Generator to being a clock or a PRBS test signal
	CTRL_PRBS_GEN_CLK_SRC	Selects the clock source used by the PRBS Generator
	CTRL_PRBS_GEN_CLK_DIVIDER	If a clock is selected as the PRBS output signal, this parameter sets the divide ratio of the clock
	CTRL_PRBS_GEN_INVERT	Allows the polarity of the PRBS signal to be inverted
	CTRL_PRBS_GEN_DATA_RATE	If a PRBS test signal is selected as the output signal, this parameter sets the data rate of the PRBS7 signal
	CTRL_PRBS_GEN_ENABLE	Used to enable or disable the PRBS Generator

4.8 Output Drivers

The GS3590 features two independent output drivers (see Figure 3-2 and Figure 3-3), with data and PRBS Generators available on both outputs. The two drivers provide highly-configurable amplitude and pre-emphasis control. The Cable Driver output on *SDIO* can compensate for significant loss between the device output and BNC. The Trace Driver, *DDO*, can compensate for up 15dB of insertion loss at 1.485GHz. This can represent up to 60" of compensation at 3G for typical micro-strip and strip-line routing. In normal operation, re-timed and bypassed data is available at both outputs. The signal on the outputs can be inverted to help with signal polarity when layout requires trace inversion. The PRBS Generator is available at both outputs. The LOS (Loss Of Signal) status from the equalizer stage can be used to automatically mute or disable the outputs on their assertion. The Loss Of Lock status from the CDR block can be used to mute the outputs. The Cable Driver is always disabled during sleep, while the Trace Driver can be configured to mute or disable during sleep. The sleep control modes takes precedence over the manual or automatic LOS and Loss of Lock output control modes.

Note: The <n> in the control parameter names refers to the output number. Output 0 is the cable driver output *SDIO* and output 1 is the trace driver output *DDO*.

4.8.1 Bypassed Re-timer Signal Output Control

With the default power-up settings, the GS3590 outputs will automatically switch to the bypassed signal (non-re-timed) whenever the PLL is unlocked. Alternatively, manual re-timer bypass may be configured by setting the **CTRL_OUTPUT<n>_RETIMER_AUTO_BYPASS** and **CTRL_OUTPUT<n>_RETIMER_MANUAL_BYPASS** parameters in register 0x4C to 0_b and 1_b respectively via the host interface, in which case the PLL will remain bypassed for all rates.

The re-timer bypass function, manual or automatic, does not affect the input equalization function of the device.

If the GS3590 is in Cable Driver Mode, and loop-back is not enabled, then setting *SDIO* to manual bypass will power-down the CDR block and features of the re-timer such as rate detect and lock detect will no longer be accessible in this mode. The same is true if the GS3590 is in Cable Equalizer Mode and *DDO* is set to manual bypass.

4.8.2 Output Driver Polarity Inversion

While in Data Mode, the signal polarity may be inverted at the outputs through the **CTRL_OUTPUT<n>_DATA_INVERT** parameters in register 0x48. This may be useful to compensate for an inverted upstream signal or to facilitate board signal routing. To invert the polarity of either of the two output drivers, write 1_b to control parameter **CTRL_OUTPUT<n>_DATA_INVERT**.

4.8.3 Output Driver Data Rate Selection

The following information describes the default output driver configuration for each operational mode, and how to modify them if required by the application.

Cable Driver Mode

In cable driver mode, with default settings active, the GS3590 uses the output driver and slew rate group settings for the data rate to which the CDR is locked.

When the CDR is unlocked it will use the Bypass rate group:

- **CFG_OUTPUT0_CD_BYPASS_DRIVER_SWING**
- **CFG_OUTPUT0_CD_BYPASS_PREEMPH_WIDTH**
- **CFG_OUTPUT0_CD_BYPASS_PREEMPH_AMPL**
- **CFG_OUTPUT0_CD_BYPASS_PREEMPH_PWRDWN**

If required, manual selection of the output driver and slew rate group is possible using the following steps:

1. Set **CTRL_OUTPUT0_AUTO_SLEW** = 0
2. Set **CTRL_OUTPUT0_MANUAL_SLEW** to the desired rate group. The slew rate options are as follows:

   0 = SD/MADI
   1 = HD/3G

Trace Driver Mode

In trace driver mode, with default settings active, the GS3590 uses the SD trace driver output group settings for all data rates, regardless of CDR lock condition or data rate being applied.

The following parameters are used to control the output for all data rates in the default condition:

- **CFG_OUTPUT1_TD_SD_DRIVER_SWING**
- **CFG_OUTPUT1_TD_SD_PREEMPH_WIDTH**
- **CFG_OUTPUT1_TD_SD_PREEMPH_AMPL**
- **CFG_OUTPUT1_TD_SD_PREEMPH_PWRDWN**

If required, per-rate selection of the trace driver output group setting is possible by setting **CTRL_OUTPUT1_TRDR_PER_RATE** = 1. Once set, the trace driver output group will be determined by the rate to which the CDR is locked.

For example, if the CDR is locked to 3G, the following parameters will be used to control the output drivers:

- **CFG_OUTPUT1_TD_3G_DRIVER_SWING**
- **CFG_OUTPUT1_TD_3G_PREEMPH_WIDTH**
- **CFG_OUTPUT1_TD_3G_PREEMPH_AMPL**
- **CFG_OUTPUT1_TD_3G_PREEMPH_PWRDWN**

Note: If per-rate settings are being used, when the CDR is not locked the trace driver will use the Bypass trace driver output group settings.

4.8.4 Amplitude and Pre-Emphasis Control

The two output drivers offer very granular amplitude and pre-emphasis control. For optimal loss compensation, both the pre-emphasis pulse amplitude and the pre-emphasis pulse width can be independently configured on both output drivers. This extra flexibility provides a mechanism to better shape the pre-emphasis gain to match the frequency loss response of interconnect composed of trace, connector and via losses. The swing and pre-emphasis can be independently configured for specific data rates.

Note: Output 0 references the Cable Driver, and Output 1 references the Trace Driver.

The output swing on the Cable Driver can be configured for the following three rate groups:

CFG_OUTPUT0_CD_SD_DRIVER_SWING (MADI and SD)
CFG_OUTPUT0_CD_HD_DRIVER_SWING (HD and 3G)
CFG_OUTPUT0_CD_BYPASS_DRIVER_SWING (Bypass)

The output pre-emphasis on the Cable Driver can be configured for the following two rate groups:

CFG_OUTPUT0_CD_HD_PREEMPH_WIDTH (HD and 3G)
CFG_OUTPUT0_CD_HD_PREEMPH_AMPL (HD and 3G)
CFG_OUTPUT0_CD_BYPASS_PREEMPH_WIDTH (Bypass)
CFG_OUTPUT0_CD_BYPASS_PREEMPH_AMPL (Bypass)

The output driver swing and pre-emphasis will use the rate specific swing configuration when the CDR is locked to that rate. The default swing setting is ~800mV$_{pp}$ single-ended into an external 75Ω load, and is adjustable in each of the output swing parameters listed above. The Cable Driver supply is pin 25 (*VCCO_0*) and should be connected to a 2.5V supply. The default pre-emphasis settings provide minimal insertion loss compensation.

The Trace Driver amplitude can be configured to use the same swing for all rates, or similarly to the Cable Driver, can have a specific swing for each rate.

The following registers allow a per rate swing to be configured for 4 rates:

CFG_OUTPUT1_TD_SD_DRIVER_SWING (SD)
CFG_OUTPUT1_TD_HD_DRIVER_SWING (HD)
CFG_OUTPUT1_TD_3G_DRIVER_SWING (3G)
CFG_OUTPUT1_TD_BYPASS_DRIVER_SWING (Bypass)

The output pre-emphasis on the Trace Driver can be configured for the following four rates:

CFG_OUTPUT1_TD_SD_PREEMPH_WIDTH (SD)
CFG_OUTPUT1_TD_SD_PREEMPH_AMPL (SD)
CFG_OUTPUT1_TD_HD_PREEMPH_WIDTH (HD)
CFG_OUTPUT1_TD_HD_PREEMPH_AMPL (HD)
CFG_OUTPUT1_TD_3G_PREEMPH_WIDTH (3G)
CFG_OUTPUT1_TD_3G_PREEMPH_AMPL (3G)
CFG_OUTPUT1_TD_BYPASS_PREEMPH_WIDTH (Bypass)
CFG_OUTPUT1_TD_BYPASS_PREEMPH_AMPL (Bypass)

The Trace Driver swing can be adjusted in ≈25mV$_{pp}$ increments. The default swing value is 400V$_{ppd}$ into an external 100Ω differential load. Although an adequate swing and

pre-emphasis can be achieved with a 1.8V output supply, for long traces where maximum output swing and pre-emphasis range is desired, it is recommended that the device *VCC_DDO* output supply pin be connected to a 2.5V supply. The default pre-emphasis settings provide minimal insertion loss compensation.

4.8.4.1 Pre-emphasis Optimization

The goal of pre-emphasis is to open the eye at the downstream receiver as much as possible. This means minimizing ISI jitter while meeting sufficient inner eye amplitude to meet a receiver's input sensitivity. The Cable Driver has the additional requirement to meet the SMPTE output specification.

The GS3590 has a high level of precision for pre-emphasis control, which allows for fine optimization of any loss channel. The default Cable Driver settings should meet SMPTE output specification for most applications with short (1 to 2 inch) trace between the GS3590 and the output BNC. However, the pre-emphasis values may be adjusted to produce a better-looking eye. It is difficult to provide guidance regarding dB, as a 3G eye diagram looks different depending on the video test equipment used. The designer must optimize for their targets.

The only requirement of the Trace Driver pre-emphasis settings is to minimize ISI introduced by a lossy link and maximize the eye opening at the receiver. The pre-emphasis compensation of the GS3590 output channel is a two-step process. The first step is to use the settings from Figure 4-12 to Figure 4-19 that best match the insertion loss of the link in the application, while the second step is a fine optimization procedure.

In most cases, where the downstream device has a CDR, the first step alone may meet the design target. However, if the downstream device is a non-re-timed buffer or crosspoint, it may be required to further optimize the settings to minimize the jitter thereby maximizing the system jitter budget. To do this, please see the Fine Optimization Procedure.

In the remainder of this section the following abbreviations are used for clarity:

DS = Driver Swing

PPA = Pre-emphasis Pulse Amplitude

PPW = Pre-emphasis Pulse Width

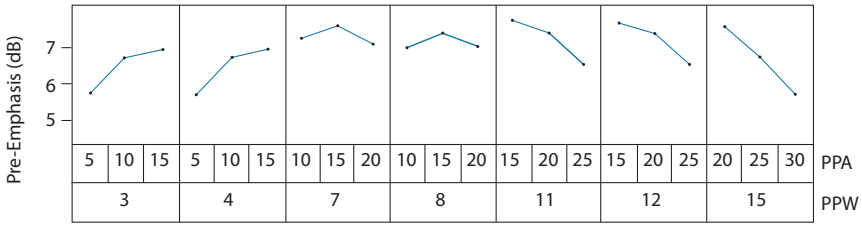


Figure 4-12: Pre-emphasis Settings for VCCO_1 = 1.2V and DS = 7 (swing = 200mV$_{pp}$)

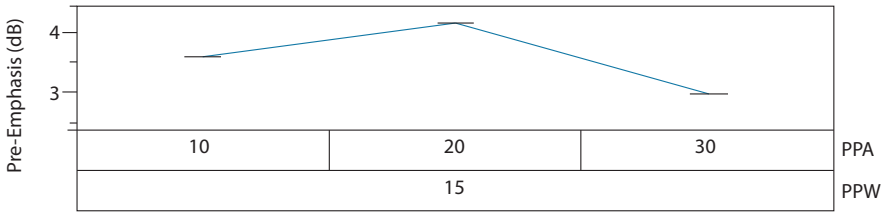


Figure 4-13: Pre-emphasis Settings for VCCO_1 = 1.2V and DS = 16 (swing = 400mV$_{pp}$)

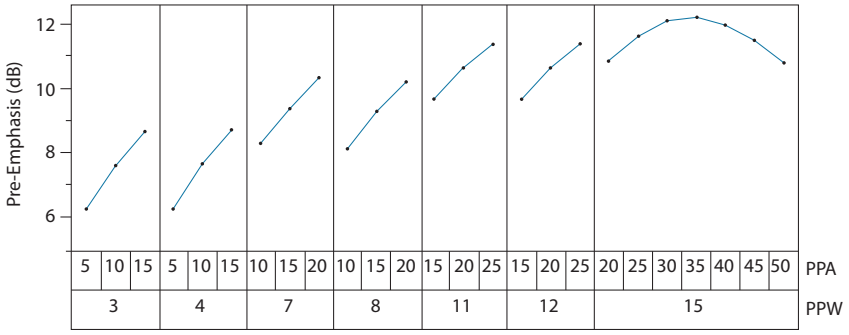


Figure 4-14: Pre-emphasis Settings for VCCO_1 = 1.8V and DS = 7 (swing = 200mV$_{pp}$)

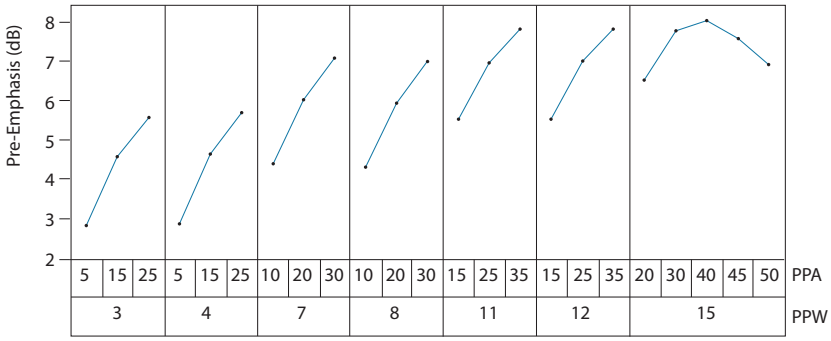


Figure 4-15: Pre-emphasis Settings for VCCO_1 = 1.8V and DS = 16 (swing = 400mV$_{pp}$)

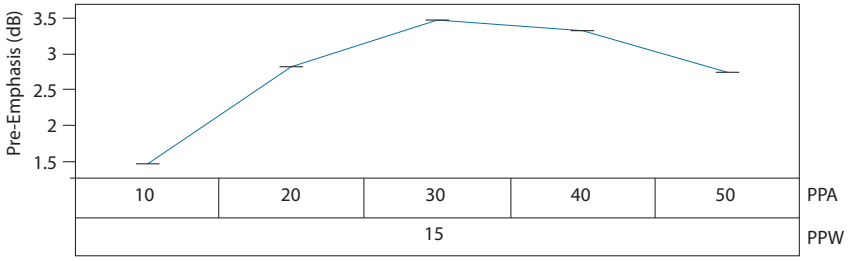


Figure 4-16: Pre-emphasis Settings for VCCO_1 = 1.8V and DS = 35 (swing = 800mV$_{pp}$)

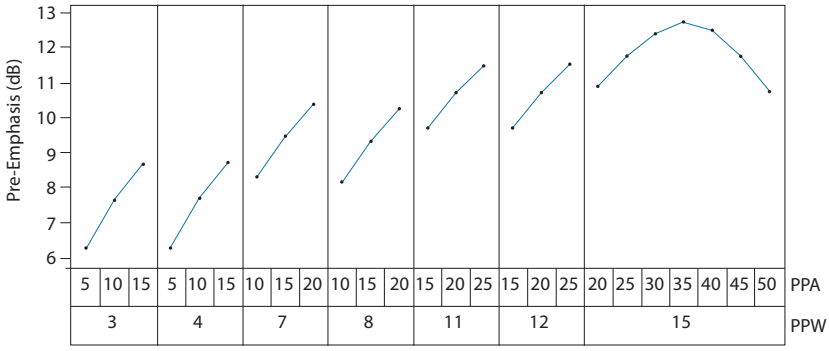


Figure 4-17: Pre-emphasis Settings for VCCO_1 = 2.5V and DS = 7 (swing = 200mV$_{pp}$)

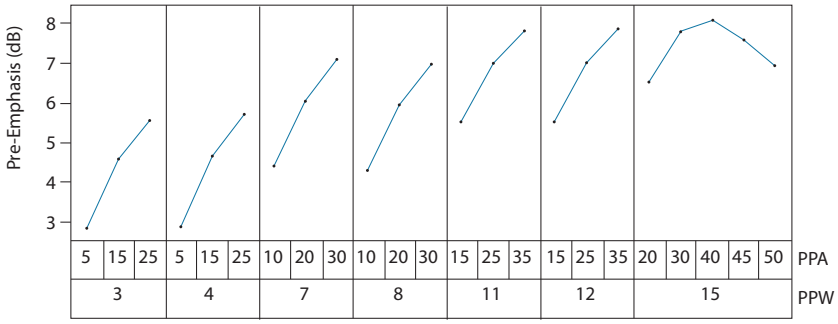


Figure 4-18: Pre-emphasis Settings for VCCO_1 = 2.5V and DS = 16 (swing = 400mV$_{pp}$)

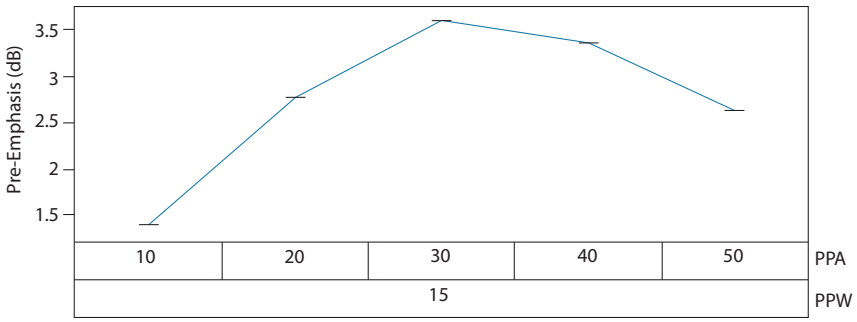


Figure 4-19: Pre-emphasis Settings for VCCO_1 = 2.5V and DS = 35 (swing = 800mV$_{pp}$)

4.8.4.1.1 Fine Optimization Procedure

The procedure requires access to the signal at the downstream device input, or non-re-timed device output. If there are multiple stages between the initial downstream device input and final measurement point, it is still possible to perform optimization; however link settings within the other stages must be fairly optimized. The pre-emphasis amplitude (PPA) and pre-emphasis width (PPW) settings can be optimized by sweeping the PPA and PPW settings in increments of 'a' and 'w' and selecting the setting which results in the lowest jitter. For Trace Driver optimization, 'a' and 'w' increments of 5 should be sufficient.

The procedure has three steps.

1. Pre-emphasis Amplitude (PPA) Optimization: Set the PPA and PPW to the values obtained from the graph selected out of Figure 4-12 to Figure 4-19, and then measure the downstream jitter. While keeping PPW constant, increment the PPA by 'a'. If the jitter is lower after the first increment, continue to increment by 'a' until the jitter begins increasing or a setting of 50 is reached. If there was a setting which resulted in a lower jitter measurement than the initial setting, that is the Optimized Pre-emphasis Amplitude setting: $PPA_{Optimal}$, and the PPA optimization procedure is complete.

   However, if the jitter increased after the first increment, decrement the setting by 'a' below the initial value. If the jitter is lower after the first decrement, continue to decrement by 'a' until the jitter begins increasing or a setting of 0 is reached. If there was a setting which resulted in a lower jitter measurement than the initial setting, that is the Optimized Pre-emphasis Amplitude: $PPA_{Optimal}$.

   If incrementing the PPA or decrementing the PPA did not result in a setting with lower jitter, then the initial setting obtained from the graph selected out of Figure 4-12 to Figure 4-19 is the PPA optimized Pre-emphasis Amplitude setting: $PPA_{Optimal.}$

2. The second step is to set the PPA to the optimized setting $PPA_{Optimal}$ determined in step 1 and PPW to the values obtained from the graph selected out of Figure 4-12 to Figure 4-19, then measure the downstream jitter. While keeping PPA constant, increment the PPW by 'w'. If the jitter is lower after the first increment, continue to increment by 'w' until the jitter begins increasing or a setting of 15 is reached. If there was a setting which resulted in a lower jitter measurement than the initial setting, that is the Optimized Pre-emphasis Width setting: $PPW_{Optimal}$, and the optimization procedure is complete.
   However, if the jitter increased after the first increment, decrement the setting by 'w' below the initial value. If the jitter is lower after the first decrement, continue to decrement by 1 until the jitter begins increasing or a value of 0 is reached. If there was a setting which resulted in a lower jitter measurement than the initial setting, that is the Optimized Pre-emphasis Width setting: $PPW_{Optimal,}$ and the optimization procedure is complete.

   If incrementing the PPW or decrementing the PPW did not result in a setting with lower jitter, then the initial setting value obtained from the graph selected out of Figure 4-12 to Figure 4-19 is the optimized Pre-emphasis Width setting: $PPW_{Optimal}$.

3. Pre-emphasis pulse amplitude has a direct impact on swing amplitude. The third and final step is to readjust the driver swing until the swing amplitude design target is met. The fine optimization procedure maybe repeated to ensure that the $PPA_{Optimal}$ and $PPW_{Optimal}$ settings previously determined still hold with the new DS setting.

Steps 1 and 2 are illustrated in Figure 4-20: PPA Optimization Flow Chart and Figure 4-21: PPW Optimization Flow Chart below.

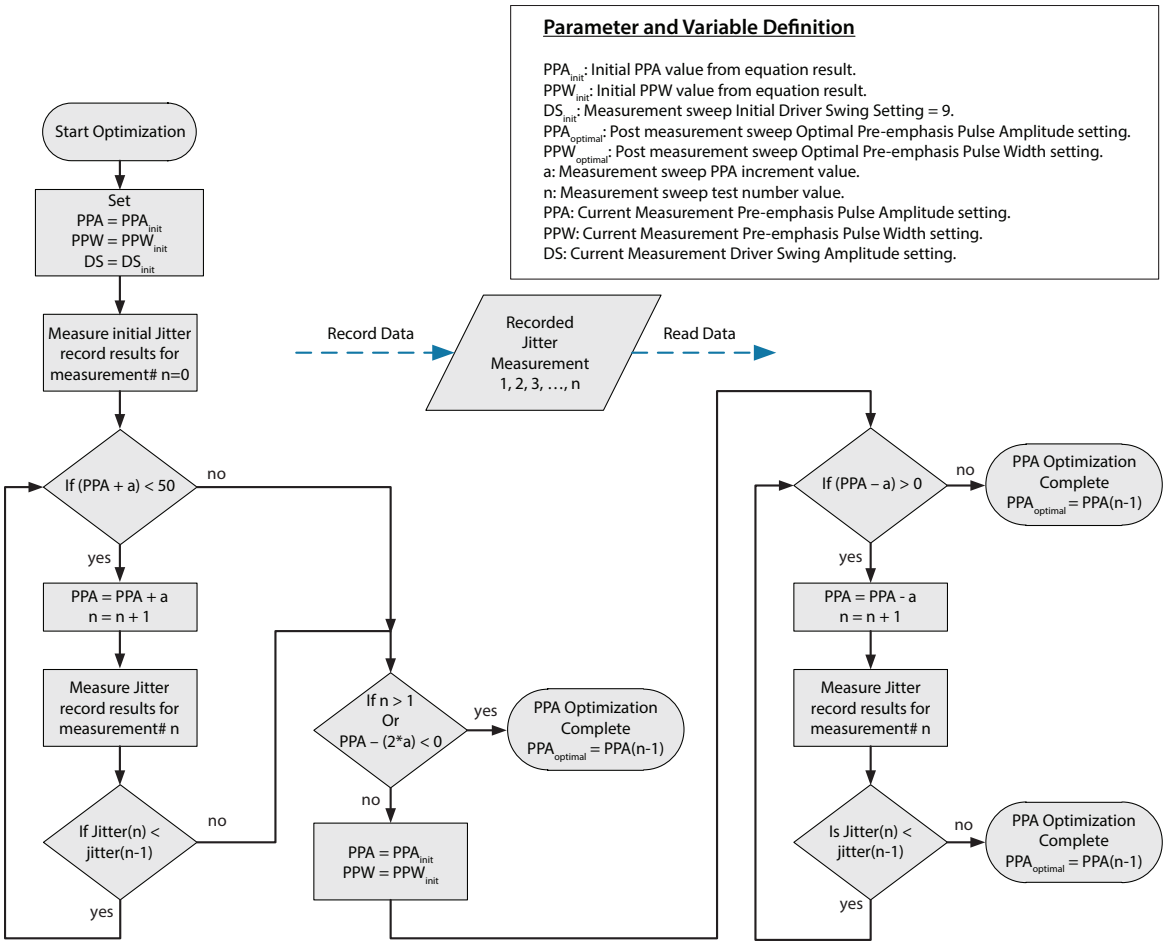


Figure 4-20: PPA Optimization Flow Chart

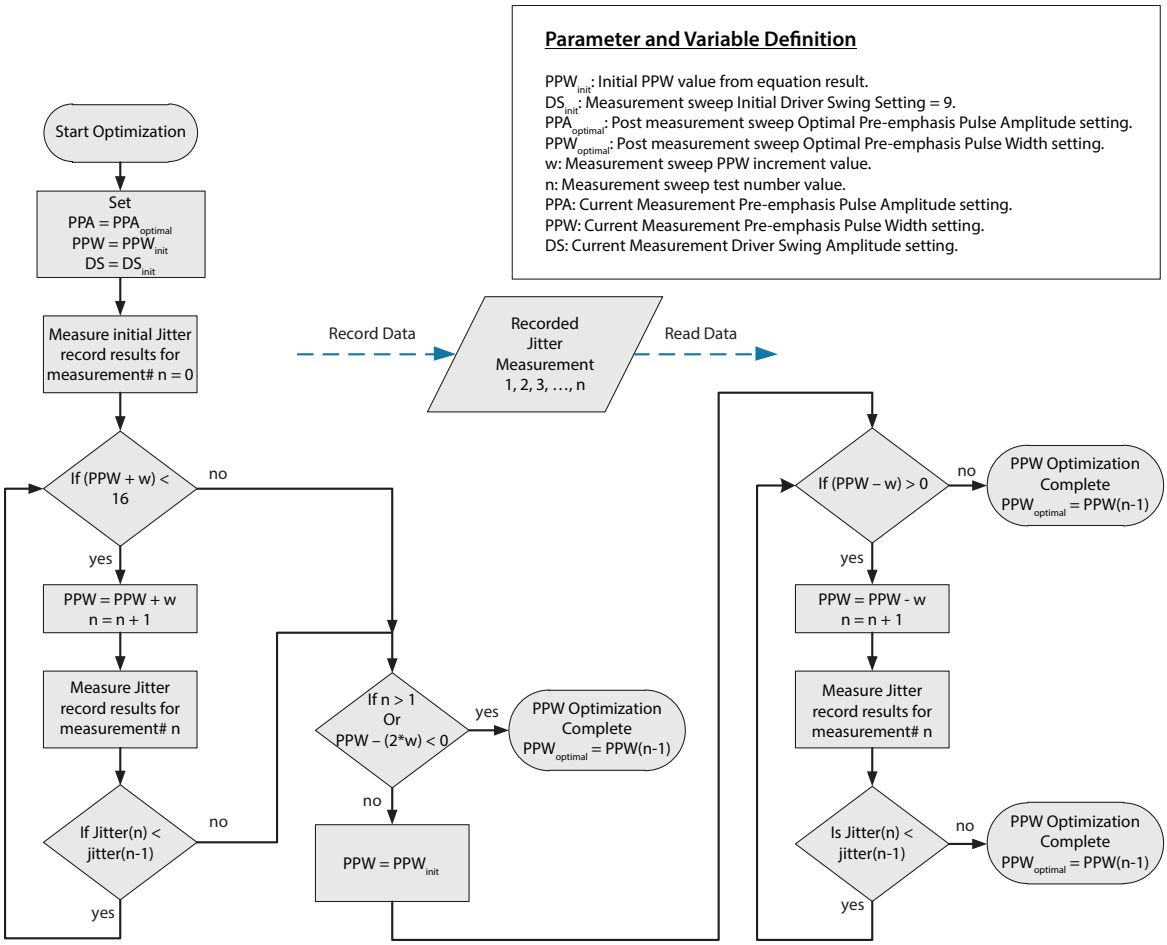


Figure 4-21: PPW Optimization Flow Chart

Table 4-9: Output Swing and Pre-emphasis Control Parameters

Register Address$_h$ and Name	Parameter Name	Description
2B/29 OUTPUT_PARAM_CD_SD_3/OUTPUT_PARAM_TD_SD_1	CFG_OUTPUT<n>_CD/TD_SD_DRIVER_SWING	Output amplitude configuration parameter. <n>=0:For SD and MADI rates on SDIO. <n>=1:For SD or all rates* on DDO. **Note:** If CTRL_OUTPUT1_TRDR_PER_RATE = 0, this setting will be used for all data rates output form DDO.
2A/28 OUTPUT_PARAM_CD_SD_2/OUTPUT_PARAM_TD_SD_0	CFG_OUTPUT<n>_CD/TD_SD_PREEMPH_WIDTH	Output pre-emphasis pulse width configuration parameter. <n>=0:Reserved - do not modify. <n>=1:For SD or all rates* on DDO. **Note:** If CTRL_OUTPUT1_TRDR_PER_RATE = 0, this setting will be used for all data rates output form DDO.
	CFG_OUTPUT<n>_CD/TD_SD_PREEMPH_PWRDWN	Output pre-emphasis power-down configuration parameter. <n>=0:Reserved - do not modify. <n>=1:For SD or all rates* on DDO. **Note:** If CTRL_OUTPUT1_TRDR_PER_RATE = 0, this setting will be used for all data rates output form DDO.
	CFG_OUTPUT<n>_CD/TD_SD_PREEMPH_AMPL	Output amplitude configuration parameter. <n>=0:Reserved - do not modify. <n>=1:For SD or all rates* on DDO. **Note:** If CTRL_OUTPUT1_TRDR_PER_RATE = 0, this setting will be used for all data rates output form DDO.
2D/2F OUTPUT_PARAM_TD_HD_1/OUTPUT_PARAM_CD_HD_3	CFG_OUTPUT<n>_CD/TD_HD_DRIVER_SWING	Output amplitude configuration parameter. <n>=0:For HD and 3G rates on SDIO. <n>=1: For HD rates on DDO.
2C/2E OUTPUT_PARAM_TD_HD_0/OUTPUT_PARAM_CD_HD_2	CFG_OUTPUT<n>_CD/TD_HD_PREEMPH_WIDTH	Output pre-emphasis pulse width configuration parameter. <n>=0:For HD and 3G rates on SDIO. <n>=1:For HD rates on DDO.
	CFG_OUTPUT<n>_CD/TD_HD_PREEMPH_PWRDWN	Output pre-emphasis power-down configuration parameter. <n>=0:For HD and 3G rates on SDIO. <n>=1:For HD rates on DDO.
	CFG_OUTPUT<n>_CD/TD_HD_PREEMPH_AMPL	Output pre-emphasis power-down configuration parameter. <n>=0:For HD and 3G rates on SDIO. <n>=1:For HD rates on DDO.

Table 4-9: Output Swing and Pre-emphasis Control Parameters (Continued)

Register Address$_h$ and Name	Parameter Name	Description
31/33 OUTPUT_PARAM_TD_3G_1/ OUTPUT_PARAM_CD_BYPASS_3	CFG_OUTPUT<n>_TD/CD_3G/BYPASS_DRIVER_SWING	Output amplitude configuration parameter. <n>=0:Bypass. <n>=1:For 3G rates on DDO.
30/32 OUTPUT_PARAM_TD_3G_0/ OUTPUT_PARAM_CD_BYPASS_2	CFG_OUTPUT<n>_TD/CD_3G/BYPASS_PREEMPH_WIDTH	Output pre-emphasis pulse width configuration parameter. <n>=0:Bypass. <n>=1:For 3G rates on DDO.
	CFG_OUTPUT<n>_TD/CD_3G/BYPASS_PREEMPH_PWRDWN	Output pre-emphasis power-down configuration parameter. <n>=0:Bypass. <n>=1:For 3G rates on DDO.
	CFG_OUTPUT<n>_TD/CD_3G/BYPASS_PREEMPH_AMPL	Output pre-emphasis pulse amplitude configuration parameter. <n>=0:Bypass. <n>=1:For 3G rates on DDO.
39 OUTPUT_PARAM_TD_BYPASS_1	CFG_OUTPUT1_TD_BYPASS_DRIVER_SWING	DDO Trace Driver amplitude configuration parameter for Bypass.
38 OUTPUT_PARAM_TD_BYPASS_0	CFG_OUTPUT1_TD_BYPASS_PREEMPH_WIDTH	DDO Trace Driver output pre-emphasis pulse width configuration parameter for Bypass.
	CFG_OUTPUT1_TD_BYPASS_PREEMPH_PWRDWN	DDO output pre-emphasis power-down configuration parameter for Bypass.
	CFG_OUTPUT1_TD_BYPASS_PREEMPH_AMPL	DDO Trace Driver output pre-emphasis pulse amplitude configuration parameter for Bypass.

4.8.5 Trace Driver DC-Coupling Requirements

Table 4-10 lists the required V_{cco} (driver supply voltage) and DS (driver swing) required to achieve three common nominal $VDDO_{ppd}$ (peak-to-peak differential output voltages) and their associated nominal V_{cmout} (output common mode voltage).

In the DC-coupled case, where V_{cco} is connected to the same supply as the input buffer supply voltage of the downstream device, V_{cmount} in Table 4-10 is the common mode voltage at the output of the GS3590 driver. For short low-loss transmission lines, this will also be the common mode voltage created at the input termination of the downstream input buffer. However, for long and lossy transmission lines, the amplitude will be attenuated at the downstream receiver and therefore the common mode voltage created at the input termination will be higher and must be measured or simulated for accuracy. For proper link operation, the common mode voltage created at the input termination of the downstream input buffer must be within the V_{cmin} range specified by that device.

In the AC-coupled case, V_{cmout} is the common mode voltage at the driver side of the AC-coupling capacitor placed near the driver. In the AC-coupled case, V_{cmout} does not need to be within the V_{cmin} range specified by the downstream device. However, the capacitor should have a voltage rating that exceeds $|V_{cmout}-V_{cmin}|$. In addition to the voltage rating, the recommended value of the AC-coupling capacitor should be at least 4.7µF to meet the low cut-off frequency requirement of low transition density signals such as the check-field pattern defined in SMPTE RP-198. The capacitor should have a temperature rating that maintains the capacitance over the required operating range.

Table 4-10: ΔV_{DDO} (mV_{ppd}) and V_{CMOUT}(V) vs. DS Setting and V_{CCO}

	ΔV_{DDO} (mV_{ppd}) vs. DS Setting			DC-Coupled V_{CMOUT} (V) vs. DS Setting			AC-Coupled V_{CMOUT} (V) vs. DS Setting		
V_{cco} (V)	8	17	37	8	17	37	8	17	37
1.2	200	400	—	1.15	1.1	—	1.1	1	—
1.8	200	400	800	1.75	1.7	1.6	1.7	1.6	1.4
2.5	200	400	800	2.45	2.4	2.3	2.4	2.3	2.1

4.8.6 Output State Control Modes

The GS3590 provides several output state control modes to meet specific application requirements. The Trace Driver has the following three output modes: operational, muted, or disabled. The Cable Driver also has these three modes and additionally has a balanced mode. During non-sleep, if the control modes are configured such that multiple output modes are enabled, the priorities of the control modes from highest to lowest are the following: balanced (Cable Driver only), disabled, and then muted. Section 4.8.6.1 through Section 4.8.6.3 describe how to configure the output control modes that are enabled during non-sleep.

If the device enters sleep, either manually or automatically, the sleep output control modes take precedence over the non-sleep control modes. During sleep, the Cable Driver will always be disabled, while the Trace Driver can be configured to mute or disable during sleep. The default Trace Driver configuration is for it to be disabled during sleep; however the Trace Driver can be configured to mute during sleep by setting the **CFG_SLEEP_OUTPUT1_MUTE** parameter in register 0x5 to 1_b.

4.8.6.1 Output Mute Control Mode

Each of the outputs on the GS3590 have independent mute control modes, which can be configured through the host interface.

The following are the four output mute control modes:

1. The outputs automatically mute on LOS (default).
2. The outputs automatically mute on LOS and during rate search.
3. The outputs never mute.
4. The outputs are always muted.

The first mute control mode is the default power-up configuration for both output drivers (the **CTRL_OUTPUT<n>_AUTO_MUTE** control parameter in register 0x49 is set to 1_b). In this mode, the outputs will automatically mute on the assertion of LOS. This includes LOS as a result of setting up Squelch Adjust (see Section 4.2.3 for more details). In addition to mute on LOS, with auto mute control mode configured, setting the **CTRL_OUTPUT<n>_AUTO_MUTE_DURING_RATE_SEARCH** control parameter in register 0x49 to 1_b, will configure the outputs to also mute when the device loses lock and begins to rate search.

The outputs can be manually configured to never mute by setting both the **CTRL_OUTPUT<n>_AUTO_MUTE** and **CTRL_OUTPUT<n>_MANUAL_MUTE** control parameters in register 0x49 to 0_b. Alternatively, the outputs can be manually configured to always be muted by setting the **CTRL_OUTPUT<n>_AUTO_MUTE** and **CTRL_OUTPUT<n>_MANUAL_MUTE** control parameters to 0_b and 1_b respectively.

4.8.6.2 Output Disable Control Mode

Each of the outputs on the GS3590 also have independent disable control modes, which can be configured through the host interface.

The following are the three output disable control modes:

1. The outputs are never disabled (default).
2. The outputs are automatically disabled on LOS.
3. The outputs are always disabled.

The first disable control mode is the default power-up configuration for both output drivers (the **CTRL_OUTPUT<n>_AUTO_DISABLE** and **CTRL_OUTPUT<n>_MANUAL_DISABLE** control parameters in register 0x4A are both set to 0_b). In this mode, the outputs will never disable. By setting the **CTRL_OUTPUT<n>_AUTO_DISABLE** control parameter in register 0x4A to 1_b, the outputs will automatically disable on the assertion of LOS. This includes LOS as a result of setting up Squelch Adjust (see Section 4.2.3 for more details).

The output can be manually disabled by leaving the **CTRL_OUTPUT<n>_AUTO_DISABLE** control parameter set to 0_b and setting the **CTRL_OUTPUT<n>_MANUAL_DISABLE** control parameter to 1_b.

The disable control mode takes precedence over the output mute control mode.

4.8.6.3 Output Balanced Control Mode

The GS3590 has a feature designed to facilitate reliable Output Return Loss (ORL) measurements on *SDIO/$\overline{SDO}$* while the device is still powered. The device can be put into BALANCE mode which prevents the outputs from toggling while ORL is being measured. BALANCE mode can be enabled through the host interface, by setting control parameter **CTRL_OUTPUT0_BALANCED** in register $4D_h$ to 1_b. This control is solely for the Cable Driver output. This control mode takes precedence over both the output mute and output disable control modes.

4.8.6.4 Loopback Control

The GS3590 has the ability to loop a re-clocked version of the signal applied to the trace equalizer input (DDI) to the trace driver output (DDO) while in Cable Driver Mode. To enable this feature set **CTRL_LOOPBACK_ENA** to 1.

With default settings applied, and the device set to Cable Driver Mode, the Trace Driver is inactive and it is controlled by the **CFG_TRDR_MUTE_WHEN_CABLE_DRIVER** parameter to determine whether it is muted or disabled. Once **CTRL_LOOPBACK_ENA** is set to 1, it overrides any setting in **CFG_TRDR_MUTE_WHEN_CABLE_DRIVER**.

Note: When using the Loopback feature, please note the following:

- The Loopback signal of DDI appearing on DDO will be only be re-clocked if the device is locked to the signal applied to the trace equalizer input (DDI). If the CDR is bypassed or not locked, the loopback signal will not be re-clocked.

- The output state control modes described in Section 4.8.6.1 to Section 4.8.6.3 (disable, mute, and balanced) take priority over the **CTRL_LOOPBACK_ENA** parameter.
- This mode is only applicable to Cable Driver Mode, using DDI as the input.

4.9 GPIO Controls

There are four configurable *GPIO* pins which can independently be configured as inputs or outputs. Each *GPIO* has a default function which can be re-configured through the host interface.

If there is a conflict between the internal register configuration of a given device function and the logic-level applied to a *GPIO* pin that is configured to control that same device function, the GPIO logic-level takes precedence over the internal register configuration. The logic HIGH and LOW levels of the *GPIO[3:0]* pin to which LOS is connected are specified by the EIA/JESD8-5A standard for 1.8V operation.

For a list of available functions and configuration details of *GPIO[3:0]*, please refer to the GPIO Configuration Registers in Section 5.

4.10 GSPI Host Interface

The GS3590 is configured via the Gennum Serial Peripheral Interface (GSPI).

The GSPI host interface is comprised of a serial data input signal (*SDIN* pin), serial data output signal (*SDOUT* pin), an active-LOW chip select ($\overline{CS}$ pin) and a burst clock (*SCLK* pin).

The GS3590 is a slave device, so the SCLK, SDIN and $\overline{CS}$ signals must be sourced by the application host processor.

All read and write access to the device is initiated and terminated by the application host processor.

4.10.1 $\overline{CS}$ Pin

The Chip Select pin ($\overline{CS}$) is an active-low signal provided by the host processor to the GS3590.

The HIGH-to-LOW transition of this pin marks the start of serial communication to the GS3590.

The LOW-to-HIGH transition of this pin marks the end of serial communication to the GS3590.

Each device may use its own separate Chip Select signal from the host processor or up to 32 devices may be connected to a single Chip Select when making use of the Unit Address feature.

Only those devices whose Unit Address matches the UNIT ADDRESS in GSPI Command Word 1 will respond to communication from the host processor (unless the B'CAST ALL bit in GSPI Command Word 1 is set to 1).

4.10.2 SDIN Pin

The *SDIN* pin is the GSPI serial data input pin of the GS3590.

The 32-bit Command and 16-bit Data Words from the host processor or from the *SDOUT* pin of other devices are shifted into the device on the rising edge of SCLK when the $\overline{CS}$ pin is LOW.

4.10.3 SDOUT Pin

The *SDOUT* pin is the GSPI serial data output of the GS3590.

All data transfers out of the GS3590 to the host processor or to the *SDIN* pin of other connected devices occur from this pin.

By default at power-up or after system reset, the *SDOUT* pin provides a non-clocked path directly from the *SDIN* pin, regardless of the $\overline{CS}$ pin state, except during the GSPI Data Word portion for read operations from the device. This allows multiple devices to be connected in Loop-Through configuration.

For read operations, the *SDOUT* pin is used to output data read from an internal Configuration and Status Register (CSR) when $\overline{CS}$ is LOW. Data is shifted out of the device on the falling edge of SCLK, so that it can be read by the host processor or other downstream connected device on the subsequent SCLK rising edge.

4.10.3.1 GSPI Link Disable Operation

It is possible to disable the direct *SDIN* to *SDOUT* (Loop-Through) connection by writing a value of 1 to the **GSPI_LINK_DISABLE** bit in **CONTROL_REG**. When disabled, any data appearing at the *SDIN* pin will not appear at the *SDOUT* pin and the *SDOUT* pin is HIGH.

Note: Disabling the Loop-Through operation is temporarily required when initializing the Unit Address for up to 32 connected devices.

The time required to enable/disable the Loop-Through operation from assertion of the register bit is less than the GSPI configuration command delay as defined by the parameter $t_{cmd_GSPI_config}$ (4 SCLK cycles).

Table 4-11: GSPI_LINK_DISABLE Bit Operation

Bit State	Description
0	SDIN pin is looped through to the SDOUT pin
1	Data appearing at SDIN does not appear at SDOUT, and SDOUT pin is HIGH.

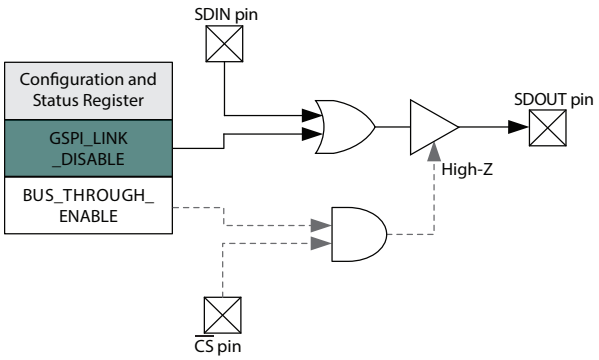


Figure 4-22: GSPI_LINK_DISABLE Operation

4.10.3.2 GSPI Bus-Through Operation

Using GSPI Bus-Through operation, the GS3590 can share a common PCB trace with other GSPI devices for SDOUT output.

When configured for Bus-Through operation, by setting **GSPI_BUS_THROUGH_ENABLE** bit to 1, the *SDOUT* pin will be high-impedance when the $\overline{CS}$ pin is HIGH.

When the $\overline{CS}$ pin is LOW, the *SDOUT* pin will be driven and will follow regular read and write operation as described in Section 4.10.3.

Multiple chains of GS3590 devices can share a single SDOUT bus connection to host by configuring the devices for Bus-Through operation. In such configuration, each chain requires a separate Chip Select ($\overline{CS}$).

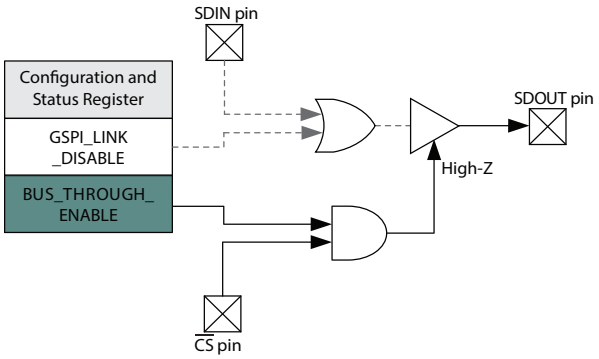


Figure 4-23: GSPI_BUS_THROUGH_ENABLE Operation

4.10.4 SCLK Pin

The *SCLK* pin is the GSPI serial data shift clock input to the device, and must be provided by the host processor.

Serial data is clocked into the GS3590 *SDIN* pin on the rising edge of SCLK. Serial data is clocked out of the device from the *SDOUT* pin on the falling edge of SCLK (read operation). SCLK is ignored when $\overline{CS}$ is HIGH.

The maximum interface clock rate is 27MHz.

4.10.5 Command Word 1 Description

All GSPI accesses are a minimum of 48 bits in length (two 16-bit Command Words followed by a 16-bit Data Word) and the start of each access is indicated by the HIGH-to-LOW transition of the Chip Select ($\overline{CS}$) pin of the GS3590.

The format of the Command Words and Data Word are shown in Figure 4-24.

Data received immediately following this HIGH-to-LOW transition will be interpreted as a new Command Word.

4.10.5.1 R/$\overline{W}$ bit—B15 Command Word 1

This bit indicates a read or write operation.

When R/$\overline{W}$ is set to 1, a read operation is indicated, and data is read from the register specified by the ADDRESS field of the Command Word.

When R/$\overline{W}$ is set to 0, a write operation is indicated, and data is written to the register specified by the ADDRESS field of the Command Word.

4.10.5.2 B'CAST ALL—B14 Command Word 1

This bit is used in write operations to configure all devices connected in Loop-Through and Bus-Through configuration with a single command.

When B'CAST ALL is set to 1, the following Data Word (AUTOINC = 0) or Data Words (AUTOINC = 1) are written to the register specified by the ADDRESS field of the Command Words (and subsequent addresses when AUTOINC = 1), regardless of the setting of the UNIT ADDRESS(es).

When B'CAST ALL is set to 0, a normal write operation is indicated. Only those devices that have a Unit Address matching the UNIT ADDRESS field of Command Word 1 write the Data Word to the register specified by the ADDRESS field of the Command Words.

4.10.5.3 EMEM—B13 Command Word 1

The EMEM bit must be set to 1 in Command Word 1. When EMEM is set to 1, a 23-bit address split between Command Word 1 and Command Word 2 is used to access the registers in this device.

4.10.5.4 AUTOINC—B12 Command Word 1

When AUTOINC is set to 1, Auto-Increment read or write access is enabled.

In Auto-Increment Mode, the device automatically increments the register address for each contiguous read or write access, starting from the address defined in the ADDRESS field of the Command Word.

The internal address is incremented for each 16-bit read or write access until a LOW-to-HIGH transition on the $\overline{CS}$ pin is detected.

When AUTOINC is set to 0, single read or write access is required.

Auto-Increment write must not be used to update values in **CONTROL_REG**.

4.10.5.5 UNIT ADDRESS—B11:B7 Command Word 1

The 5 bits of the UNIT ADDRESS field of the Command Word are used to select one of 32 devices connected on a single chip select in Loop-Through or Bus-Through configurations.

Read and write accesses are only accepted if the UNIT ADDRESS field matches the programmed DEV_UNIT_ADDRESS in **CONTROL_REG**.

By default at power-up or after a device reset, the DEV_UNIT_ADDRESS is set to 00_h.

4.10.5.6 ADDRESS—B6:B0 Command Word 1 and B15:B0 Command Word 2

The Command and Data Word formats are shown in Figure 4-24 and Figure 4-25. As an example of the command word structure, reading register 0x90 from a device with unit address 3, that has AUTOINC = 0, and B'CAST ALL = 0 would be structured as follows:

- Command word 1: 1010 0001 1000 0000 (0xA180)
- Command word 2: 0000 0000 1001 0000 (0x90)

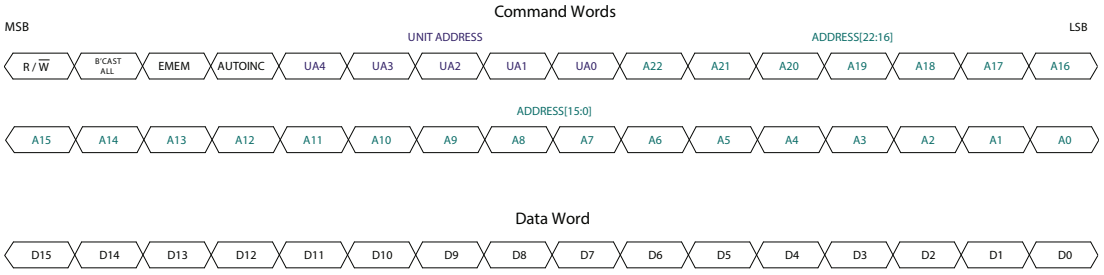


Figure 4-24: Command and Data Word Format

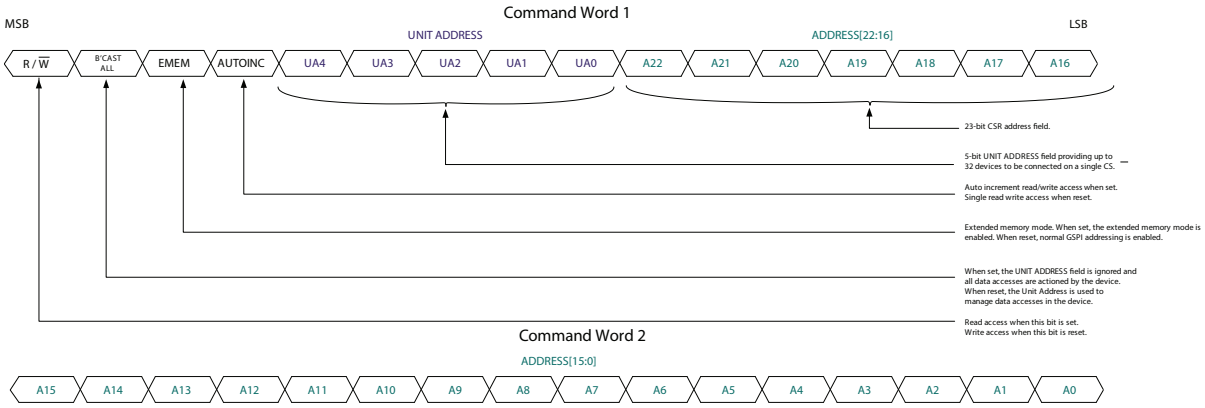


Figure 4-25: Command Word 1 and Command Word 2 Details

Note: Please see Section 4.10.5.6 ADDRESS—B6:B0 Command Word 1 and B15:B0 Command Word 2 for an example of the command word structure.

4.10.6 GSPI Transaction Timing

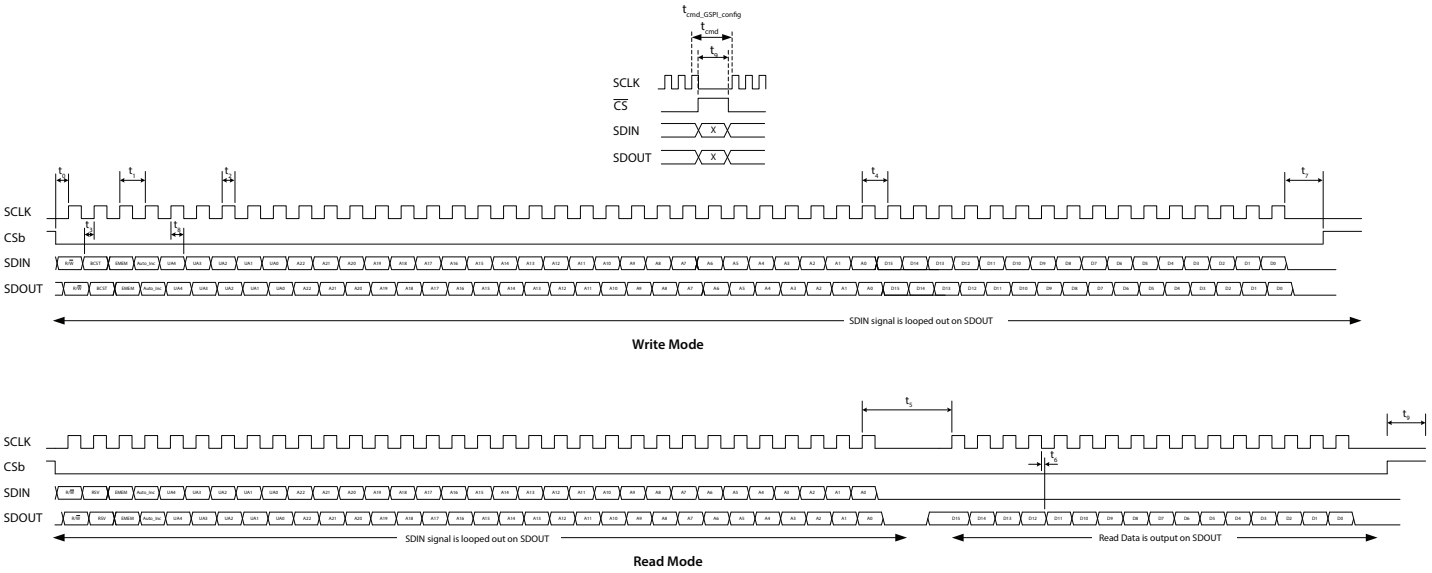


Figure 4-26: GSPI External Interface Timing

Table 4-12: GSPI Timing Parameters

Parameter	Symbol	Equivalent SCLK Cycles	Min	Typ	Max	Units
SCLK Frequency	—	—	—	—	27	MHz
$\overline{CS}$ LOW Before SCLK Rising Edge	t_0	—	1.7	—	—	ns
SCLK Period	t_1	—	37	—	—	ns
SCLK Duty Cycle	t_2	—	40	50	60	%
Input Data Setup Time	t_3	—	2.3	—	—	ns
SCLK Idle Time – Write	t_4	1	38.5[1]	—	—	ns
SCLK Idle Time – Read	t_5	—	138	—	—	ns
Inter–Command Delay Time	t_{cmd}	3	115	—	—	ns
Inter–Command Delay Time (after GSPI configuration write)	$t_{cmd_GSPI_conf}$[2]	4	139	—	—	ns
SDOUT After SCLK Falling Edge	t_6	—	1.3	—	6.4	ns
CS HIGH After Final SCLK Falling Edge	t_7	—	0	—	—	ns
Input Data Hold Time	t_8	—	1.2	—	—	ns
$\overline{CS}$ HIGH Time	t_9	—	58	—	—	ns
SDIN to SDOUT Combinatorial Delay	—	—	—	—	3.4	ns
Max chips daisy-chained at max SCLK frequency (26 MHz)	When host clocks in SDOUT data on falling edge of SCLK		—	—	8	# of compatible Semtech devices
Max frequency for 32 daisy-chained devices			—	—	7.5	MHz

Note:

1. Parameter is exactly multiple of SCLK periods and scales proportionally.
2. $t_{cmd_GSPI_conf}$ inter-command delay must be used whenever modifying CONTROL_REG register at address 0x00.

4.10.7 Single Read/Write Access

Single read/write access timing for the GSPI interface is shown in Figure 4-27 to Figure 4-31.

When performing a single read or write access, one Data Word is read from/written to the device per access. Each access is a minimum of 48-bits long, consisting of two Command Words and a single Data Word. The read or write cycle begins with a HIGH-to-LOW transition of the $\overline{CS}$ pin. The read or write access is terminated by a LOW-to-HIGH transition of the $\overline{CS}$ pin.

The maximum interface clock rate is 27MHz and the inter-command delay time indicated in the figures as t_{cmd}, is a minimum of 3 SCLK clock cycles. After modifying values in **CONTROL_REG**, the inter-command delay time, $t_{cmd_GSPI_config}$, is a minimum of 4 SCLK clock cycles.

For read access, the time from the last bit of Command Word 2 to the start of the data output, as defined by t_5, corresponds to no less than 4 SCLK clock cycles at 27MHz.

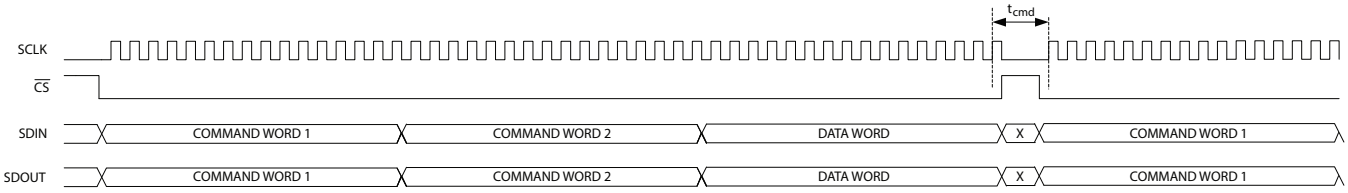


Figure 4-27: GSPI Write Timing—Single Write Access with Loop-Through Operation (default)

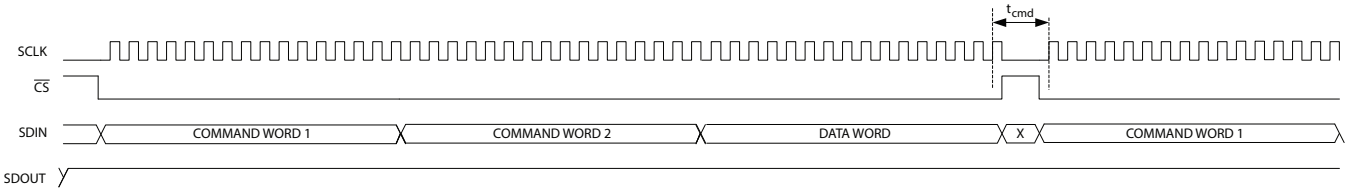


Figure 4-28: GSPI Write Timing—Single Write Access with GSPI Link-Disable Operation

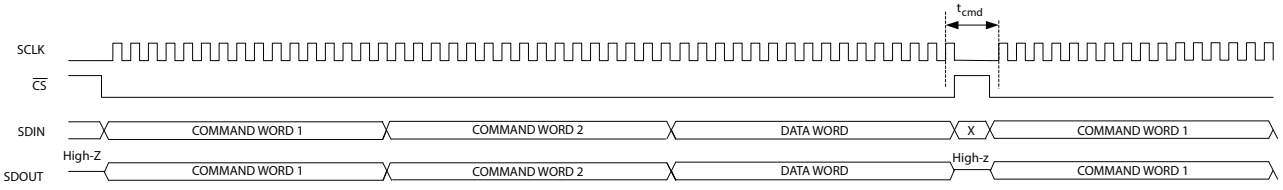


Figure 4-29: GSPI Write Timing—Single Write Access with Bus-Through Operation

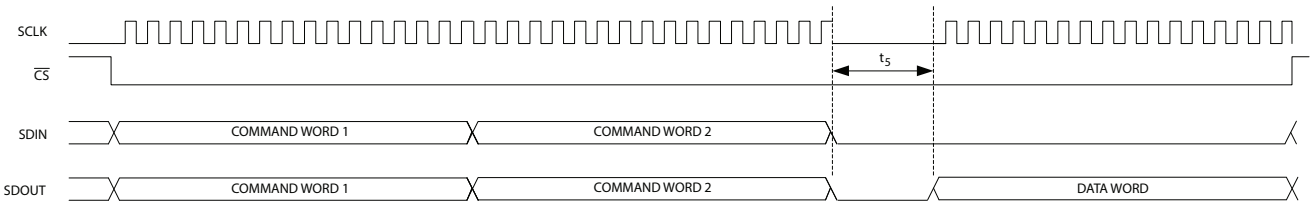


Figure 4-30: GSPI Read Timing—Single Read Access with Loop-Through Operation (default)

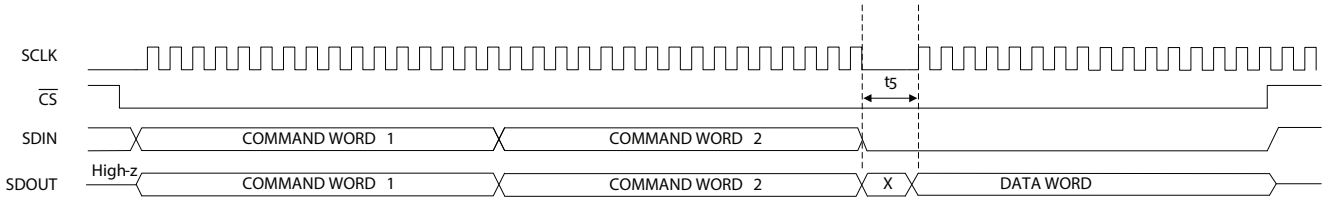


Figure 4-31: GSPI Read Timing—Single Read Access with Bus-Through Operation

4.10.8 Auto-increment Read/Write Access

Auto-increment read/write access timing for the GSPI interface is shown in Figure 4-32 to Figure 4-36.

Auto-increment mode is enabled by the setting the **AUTOINC** bit of Command Word 1.

In this mode, multiple Data Words can be read from/written to the device using only one starting address. Each access is initiated by a HIGH-to-LOW transition of the $\overline{CS}$ pin, and consists of two Command Words and one or more Data Words. The internal address is automatically incremented after the first read or write Data Word, and continues to increment until the read or write access is terminated by a LOW-to-HIGH transition of the $\overline{CS}$ pin.

Note: Writing to **CONTROL_REG** using Auto-increment access is not allowed.

The maximum interface clock rate is 27MHz and the inter-command delay time indicated in the diagram as t_{cmd}, is a minimum of 3 SCLK clock cycles.

For read access, the time from the last bit of the second Command Word to the start of the data output of the first Data Word as defined by t_5 will be no less than 4 SCLK cycles at 27MHz. All subsequent read data accesses will not be subject to this delay during an Auto-Increment read.

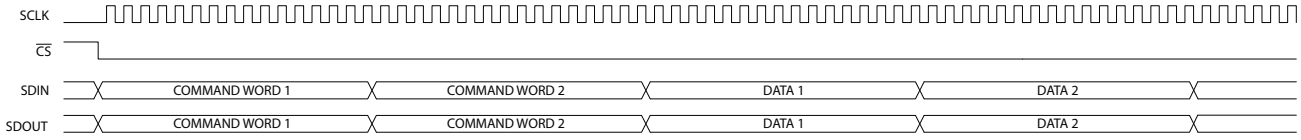


Figure 4-32: GSPI Write Timing—Auto-Increment with Loop-Through Operation (default)

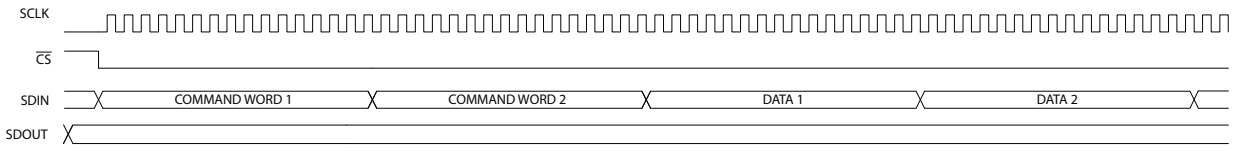


Figure 4-33: GSPI Write Timing—Auto-Increment with GSPI Link Disable Operation

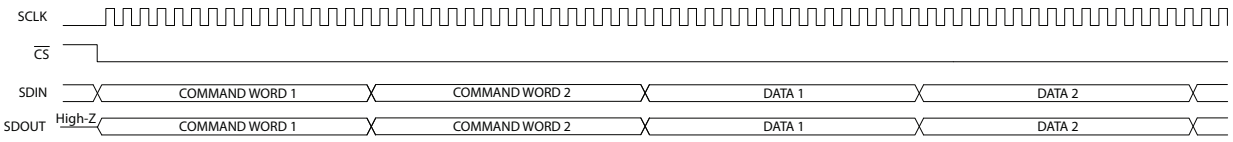


Figure 4-34: GSPI Write Timing—Auto-Increment with Bus-Through Operation

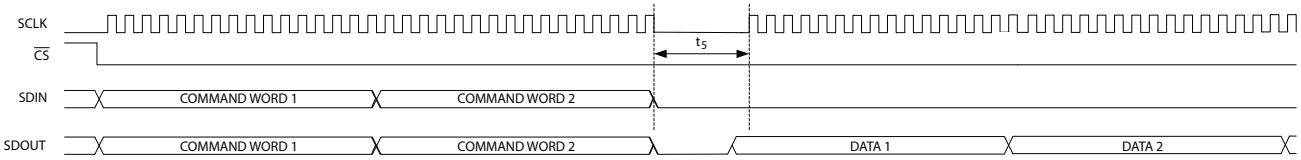


Figure 4-35: GSPI Read Timing—Auto-Increment Read with Loop-Through Operation (default)

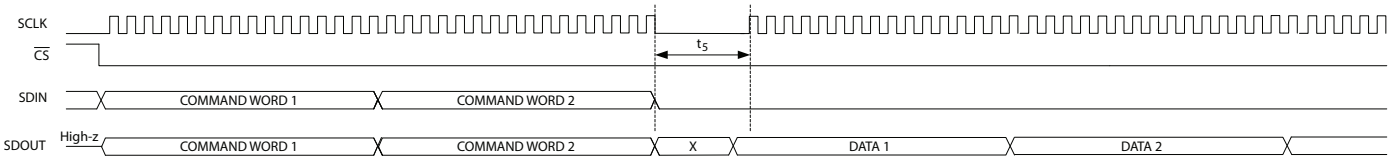


Figure 4-36: GSPI Read Timing—Auto-Increment Read with Bus-through Operation

4.10.9 Setting a Device Unit Address

Multiple (up to 32) GS3590 devices can be connected to a common Chip Select ($\overline{CS}$) in Loop-Through or Bus-Through operation.

To ensure that each device selected by a common $\overline{CS}$ can be separately addressed, a unique Unit Address must be programmed by the host processor at start-up as part of system initialization or following a device reset.

Note: By default at power-up or after a device reset, the **DEV_UNIT_ADDRESS** of each device is set to 0_h and the SDIN→SDOUT non-clocked loop-through for each device is enabled.

These are the steps required to set the **DEV_UNIT_ADDRESS** of devices in a chain to values other than 0:

1. Write to Unit Address 0 selecting **CONTROL_REG** (ADDRESS = 0), with the **GSPI_LINK_DISABLE** bit set to 1 and the **DEV_UNIT_ADDRESS** field set to 0. This disables the direct SDIN→SDOUT non-clocked path for all devices on chip select.
2. Write to Unit Address 0 selecting **CONTROL_REG** (ADDRESS = 0), with the **GSPI_LINK_DISABLE** bit set to 0 and the **DEV_UNIT_ADDRESS** field set to a unique Unit Address. This configures **DEV_UNIT_ADDRESS** for the first device in the chain. Each subsequent such write to Unit Address 0 will configure the next device in the chain. If there are 32 devices in a chain, the last (32nd) device in the chain must use **DEV_UNIT_ADDRESS** value 0.
3. Repeat step 2 using new, unique values for the **DEV_UNIT_ADDRESS** field in **CONTROL_REG** until all devices in the chain have been configured with their own unique Unit Address value.

Note: $t_{cmd_GSPI_conf}$ delay must be observed after every write that modifies **CONTROL_REG**.

All connected devices receive this command (by default the Unit Address of all devices is 0), and the Loop-Through operation will be re-established for all connected devices.

Once configured, each device will only respond to Command Words with a UNIT ADDRESS field matching the **DEV_UNIT_ADDRESS** in **CONTROL_REG**.

Note: Although the Loop-Through and Bus-Through configurations are compatible with previous generation GSPI enabled devices (backward compatibility), only devices supporting Unit Addressing can share a chip select. All devices on any single chip select must be connected in a contiguous chain with only the last device's SDOUT connected to the application host processor. Multiple chains configured in Bus-Through mode can have their final SDOUT outputs connected to a single application host processor input.

4.10.10 Default GSPI Operation

By default at power up or after a device reset, the GS3590 is set for Loop-Through Operation and the internal **DEV_UNIT_ADDRESS** field of the device is set to 0.

Figure 4-37 shows a functional block diagram of the Configuration and Status Register (CSR) map in the GS3590.

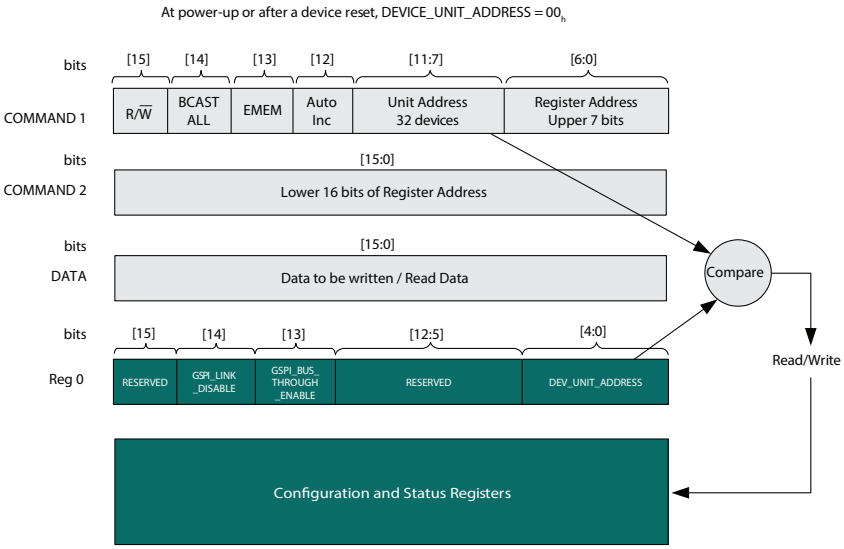


Figure 4-37: Internal Register Map Functional Block Diagram

The steps required for the application host processor to write to the Configuration and Status Registers via the GSPI, are as follows:

1. Set Command Word 1 for write access ($R/\overline{W} = 0$); set Auto Increment; set the Unit Address field in the Command Word 1 to match the configured **DEV_UNIT_ADDRESS** which will be zero after power-up. Set the Register Address bits in Command Word 1 to match the upper 7 bits of the register address to be accessed. Set the bits in Command Word 2 to match the lower 16 bits of the register address to be accessed. Write Command Word 1 and Command Word 2.
2. Write the Data Word to be written to the first register.

3. Write the Data Word to be written to the next register in Auto Increment mode, etc.

Read access is the same as the above with the exception of step 1, where the Command Word 1 is set for read access (R/$\overline{W}$ = 1).

Note: The UNIT ADDRESS field of Command Word 1 must always match **DEV_UNIT_ADDRESS** for an access to be accepted by the device. Changing **DEV_UNIT_ADDRESS** to a value other than 0 is only required if multiple devices are connected to a single chip select (in Loop-Through or Bus-Through configuration).

4.10.11 Clear Sticky Counts Through Four Way Handshake

There are four sticky counters that keep count of changes in status of primary and secondary carrier detect, rate changes, and lock changes. The counters can be read from the following four parameters in register 0x84 and 0x85: **STAT_CNT_PRI_CD_CHANGES, STAT_CNT_SEC_CD_CHANGES**, **STAT_CNT_RATE_CHANGES**, and **STAT_CNT_PLL_LOCK_CHANGES**. The counters saturate at 255 (0xFF) and must be cleared before additional status changes can be counted. The following four way handshake procedures clears the counters.

1. Poll **STAT_CLEAR_COUNTS_STATUS** parameter until equal to 0 (idle), then set **CTRL_CLEAR_COUNTS** = 1 (clear sticky counts).
2. Poll **STAT_CLEAR_COUNTS_STATUS** parameter until equal to 2 (cleared), then reset **CTRL_CLEAR_COUNTS** to 0.

The device will now reset **STAT_CLEAR_COUNTS_STATUS** to 0 (idle) and the clearing process can be repeated at any time.

4.10.12 Device Power-Up Sequence

If all power supplies cannot be guaranteed to power up simultaneously, ensure that *VCC_DDI* powers up first. Please note that there is no minimum time requirement between power supply initializations after *VCC_DDI* is energized.

Note: Please check with your local FAE (field applications engineer), as some devices may need updated configuration settings. If a configuration file has been provided by the FAE, see the timing information in the Serial Routing and Distribution Product Configuration Loading Procedure Application Note (PDS-061176).

4.10.12.1 Power-Up Timing Sequence

The following timing sequence must be observed after power-up when no external configuration loading is required. See Figure 4-38 for the timing requirements of Steps 1 and 2 below.

Step 1 – No GSPI Access Allowed

a) Device supply reaches 90% of target. POR (Power On Reset) is activated.

b) Internal blocks reset, default device configuration boot-up begins.

c) Default device configuration boot-up process.

Step 2 – GSPI Access Allowed

a) Host sets **EYE_MON_INT_CFG_3** (register address 0x57) to 0x8006.

b) If there are multiple devices on the GSPI chain, the host should configure the unit address of each device. See Section 4.10.9 for further information on unit addressing.

c) Host sets custom application specific settings.

d) Normal operation begins.

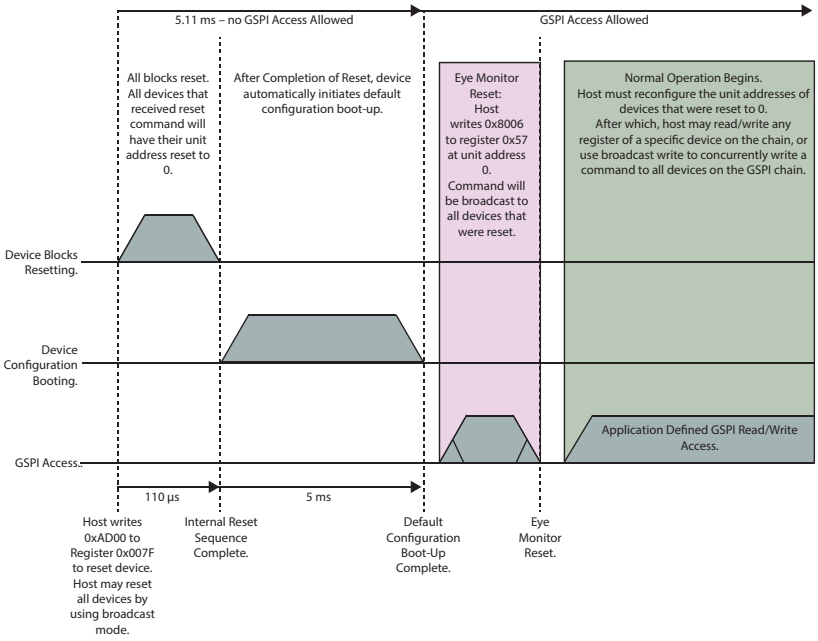


Figure 4-38: Power-Up Sequence.

4.10.13 Host Initiated Device Reset

The GS3590 includes a reset function accessible via the device's host interface, which reverts all internal logic and register values to their default values.

The device can be reset with a single write of $AD00_h$ to the **RESET_CONTROL** bits of the **CONTROL_RESET** register, which will assert and de-assert the device reset within the duration of the GSPI write access Data Word.

The device can be placed and held in reset by writing $AA00_h$ to the **RESET_CONTROL** bits of the **CONTROL_RESET** register. Subsequent writes of $DD00_h$ to the **RESET_CONTROL** bits will de-assert device reset.

The current state of user-initiated device reset can be read from the **RESET_CONTROL** bits of **CONTROL_RESET** register.

While in reset, host interface access to any other register will not be functional and all logic and configuration registers will be in reset state. While in reset, output behaviour is undefined. The digital logic and registers within the device will exit the reset state 5ms after device reset is de-asserted.

The following timing sequence must be observed to initiate a device reset.

Note: Please check with your local FAE (field applications engineer), as some devices may need updated configuration settings. If a configuration file has been provided by the FAE, see the timing information in the Serial Routing and Distribution Product Configuration Loading Procedure Application Note (PDS-061176).

4.10.13.1 Host Initiated Device Reset Timing Sequence

The following timing sequence must be observed after a Host Initiated Device Reset when no external configuration loading is required. See Figure 4-39 for the timing requirements of the Steps 1 to 3 below.

Step 1 – GSPI Access Allowed

a) Host writes 0xAD00 to register 0x007F to reset selected devices, or all devices using broadcast.

Step 2– No GSPI Access Allowed

a) Internal blocks reset, default device configuration boot-up begins.

b) Default device configuration boot-up completes.

Step 3 – GSPI Access Allowed

a) Host sets **EYE_MON_INT_CFG_3** (register address 0x57) to 0x8006.

b) If there are multiple devices on the GSPI chain, host must reconfigure unit address of each device that was reset. See Section 4.10.9 for further information on unit addressing.

c) Host sets custom application specific settings.

d) Normal operation begins.

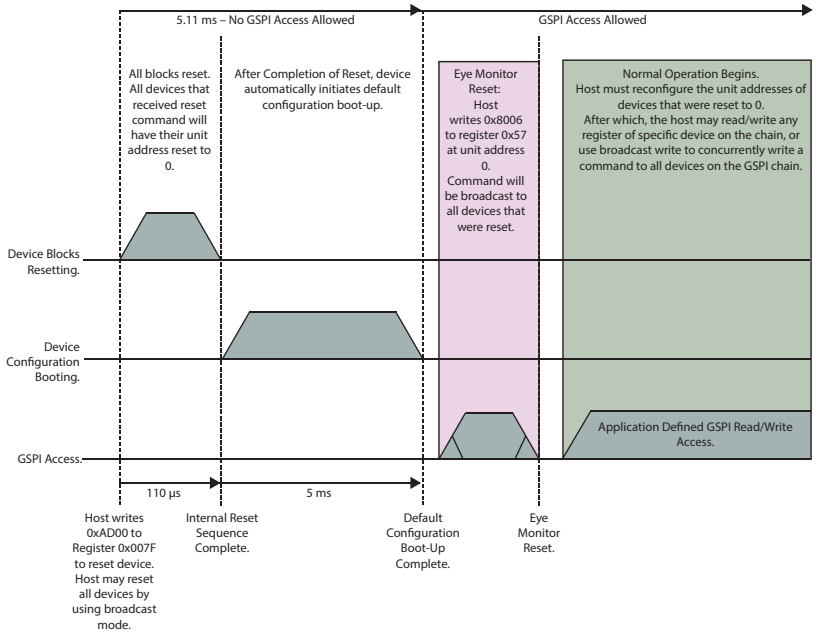


Figure 4-39: Host Initiated Device Reset Timing Sequence.

5. Register Map

The host interface on the GS3590 provides users complete control of key features such as GPIO configuration, PLL loop bandwidth settings, re-time parameters, carrier detection, cable equalization, bypass modes, output swing controls, mute functions, pre-emphasis control and many others.

It also includes a wide selection of Status Registers which allow the user to read back several key metrics of information from the GS3590 to add more flexibility to their designs.

Section 5.1 to Section 5.3 cover each Control and Status Register in detail.

5.1 Control Registers

Table 5-1: Control Registers

GSPI Address$_h$	Register Name	R/W
0	CONTROL_ REG	RW
1	DEVICE_ID	RO
2	RSVD	RW
7F	CONTROL_ RESET	RW
3	CONTROL_ SLEEP	RW
4	MISC_CNTRL	RW
5	MISC_CFG	RW
6	RATE_ DETECT_ MODE	RW
7	RATE_ DETECT_CFG	RW
CDR Configuration		
8	RSVD	RW
9	FACTORY_ CDR_ PARAMETERS	RW
0A	RSVD	RW
0B	PLL_LOOP_ BANDWIDTH_ 1	RW
0C	PLL_LOOP_ BANDWIDTH_ 2	RW
0D to 0F	RSVD	RW
GPIO Configuration		
10	GPIO0_CFG	RW
11	GPIO1_CFG	RW
12	GPIO2_CFG	RW

Table 5-1: Control Registers (Continued)

GSPI Address$_h$	Register Name	R/W
13	GPIO3_CFG	RW
Equalizer Configuration		
14	INPUT_ SELECT_CTRL	RW
15	CARR_ DET_CFG	RW
16	SQUELCH_ PARAMETERS	RW
17	CABLE_EQ_ BYPASS_ MODE	RW
18	INPUT_ LAUNCH_ SWING_CFG	RW
19 to 1D	RSVD	RW
1E	TREQ0_ INPUT_BOOST	RW
1F	TREQ0_CD_ HYSTERESIS	RW
20	CD_FILTER_ DELAYS_0	RW
21	CD_FILTER_ DELAYS_1	RW
22	CD_FILTER_ DELAYS_2	RW
23 to 25	RSVD	RW
Output Configuration		
26 to 27	RSVD	RW
28	OUTPUT_ PARAM_TD_ SD_0	RW
29	OUTPUT_ PARAM_ TD_SD_1	RW
2A	OUTPUT_ PARAM_CD_ SD_2	RW
2B	OUTPUT_ PARAM_CD_ SD_3	RW
2C	OUTPUT_ PARAM_ TD_HD_0	RW
2D	OUTPUT_ PARAM_ TD_HD_1	RW
2E	OUTPUT_ PARAM_ CD_HD_2	RW
2F	OUTPUT_ PARAM_ CD_HD_3	RW
30	OUTPUT_ PARAM_ TD_3G_0	RW
31	OUTPUT_ PARAM_ TD_3G_1	RW
32	OUTPUT_ PARAM_ CD_BYPASS_2	RW
33	OUTPUT_ PARAM_ CD_BYPASS_3	RW
34 to 37	RSVD	RW
38	OUTPUT_ PARAM_ TD_BYPASS_0	RW
39	OUTPUT_ PARAM_ TD_BYPASS_1	RW

Table 5-1: Control Registers (Continued)

GSPI Address$_h$	Register Name	R/W
3A to 40	RSVD	RW
41	OUTPUT_ PARAM_ MUTE_1	RW
42 to 47	RSVD	RW
Output Control		
48	OUTPUT_ SIG_SELECT	RW
49	CONTROL_ OUTPUT_ MUTE	RW
4A	CONTROL_ OUTPUT_ DISABLE	RW
4B	CONTROL_ OUTPUT_ SLEW	RW
4C	CONTROL_ RETIMER_ BYPASS	RW
4D	CONTROL_ BALANCED_ MODE	RW
4E to 4F	RSVD	RW
Test Functions		
50	PRBS_ CHK_CFG	RW
51	PRBS_CHK_ CTRL	RW
52	PRBS_GEN_ CTRL	RW
53	RSVD	RW
54	EYE_MON_ INT_CFG_0	RW
55	EYE_MON_ INT_CFG_1	RW
56	EYE_MON_ INT_CFG_2	RW
57	EYE_MON_ INT_CFG_3	RW
58 to 59	RSVD	RW
5A	EYE_MON_ SCAN_CTRL_0	RW
5B	EYE_MON_ SCAN_CTRL_1	RW
5C	EYE_MON_ SCAN_CTRL_2	RW
5D	EYE_MON_ SCAN_CTRL_3	RW
5E to 5F	RSVD	RW
Internal Only Configuration (Do not write to these registers)		
60 to 7E	RSVD	—

5.2 Status Registers

Table 5-2: Status Registers

GSPI Address$_h$	Register Name	R/W
80	RSVD	RW
81	VERSION_0	RO
82	VERSION_1	RO
83	VERSION_2	RO
84	STICKY_ COUNTS_0	RO
85	STICKY_ COUNTS_1	RO
86	CURRENT_ STATUS_0	RO
87	CURRENT_ STATUS_1	RO
88	EQ_GAIN_IND	RO
89	PRBS_ CHK_ERR_CNT	RO
8A	PRBS_ CHK_STATUS	RO
8B	EYE_MON_ SCAN_ SIZE_OUTPUT	RO
8C	EYE_MON_ SHAPE_ OUTPUT_0	RO
8D	EYE_MON_ SHAPE_ OUTPUT_1	RO
8E	EYE_MON_ SHAPE_ OUTPUT_2	RO
8F	EYE_MON_ SHAPE_ OUTPUT_3	RO
90	EYE_MON_ STATUS	RO
91 to BF	RSVD	RW

5.3 Register Descriptions

5.3.1 Control Register Descriptions

Table 5-3: Control Register Descriptions

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
0	CONTROL_ REG	RSVD	15	RW	0	Reserved — do not modify.
		GSPI_LINK_DISABLE	14	RW	0	0 = Enable loop-through. SDIN pin is looped through to the SDOUT pin 1 = Disable loop-through. Data appearing at SDIN does not appear at SDOUT, and SDOUT pin is HIGH
		GSPI_BUS_THROUGH_ ENABLE	13	RW	0	0 = Disable bus-through mode 1 = Enable bus-through mode
		RSVD	12:5	RW	0	Reserved — do not modify.
		DEV_UNIT_ADDRESS	4:0	RW	0	Device address programmed by application. See Section 4.10.9 for further information.
1	DEVICE_ID	DEVICE_VERSION	15:0	RO	—	This register contains the device's identification, including revision. Contact the local technical sales representative for details.
2	RSVD	RSVD	15:0	R/W	0	Reserved— do not modify.
7F	CONTROL_ RESET	RESET_CONTROL	15:0	R/W	DD00	Device Reset, Reverts all internal logic and register values to defaults. Write Values: $AA00_h$ = Asserts device reset $DD00_h$ = De-assert device reset $AD00_h$ = Assert/de-assert device reset in a single write Read Values: $AA00_h$ = User-initiated reset is asserted $DD00_h$ = User-initiated reset is de-asserted See Section 4.10.13 for further information.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
3	CONTROL_SLEEP	RSVD	15:2	R/W	0	Reserved—do not modify.
		CTRL_MANUAL_SLEEP	1	R/W	0	Sleep manual mode control: 0 = Never Sleep 1 = Always Sleep Controls sleep mode when auto sleep (CTRL_AUTO_SLEEP) is disabled.
		CTRL_AUTO_SLEEP	0	R/W	1	Sleep auto mode control: 0 = Disable auto sleep mode 1 = Enable auto sleep mode If CTRL_AUTO_SLEEP = 0 (manual sleep mode), then CTRL_MANUAL_SLEEP controls sleep. If CTRL_AUTO_SLEEP = 1 (auto sleep mode), sleep is automatically entered on loss of signal.
4	MISC_CNTRL	RSVD	15:1	R/W	0	Reserved—do not modify.
		CTRL_CLEAR_COUNTS	0	R/W	0	Clear sticky counts control register. 0 = no action 1 = clear sticky counts. Part of a four way handshake with STAT_CLEAR_COUNTS_STATUS. See Section 4.10.11 for more details on implementing the four way handshake for this operation.
5	MISC_CFG	RSVD	15:5	R/W	0	Reserved—do not modify.
		CFG_TRDR_MUTE_WHEN_CABLE_DRIVER	4	R/W	0	Controls whether Trace Driver (DDO) is muted or disabled when GS3590 bi-directional part is in Cable Driver Mode and CTRL_LOOPBACK_ENA = 0: 0 = Disable (power-down) 1 = Mute
		CFG_SLEEP_OUTPUT1_MUTE	3	R/W	0	Controls whether Trace Driver (DDO) is muted or disabled (powered-down) during sleep: 0 = Disable (power-down) output during sleep 1 = mute output during sleep
		RSVD	2:0	R/W	1	Reserved—do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
6	RATE_ DETECT_ MODE	RSVD	15:12	R/W	3	Reserved—do not modify.
		CFG_RATE_ENA_3G	11	R/W	1	3G auto rate detection enable: 0 = Disable rate 1 = Enable rate **Note**: This parameter is only applicable to the trace equalizer input (DDI).
		CFG_RATE_ENA_HD	10	R/W	1	HD auto rate detection enable: 0 = Disable rate 1 = Enable rate **Note**: This parameter is only applicable to the trace equalizer input (DDI).
		CFG_RATE_ENA_SD	9	R/W	1	SD auto rate detection enable: 0 = Disable rate 1 = Enable rate **Note**: This parameter is only applicable to the trace equalizer input (DDI).
		CFG_RATE_ENA_MADI	8	R/W	0	MADI auto rate detection enable: 0 = Disable rate 1 = Enable rate **Note**: This parameter is only applicable to the trace equalizer input (DDI).
		RSVD	7:5	R/W	0	Reserved—do not modify.
		CFG_MANUAL_RATE	4:1	R/W	0	Manual rate selection. The CDR will only lock to the selected rate if CFG_AUTO_RATE_DETECT_ENA = 0: 0 = < MADI (only applicable in Cable Equalizer Mode) 1 = MADI 2 = SD 3 = HD 4 = 3G 5 = Reserved—do not modify 6 = Reserved—do not modify 7 = Reserved—do not modify
		CFG_AUTO_RATE_ DETECT_ENA	0	R/W	1	Set or disable auto rate detection mode. 0 = Disable auto rate detection 1 = Enable auto rate detection When automatic rate detection is disabled, the rate is set by CFG_MANUAL_RATE. **Note**: If using manual rate selection while in cable driver mode, the host should set CFG_MANUAL_RATE to 1 through 7 first, then set CFG_AUTO_RATE_ENA = 0.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
7	RATE_ DETECT_CFG	RSVD	15:5	R/W	0	Reserved—do not modify.
		CFG_RD_SD_MADI_ THRESHOLD	4	R/W	0	Select data rate threshold between SD and MADI: 0 = 181Mb/s 1 = 198Mb/s **Note**: This parameter is only applicable to the cable equalizer input (SDIO).
		CFG_RD_MADI_ LTMADI_DATADIV	3:2	R/W	0	CFG_RD_SD_MADI_THRESHOLD and CFG_RD_MADI_LTMADI_DATADIV (bit slice [3:0]) determines the rate detection threshold between MADI and <MADI rates. The following threshold settings are available: 0x0 = 53Mb/s 0x2 = 32Mb/s 0x3 = 79Mb/s (default) 0x6 = 63Mb/s 0x9 = 48Mb/s 0xA = 95Mb/s 0xC = 111Mb/s 0x1, 0x4, 0x5, 0x7, 0x8, 0xB, 0xD, and 0xE = Reserved—do not use **Note**: This parameter is only applicable to the cable equalizer input (SDIO).
		CFG_RD_MADI_ LTMADI_CLKDIV	1:0	R/W	3	See CFG_RD_MADI_ LTMADI_DATADIV. **Note**: This parameter is only applicable to the cable equalizer input (SDIO).
CDR Configuration						
8	RSVD	RSVD	15:0	R/W	3	Reserved—do not modify.
9	FACTORY_ CDR_ PARAMETERS	RSVD	15:2	R/W	1C	Reserved—do not modify.
		CFG_MIN_LBW	1	R/W	1	To maximize loop bandwidth of PLL and consequently IJT of CDR, set this parameter to 0.
		RSVD	0	R/W	0	Reserved—do not modify.
0A		RSVD	15:0	R/W	808	Reserved—do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
0B	PLL_LOOP_BANDWIDTH_1	RSVD	15:13	R/W	0	Reserved—do not modify.
		CFG_PLL_LBW_3G	12:8	R/W	8	Configure 2.97Gb/s (3G) PLL loop bandwidth in terms of ratio to nominal loop bandwidth 'x' (see Table 2-3). 2.97Gb/s (3G) loop bandwidth setting: 0x00 = Reserved—do not use 0x01 = 0.0625x 0x02 = 0.125x 0x03 = 0.1875x 0x04 = 0.25x 0x05 = 0.3125x 0x06 = 0.375x 0x07 = 0.4375x 0x08 = 0.5x 0x09 = 0.5625x 0x0A = 0.625x 0x0B = 0.6875x 0x0C = 0.75x 0x0D = 0.8125x 0x0E = 0.875x 0x0F = 0.9375x 0x10 to 0x1B = Reserved - do not use 0x1C = 1.0x (nominal) 0x1D = 1.0625x 0x1E = 1.125x 0x1F = 1.1875x
		RSVD	7:5	R/W	0	Reserved—do not modify.
		CFG_PLL_LBW_HD	4:0	R/W	8	Configure 1.485Gb/s (HD) PLL loop bandwidth in terms of ratio to nominal loop bandwidth 'x' (see Table 2-3). See CFG_PLL_LBW_3G parameter for available settings.
0C	PLL_LOOP_BANDWIDTH_2	RSVD	15:13	R/W	0	Reserved—do not modify.
		CFG_PLL_LBW_SD	12:8	R/W	1C	Configure 270Mb/s (SD) PLL loop bandwidth in terms of ratio to nominal loop bandwidth 'x' (see Table 2-3). See CFG_PLL_LBW_3G parameter for available settings.
		RSVD	7:5	R/W	0	Reserved—do not modify.
		CFG_PLL_LBW_MADI	4:0	R/W	8	Configure 125Mb/s (MADI) PLL loop bandwidth in terms of ratio to nominal loop bandwidth 'x' (see Table 2-3). See CFG_PLL_LBW_3G parameter for available settings.
0D to 0F	RSVD	RSVD	15:0	R/W	0	Reserved—do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
GPIO Configuration						
10	GPIO0_CFG	RSVD	15:9	R/W	0	Reserved—do not modify.
		CFG_GPIO0_ OUTPUT_ENA	8	R/W	1	GPIO0 buffer mode control. 0 = GPIO pin is configured as an input (tri-stated / high impedance) 1 = GPIO pin is configured as an output

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
10 (Continued)	GPIO0_CFG (Continued)	CFG_GPIO0_FUNCTION	7:0	R/W	80	Function select for GPIO0 pin. **GPIO0 output functions**: 0x00 = Output driven LOW 0x01 = Output driven HIGH 0x02 = PLL lock status (HIGH—PLL locked) 0x03 to 0x7F = Reserved—do not use 0x80 = LOS—equivalent to inverse of STAT_PRI_CD for trace equalizer input (DDI) and STAT_SEC_CD for cable equalizer input (SDIO) 0x81 = Carrier detect status of the selected input (STAT_PRI_CD for trace equalizer input (DDI) and STAT_SEC_CD for cable equalizer input (SDIO)) 0x82 = Sleep mode status (HIGH— Device in sleep mode) 0x83 = HIGH for SD, LOW for all other rates 0x84 = Rate detected [0] 0x85 = Rate detected [1] 0x86 = Rate detected [2] **Note:** To have full rate range using the GPIO rate detect function, one GPIO pin must be used for each Rate Detect bit [2:0]. Please see Table 4-3: Detected Data Rates for the indication values. 0x87 to 0xFF = Reserved—do not use **GPIO0 input functions**: 0x00 to 0x80 = Reserved—do not use 0x81 = SDIO disable control (HIGH—disable) 0x82 = DDO disable control (HIGH— disable) 0x83 = Reserved—do not modify 0x84 = Cable equalizer bypass enable (HIGH — Bypass enabled), Cable equalizer input (SDIO) only. 0x85 = Retimer bypass enable (HIGH—Bypass enabled) 0x86 = Sleep control (HIGH—Sleep) 0x87 = Cable Driver / Equalizer mode selection (HIGH = Cable Driver Mode, DDI as input / LOW = Cable Equalizer Mode, SDIO as input). 0x88 to 0xFF = Reserved—do not use

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
11	GPIO1_CFG	RSVD	15:9	R/W	0	Reserved—do not modify.
		CFG_GPIO1_OUTPUT_ENA	8	R/W	1	GPIO1 buffer mode control. See GPIO0_CFG: CFG_GPIO0_OUTPUT_ENA parameter for description and available settings. Default mode: Output
		CFG_GPIO1_FUNCTION	7:0	R/W	2	Function select for GPIO1 pin. See GPIO0_CFG: CFG_GPIO0_FUNCTION parameter for description and available settings. Default Function: 0x02 = PLL lock status
12	GPIO2_CFG	RSVD	15:9	R/W	0	Reserved—do not modify.
		CFG_GPIO2_OUTPUT_ENA	8	R/W	0	GPIO2 buffer mode control. See GPIO0_CFG: CFG_GPIO0_OUTPUT_ENA parameter for description and available settings. Default mode: Input
		CFG_GPIO2_FUNCTION	7:0	R/W	86	Function select for GPIO2 pin. See GPIO0_CFG: CFG_GPIO0_FUNCTION parameter for description and available settings. Default Function: 0x86 = Sleep control
13	GPIO3_CFG	RSVD	15:9	R/W	0	Reserved—do not modify.
		CFG_GPIO3_OUTPUT_ENA	8	R/W	0	GPIO3 buffer mode control. See GPIO0_CFG: CFG_GPIO0_OUTPUT_ENA parameter for description and available settings. Default mode: Input
		CFG_GPIO3_FUNCTION	7:0	R/W	87	Function select for GPIO3 pin. See GPIO0_CFG: CFG_GPIO0_FUNCTION parameter for description and available settings. Default Function: 0x87 = Cable Equalizer/Driver mode selection

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
Equalizer Configuration						
14	INPUT_ SELECT_CTRL	RSVD	15:11	R/W	0	Reserved—do not modify.
		CTRL_LOOPBACK_ENA	10	R/W	0	Enables trace input (DDI) to trace output (DDO) loopback mode when in cable driver mode. 0 = Loopback is disabled. The Trace Driver is controlled by CFG_TRDR_ MUTE_WHEN_CABLE_DRIVER. 1 = Loopback is enabled. (subject to output state control modes, see Section 4.8.6) **Note**: This parameter is only applicable to the trace equalizer input (DDI).
		RSVD	9:3	R/W	60	Reserved—do not modify.
		CTRL_DIRECTION_ SEL_MODE	2:1	R/W	0	Select bi-directional control method. 0 = pin mode (default mode) 1 = Host Interface Mode 2 = Reserved—do not select 3 = Reserved—do not select The host should configure one of the GPIO pins for input select before selecting mode 0.
		CTRL_DIRECTION_SEL	0	R/W	1	Selects bidirectional mode when CTRL_DIRECTION_SEL_MODE = 1 (Host Interface mode). 0 = Cable Equalizer Mode 1 = Cable Driver Mode
15	CARR_ DET_CFG	RSVD	15:1	R/W	0	Reserved—do not modify.
		CFG_SEC_CD_INCL_ CLI_SQUELCH	0	R/W	0	Enable or disable squelch control conditions for deriving secondary carrier detection (LOS) status for Cable Equalizer mode. 0 = Ignore CLI squelch 1 = Take into account CLI squelch **Note**: This parameter is only applicable to the cable equalizer input (SDIO).

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
16	SQUELCH_ PARAMETERS	RSVD	15	R/W	0	Reserved—do not modify.
		CFG_CLI_SQUELCH_ THRESHOLD	14:8	R/W	40	Set the input signal squelch threshold. Range = 0 to 64_d (64_d is max cable reach determined for specific rate, cable type, and launch swing compensation). **Note**: This parameter is only applicable to the cable equalizer input (SDIO).
		RSVD	7	R/W	0	Reserved—do not modify.
		CFG_CLI_SQUELCH_ HYSTERESIS	6:0	R/W	2	Set the input signal squelch hysteresis. Range = 1_d to 30_d **Note**: This parameter is only applicable to the cable equalizer input (SDIO).
17	CABLE_EQ_ BYPASS_ MODE	RSVD	15:2	R/W	0	Reserved—do not modify.
		CTRL_CEQ_MANUAL_ BYPASS	1	R/W	0	Controls Cable Equalizer bypass when auto cable equalizer bypass is disabled (CTRL_CEQ_AUTO_BYPASS= 0). 0 = Cable Equalizer never bypassed 1 = Cable Equalizer always bypassed **Note**: This parameter is only applicable to the cable equalizer input (SDIO).
		CTRL_CEQ_AUTO_ BYPASS	0	R/W	1	Auto Cable Equalizer bypass mode control: 0 = Disable auto mode 1 = Enable auto mode When CFG_CEQ_AUTO_BYPASS = 0, CEQ bypass is controlled by CFG_CEQ_BYPASS_MANUAL. **Note**: This parameter is only applicable to the cable equalizer input (SDIO).
18	INPUT_ LAUNCH_ SWING_CFG	RSVD	15:7	R/W	0	Reserved—do not modify.
		CFG_CEQ_INPUT_ LAUNCH_SWING_ COMP	6:0	R/W	50	Input launch swing compensation setting in units of 10 mV_{ppd} Default setting of 80_d (0x50) corresponds to 800mV. Default for upstream SMPTE compliant cable drivers operating at 800mv ±10%. **Note**: This parameter is only applicable to the cable equalizer input (SDIO).

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
19	RSVD	RSVD	15:0	R/W	1	Reserved—do not modify.
1A	RSVD	RSVD	15:0	R/W	0	Reserved—do not modify.
1B	RSVD	RSVD	15:0	R/W	1	Reserved—do not modify.
1C to 1D	RSVD	RSVD	15:0	R/W	0	Reserved—do not modify.
1E	TREQ0_ INPUT_BOOST	RSVD	15:5	R/W	0	Reserved—do not modify.
		CFG_TREQ0_BOOST	4:1	R/W	0	Trace Equalizer input boost setting: 0 = Bypass equalization stage 1 to 8 = 1 to 17dB of insertion loss at 1.485GHz (see Figure 4-2) Bypass is the minimum boost setting; boost 8 is maximum boost setting. **Note**: This parameter is only applicable to the trace equalizer input (DDI).
		CFG_TREQ0_CD_ BOOST	0	R/W	0	Selects boost level applied to trace equalizer input signal for carrier detection function only. 0 = Sets to boost 8 (See Figure 4-2) 1 = Use CFG_TREQ0_BOOST setting **Note**: This parameter is only applicable to the trace equalizer input (DDI).
1F	TREQ0_CD_ HYSTERESIS	RSVD	15:8	R/W	0	Reserved—do not modify.
		CFG_TREQ0_CD_ ASSERT_THRESH	7:4	R/W	4	Sets assert threshold for trace equalizer input carrier detect. 0 to15$_d$, where 0 is minimum threshold and 15$_d$ is maximum threshold (see Figure 4-3). **Note**: This parameter is only applicable to the trace equalizer input (DDI).
		CFG_TREQ0_CD_DEAS SERT_THRESH	3:0	R/W	3	Sets de-assert threshold for Trace Equalizer input carrier detect 0 to15$_d$, where 0 is minimum threshold and 15$_d$ is maximum threshold (see Figure 4-3). **Note**: This parameter is only applicable to the trace equalizer input (DDI).

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
20	CD_FILTER_DELAYS_0	RSVD	15:8	R/W	0	Reserved—do not modify.
		CFG_CD_FILTER_SAMPLE_WIN	7:0	R/W	3	Cable Equalizer input carrier detect filter sample window period in clock cycles. Sample window size is this value plus 1 clock cycle. Valid Range = 0x03 to 0xFF See Section 4.2.3 for details. **Note**: This parameter is only applicable to the cable equalizer input (SDIO).
21	CD_FILTER_DELAYS_1	RSVD	15:10	R/W	0	Reserved—do not modify.
		CFG_CD_FILTER_DEASSERT_CNT	9:0	R/W	F	Number of samples for detecting cable equalizer carrier detection de-assertion: Valid Range = 0x00 to 0x3FF See Section 4.2.3 for details. **Note**: This parameter is only applicable to the cable equalizer input (SDIO).
22	CD_FILTER_DELAYS_2	RSVD	15:10	R/W	0	Reserved—do not modify.
		CFG_CD_FILTER_ASSERT_CNT	9:0	R/W	3FF	Number of samples for detecting cable equalizer carrier detection assertion: Valid Range = 0x00 to 0x3FF See Section 4.2.3 for details. **Note**: This parameter is only applicable to the cable equalizer input (SDIO).
23 to 25	RSVD	RSVD	15:0	R/W	0	Reserved—do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
Output Configuration						
26 to 27	RSVD	RSVD	15:0	R/W	0	Reserved—do not modify.
28	OUTPUT_PARAM_TD_SD_0	RSVD	15:13	R/W	0	Reserved—do not modify.
		CFG_OUTPUT1_TD_SD_PREEMPH_WIDTH	12:8	R/W	2	Configure the Trace Driver output (DDO) SD pre-emphasis pulse width. Range: 0 to 15_d. Adjust the pre-emphasis pulse width to better match the channel loss response shape. **Note:** By default, the Trace Driver SD settings are applied for all rates (see CTRL_OUTPUT1_TRDR_PER_RATE for per rate setting).
		RSVD	7	R/W	0	Reserved—do not modify.
		CFG_OUTPUT1_TD_SD_PREEMPH_PWRDWN	6	R/W	0	Trace Driver output (DDO) SD Pre-Emphasis Power Down DDO power down control for pre-emphasis driver. 0 = Pre-emphasis driver powered up (pre-emphasis enabled) 1 = Pre-emphasis driver powered down (pre-emphasis disabled) **Note:** By default, the Trace Driver SD settings are applied for all rates (see CTRL_OUTPUT1_TRDR_PER_RATE for per rate setting).
		CFG_OUTPUT1_TD_SD_PREEMPH_AMPL	5:0	R/W	1	Configure the Trace Driver output (DDO) SD pre-emphasis pulse amplitude. Range = 0_d to 50_d Adjust the pre-emphasis pulse amplitude to better match the channel loss at Nyquist. **Note:** By default, the Trace Driver SD settings are applied for all rates (see CTRL_OUTPUT1_TRDR_PER_RATE for per rate setting).

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
29	OUTPUT_ PARAM_ TD_SD_1	RSVD	15:14	R/W	0	Reserved—do not modify.
		CFG_OUTPUT1_TD_ SD_DRIVER_SWING	13:8	R/W	11	Configure the trace driver output (DDO) SD amplitude. Range: 0 to 40_d. Adjust the differential Trace Driver amplitude. The default value produces an amplitude of 400mV_{ppd} **Note:** By default, the Trace Driver SD settings are applied for all rates (see CTRL_OUTPUT1_TRDR_PER_RATE for per rate setting).
		RSVD	7:0	R/W	70	Reserved—do not modify.
2A	OUTPUT_ PARAM_CD_ SD_2	RSVD	15:13	R/W	0	Reserved—do not modify.
		CFG_OUTPUT0_CD_ SD_PREEMPH_ WIDTH	12:8	R/W	3	Configures the MADI/SD rate pre-emphasis pulse width on Cable Driver output (SDIO): Range = 0_d to 15_d Adjust the pre-emphasis pulse width to better match the channel loss response shape.
		RSVD	7	R/W	0	Reserved—do not modify.
		CFG_OUTPUT0_CD_ SD_PREEMPH_ PWRDWN	6	R/W	1	Power-down the MADI/SD rate pre-emphasis on Cable Driver output (SDIO): 0 = Pre-emphasis driver powered-up (pre-emphasis enabled) 1 = Pre-emphasis driver powered-down (pre-emphasis disabled).
		CFG_OUTPUT0_CD_ SD_PREEMPH_AMPL	5:0	R/W	0	Configures the MADI/SD rate pre-emphasis amplitude on Cable Driver output (SDIO): Range = 0_d to 15_d Adjust the pre-emphasis pulse amplitude to better match the channel loss at Nyquist.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
2B	OUTPUT_PARAM_CD_SD_3	RSVD	15:14	R/W	0	Reserved—do not modify.
		CFG_OUTPUT0_CD_SD_DRIVER_SWING	13:8	R/W	18	Configure the Cable Driver output (SDIO) SD/MADI amplitude in ~25mV$_{pp}$ steps: Functional Range = 9_d to 31_d Precision Range = 21_d to 27_d Default value = 24_d (~800mV$_{pp}$) **Note:** In auto slew mode (CTRL_OUTPUT0_AUTO_SLEW=1), the slew rate is determined by the rate at which the CDR is locked. If the CDR is unlocked, the slew will default to Bypass Slew. See Table 2-3 for Rise/Fall Times, and Section 4.8.3 for more details on output driver selection.
		RSVD	7:0	R/W	A0	Reserved—do not modify.
2C	OUTPUT_PARAM_TD_HD_0	RSVD	15:13	R/W	0	Reserved—do not modify.
		CFG_OUTPUT1_TD_HD_PREEMPH_WIDTH	12:8	R/W	2	Configure the Trace Driver output (DDO) HD pre-emphasis pulse width. Range = 0_d to 15_d Adjust the pre-emphasis pulse width to better match the channel loss response shape.
		RSVD	7	R/W	0	Reserved—do not modify.
		CFG_OUTPUT1_TD_HD_PREEMPH_PWRDWN	6	R/W	0	Trace Driver output (DDO) HD pre-emphasis power-down Power-down control for pre-emphasis driver. 0 = Pre-emphasis driver powered-up (pre-emphasis enabled) 1 = Pre-emphasis driver powered-down (pre-emphasis disabled)
		CFG_OUTPUT1_TD_HD_PREEMPH_AMPL	5:0	R/W	1	Configure the Trace Driver output (DDO) HD pre-emphasis pulse amplitude. Range = 0_d to 50_d Adjust the pre-emphasis pulse amplitude to better match the channel loss at Nyquist.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
2D	OUTPUT_PARAM_TD_HD_1	RSVD	15:14	R/W	0	Reserved—do not modify.
		CFG_OUTPUT1_TD_HD_DRIVER_SWING	13:8	R/W	11	Configure the Trace Driver output (DDO) HD amplitude. Range = 0_d to 40_d Adjust the differential trace driver amplitude. The default value produces an amplitude of 400mV$_{ppd}$.
		RSVD	7:0	R/W	70	Reserved—do not modify.
2E	OUTPUT_PARAM_CD_HD_2	RSVD	15:13	R/W	0	Reserved—do not modify.
		CFG_OUTPUT0_CD_HD_PREEMPH_WIDTH	12:8	R/W	9	Configure the Cable Driver output (SDIO) HD/3G pre-emphasis pulse width. Range = 0_d to 15_d. Adjust the pre-emphasis pulse width to better match the channel loss response shape.
		RSVD	7	R/W	0	Reserved—do not modify.
		CFG_OUTPUT0_CD_HD_PREEMPH_PWRDWN	6	R/W	0	Cable Driver output (SDIO) HD/3G pre-emphasis power-down. SDIO power-down control for pre-emphasis driver. 0 = Pre-emphasis driver powered-up (pre-emphasis enabled) 1 = Pre-emphasis driver powered-down (pre-emphasis disabled)
		CFG_OUTPUT0_CD_HD_PREEMPH_AMPL	5:0	R/W	7	Configure the Cable Driver output (SDIO) HD/3G pre-emphasis pulse amplitude. Range = 0_d to 15_d Adjust the pre-emphasis pulse amplitude to better match the channel loss at Nyquist.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
2F	OUTPUT_ PARAM_ CD_HD_3	RSVD	15:14	R/W	0	Reserved—do not modify.
		CFG_OUTPUT0_CD_ HD_DRIVER_SWING	13:8	R/W	17	Configure the Cable Driver output (SDIO) HD/3G amplitude in ~20mV$_{pp}$ steps. Functional Range = 9_d to 31_d Precision Range = 20_d to 26_d Default value = 23_d (~800mV$_{pp}$) **Note:** In auto slew mode (CTRL_OUTPUT0_AUTO_SLEW=1), the slew rate is determined by the rate at which the CDR is locked. If the CDR is unlocked, the slew will default to Bypass Slew. See Table 2-3 for Rise/Fall Times, and Section 4.8.3 for more details on output driver selection.
		RSVD	7:0	R/W	80	Reserved—do not modify.
30	OUTPUT_ PARAM_ TD_3G_0	RSVD	15:13	R/W	0	Reserved—do not modify.
		CFG_OUTPUT1_TD_ 3G_PREEMPH_WIDTH	12:8	R/W	2	Configure the Trace Driver output (DDO) 3G pre-emphasis pulse width. Range = 0_d to 15_d Adjust the pre-emphasis pulse width to better match the channel loss response shape.
		RSVD	7	R/W	0	Reserved—do not modify.
		CFG_OUTPUT1_TD_ 3G_PREEMPH_ PWRDWN	6	R/W	0	Trace Driver output (DDO) 3G pre-emphasis power down DDO power-down control for pre-emphasis driver. 0 = Pre-emphasis driver powered-up (pre-emphasis enabled) 1 = Pre-emphasis driver powered-down (pre-emphasis disabled)
		CFG_OUTPUT1_TD_ 3G_PREEMPH_AMPL	5:0	R/W	1	Configure the trace driver output (DDO) 3G pre-emphasis pulse amplitude. Range = 0_d to 50_d Adjust the pre-emphasis pulse amplitude to better match the channel loss at Nyquist.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
31	OUTPUT_ PARAM_ TD_3G_1	RSVD	15:14	R/W	0	Reserved—do not modify.
		CFG_OUTPUT1_TD_ 3G_DRIVER_SWING	13:8	R/W	11	Configure the Trace Driver output (DDO) 3G amplitude. Range = 0_d to 40_d Adjust the differential Trace Driver amplitude. The default value produces an amplitude of 400mV_{ppd}.
		RSVD	7:0	R/W	70	Reserved—do not modify.
32	OUTPUT_ PARAM_ CD_BYPASS_2	RSVD	15:13	R/W	0	Reserved—do not modify.
		CFG_OUTPUT0_CD_ BYPASS_PREEMPH_ WIDTH	12:8	R/W	7	Configure the Cable Driver output (SDIO) Bypass pre-emphasis pulse width. Range = 0_d to 15_d Adjust the pre-emphasis pulse width to better match the channel loss response shape. **Note**: In auto slew mode (CTRL_ OUTPUT0_AUTO_SLEW = 1), the slew rate is determined by the rate at which the CDR is locked. If the CDR is unlocked, the slew will default to Bypass Slew. See Table 2-3 for Rise/Fall times, and Section 4.8.3 for more details on output driver selection.
		RSVD	7	R/W	0	Reserved—do not modify.
		CFG_OUTPUT0_CD_ BYPASS_PREEMPH_ PWRDWN	6	R/W	0	Cable Driver output (SDIO) Bypass pre-emphasis power-down SDIO power-down control for pre-emphasis driver. 0 = Pre-emphasis driver powered-up (pre-emphasis enabled) 1 = Pre-emphasis driver powered-down (pre-emphasis disabled) **Note**: In auto slew mode (CTRL_ OUTPUT0_AUTO_SLEW = 1), the slew rate is determined by the rate at which the CDR is locked. If the CDR is unlocked, the slew will default to Bypass Slew. See Table 2-3 for Rise/Fall times, and Section 4.8.3 for more details on output driver selection.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
32 (Continued)	OUTPUT_ PARAM_ CD_BYPASS_2 (Continued)	CFG_OUTPUT0_CD_ BYPASS_PREEMPH_ AMPL	5:0	R/W	B	Configure the Cable Driver output (SDIO) Bypass pre-emphasis pulse amplitude. Range = 0_d to 50_d Adjust the pre-emphasis pulse amplitude to better match the channel loss at Nyquist. **Note**: In auto slew mode (CTRL_ OUTPUT0_AUTO_SLEW = 1), the slew rate is determined by the rate at which the CDR is locked. If the CDR is unlocked, the slew will default to Bypass Slew. See Table 2-3 for Rise/Fall times, and Section 4.8.3 for more details on output driver selection.
33	OUTPUT_ PARAM_ CD_BYPASS_3	RSVD	15:14	R/W	0	Reserved—do not modify.
		CFG_OUTPUT0_CD_ BYPASS_DRIVER_ SWING	13:8	R/W	18	Configure the Cable Driver output (SDIO) Bypass amplitude in ~15mV$_{pp}$ steps. Functional Range = 9_d to 31_d Default value = 24_d (~800mV$_{pp}$) **Note**: In auto slew mode (CTRL_ OUTPUT0_AUTO_SLEW = 1), the slew rate is determined by the rate at which the CDR is locked. If the CDR is unlocked, the slew will default to Bypass Slew. See Table 2-3 for Rise/Fall times, and Section 4.8.3 for more details on output driver selection.
		RSVD	7:0	R/W	60	Reserved—do not modify.
34	RSVD	RSVD	15:0	R/W	201	Reserved—do not modify.
35	RSVD	RSVD	15:0	R/W	1170	Reserved—do not modify.
36	RSVD	RSVD	15:0	R/W	201	Reserved—do not modify.
37	RSVD	RSVD	15:0	R/W	1170	Reserved—do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
38	OUTPUT_PARAM_TD_BYPASS_0	RSVD	15:13	R/W	0	Reserved—do not modify.
		CFG_OUTPUT1_TD_BYPASS_PREEMPH_WIDTH	12:8	R/W	2	Configure the Trace Driver output (DDO) Bypass pre-emphasis pulse width. Range = 0_d to 15_d Adjust the pre-emphasis pulse width to better match the channel loss response shape. **Note:** When per rate settings are chosen, the Trace Driver Bypass settings are applied for all rates when CDR is unlocked (see CTRL_OUTPUT1_TRDR_PER_RATE for per rate setting).
		RSVD	7	R/W	0	Reserved—do not modify.
		CFG_OUTPUT1_TD_BYPASS_PREEMPH_PWRDWN	6	R/W	0	Trace driver output (DDO) Bypass pre-emphasis power-down. DDO power-down control for pre-emphasis driver. 0 = Pre-emphasis driver powered-up (pre-emphasis enabled) 1 = Pre-emphasis driver powered-down (pre-emphasis disabled) **Note:** When per rate settings are chosen, the Trace Driver Bypass settings are applied for all rates when CDR is unlocked (see CTRL_OUTPUT1_TRDR_PER_RATE for per rate setting).
		CFG_OUTPUT1_TD_BYPASS_PREEMPH_AMPL	5:0	R/W	1	Configure the Trace Driver output (DDO) Bypass pre-emphasis pulse amplitude. Range: 0 to 50_d. Adjust the pre-emphasis pulse amplitude to better match the channel loss at Nyquist. **Note:** When per rate settings are chosen, the Trace Driver Bypass settings are applied for all rates when CDR is unlocked (see CTRL_OUTPUT1_TRDR_PER_RATE for per rate setting).

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
		RSVD	15:14	R/W	0	Reserved—do not modify.
39	OUTPUT_ PARAM_ TD_BYPASS_1	CFG_OUTPUT1_TD_ BYPASS_DRIVER_ SWING	13:8	R/W	11	Configure the Trace Driver output (DDO) Bypass amplitude. Range = 0_d to 40_d Adjust the differential Trace Driver amplitude. The default value produces an amplitude of 400mV_{ppd}. **Note:** When per rate settings are chosen, the Trace Driver Bypass settings are applied for all rates when CDR is unlocked (see CTRL_OUTPUT1_TRDR_ PER_RATE for per rate setting).
		RSVD	7:0	R/W	70	Reserved—do not modify.
3A	RSVD	RSVD	15:0	R/W	201	Reserved—do not modify.
3B	RSVD	RSVD	15:0	R/W	1170	Reserved—do not modify.
3C	RSVD	RSVD	15:0	R/W	342	Reserved—do not modify.
3D	RSVD	RSVD	15:0	R/W	1C90	Reserved—do not modify.
3E	RSVD	RSVD	15:0	R/W	342	Reserved—do not modify.
3F	RSVD	RSVD	15:0	R/W	1C90	Reserved—do not modify.
40	RSVD	RSVD	15:0	R/W	340	Reserved—do not modify.
		RSVD	15:14	R/W	0	Reserved—do not modify.
41	OUTPUT_ PARAM_ MUTE_1	CFG_OUTPUT1_MUTE_ DRIVER_SWING	13:8	R/W	8	Controls the output mute differential latch voltage. Default is 8=~200mV_{diff}. Increasing the setting may be required for noisy environment, but mute power increases proportionally to mute differential latch voltage. Range = 0_d to 63_d **Note**: This parameter is only applicable to the trace driver output (DDO).
		RSVD	7:0	R/W	50	Reserved—do not modify.
42	RSVD	RSVD	15:0	R/W	340	Reserved—do not modify.
43	RSVD	RSVD	15:0	R/W	850	Reserved—do not modify.
44	RSVD	RSVD	15:0	R/W	342	Reserved—do not modify.
45	RSVD	RSVD	15:0	R/W	1C90	Reserved—do not modify.
46	RSVD	RSVD	15:0	R/W	342	Reserved—do not modify.
47	RSVD	RSVD	15:0	R/W	1C90	Reserved—do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
Output Control						
48	OUTPUT_SIG_SELECT	RSVD	15:4	R/W	10	Reserved - do not modify.
		CTRL_OUTPUT0_DATA_INVERT	3	R/W	0	Controls optional signal polarity inversion on SDIO when data is selected (CTRL_OUTPUT0_SIGNAL_SEL = 0).
		CTRL_OUTPUT1_DATA_INVERT	2	R/W	0	Controls optional signal polarity inversion on DDO when data is selected (CTRL_OUTPUT1_SIGNAL_SEL = 0).
		CTRL_OUTPUT0_SIGNAL_SEL	1	R/W	0	SDIO data vs PRBS select: 0 = Data 1 = PRBS Generator output (PRBS7 or divided version of PRBS Generator clock)
		CTRL_OUTPUT1_SIGNAL_SEL	0	R/W	0	DDO data vs PRBS select: 0 = Data 1 = PRBS Generator output (PRBS7 or divided version of PRBS Generator clock)
49	CONTROL_OUTPUT_MUTE	RSVD	15:6	R/W	0	Reserved—do not modify.
		CTRL_OUTPUT1_AUTO_MUTE_DURING_RATE_SEARCH	5	R/W	0	Selects if device is auto muted during rate search, based on loss of lock at the input in cable equalizer mode. 1= Mutes DDO when CDR is not locked to the applied signal. 0= Device does not auto mute. **Note**: If passing non-standard rates through the device or using the PRBS generator, set this parameter to 0.
		CTRL_OUTPUT0_AUTO_MUTE_DURING_RATE_SEARCH	4	R/W	0	Selects if device is auto muted during rate search, based on loss of lock at the input in cable driver mode. 1= Mutes SDIO when CDR is not locked to the applied signal. 0= Device does not auto mute. **Note**: If passing non-standard rates through the device or using the PRBS generator, set this parameter to 0.
		CTRL_OUTPUT1_MANUAL_MUTE	3	R/W	0	Force manual mute mode for DDO. 0 = Unmute 1 = Mute Controls mute for DDO when auto mute (CTRL_OUTPUT1_AUTO_MUTE) is disabled.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
49 (Continued)	CONTROL_ OUTPUT_ MUTE (Continued)	CTRL_OUTPUT1_ AUTO_MUTE	2	R/W	1	Select automatic or manual mute control for DD0. 0 = Disable auto mute mode 1 = Enable auto mute mode If CTRL_OUTPUT1_AUTO_MUTE = 0, then CTRL_OUTPUT1_MANUAL_MUTE controls mute for DDO.
		CTRL_OUTPUT0_ MANUAL_MUTE	1	R/W	0	Force manual mute mode for SDIO. Same settings description as CTRL_OUTPUT1_ MANUAL_MUTE.
		CTRL_OUTPUT0_ AUTO_MUTE	0	R/W	1	Select automatic or manual mute control for SDIO Same settings description as CTRL_OUTPUT1_ AUTO_MUTE.
4A	CONTROL_ OUTPUT_ DISABLE	RSVD	15:4	R/W	0	Reserved—do not modify.
		CTRL_OUTPUT1_ MANUAL_DISABLE	3	R/W	0	Force manual disable mode for DDO. 0 = Enable output driver 1 = Disable (power-down) output driver. Controls disable for DDO when auto mute (CTRL_OUTPUT1_AUTO_DISABLE) is disabled.
		CTRL_OUTPUT1_ AUTO_DISABLE	2	R/W	0	Select automatic or manual disable control for DD0. 0 = Disable auto disable mode 1 = Enable auto disable mode If CTRL_OUTPUT1_AUTO_DISABLE = 0, then CTRL_OUTPUT1_MANUAL_DISABLE controls disable for DDO.
		CTRL_OUTPUT0_ MANUAL_DISABLE	1	R/W	0	Force manual disable mode for SDIO. Same settings description as CTRL_OUTPUT1_ MANUAL_DISABLE.
		CTRL_OUTPUT0_ AUTO_DISABLE	0	R/W	0	Select automatic or manual disable control for SDIO. Same settings description as CTRL_OUTPUT1_ AUTO_DISABLE.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
4B	CONTROL_OUTPUT_SLEW	RSVD	15:13	R/W	0	Reserved—do not modify.
		CTRL_OUTPUT1_TRDR_PER_RATE	12	R/W	0	Controls whether common or per rate trace driver output (DDO) settings are used: 0 = Common trace driver settings: CFG_OUTPUT1_TD_SD_* settings are used for all rates 1 = Per rate trace driver settings: CFG_OUTPUT1_TD_<rate>_* are used when CDR is locked to <rate> (See Table 2-3). **Note**: CFG_OUTPUT1_TD_BYPASS_* are used when CDR is not locked.
		RSVD	11:3	R/W	A0	Reserved—do not modify.
		CTRL_OUTPUT0_MANUAL_SLEW	2:1	R/W	2	Selects slew rate for SDIO when auto slew rate is disabled. 0 = SD/MADI slew 1 = HD/3G slew 2 = Bypass
		CTRL_OUTPUT0_AUTO_SLEW	0	R/W	1	Selects between auto or manual slew rate selection for SDIO. 0 = Disable auto slew rate selection 1 = Enable auto slew rate selection **Note:** In auto slew mode (CTRL_OUTPUT0_AUTO_SLEW = 1), the slew rate is determined by the rate at which the CDR is locked. If the CDR is unlocked, the slew will default to Bypass Slew. See Table 2-3 for Rise/Fall times, and Section 4.8.3 for more details on output driver selection.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
4C	CONTROL_ RETIMER_ BYPASS	RSVD	15:4	R/W	0	Reserved—do not modify.
		CTRL_OUTPUT1_ RETIMER_MANUAL_ BYPASS	3	R/W	0	Controls retimer bypass for DDO when auto mode is disabled. 0 = Disable retimer bypass 1 = Enable retimer bypass
		CTRL_OUTPUT1_ RETIMER_AUTO_ BYPASS	2	R/W	1	Selects between auto and manual control of retimer bypass for DDO. 0 = Disable auto mode 1 = Enable auto mode
		CTRL_OUTPUT0_ RETIMER_MANUAL_ BYPASS	1	R/W	0	Controls retimer bypass for SDIO when auto mode is disabled. 0 = Disable retimer bypass 1 = Enable retimer bypass
		CTRL_OUTPUT0_ RETIMER_AUTO_ BYPASS	0	R/W	1	Selects between auto and manual control of retimer bypass for SDIO. 0 = Disable auto mode 1 = Enable auto mode
4D	CONTROL_ BALANCED_ MODE	RSVD	15:1	R/W	0	Reserved—do not modify.
		CTRL_OUTPUT0_ BALANCED	0	R/W	0	Enable or disable balanced mode on SDIO for powered output return loss measurement. 0 = Disable 1 = Enable
4E to 4F	RSVD	RSVD	15:0	R/W	0	Reserved—do not modify.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
			Test Functions			

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
50	PRBS_ CHK_CFG	RSVD	15	R/W	0	Reserved—do not modify.
		CFG_PRBS_CHECK_ PHASEADJUST	14:13	R/W	0	Adjusts the phase of the clock to the PRBS Checker. Values are: 0 = 0° 1 = 90° 2 = 180° 3 = 270° **Note:** A setting of 0° is ideal for most applications. Adjustment is not expected.
		CFG_PRBS_CHECK_ INVERT	12	R/W	0	Optionally inverts the retimed data at the input to the PRBS Checker: 0 = no inversion 1 = data inverted
		CFG_PRBS_CHECK_ PREDIVIDER	11:8	R/W	0	Selects pre-divider for PRBS check measurement timer: 0 = 4 1 = 8 2 = 16 3 = 32 4 = 64 5 = 128 6 = 256 7 = 512 8 = 1024 9 = 2048
		CFG_PRBS_CHECK_ MEAS_TIME	7:0	R/W	3	Selects PRBS check measurement interval for timed measurements. See Section 4.5.1 for more details.
51	PRBS_CHK_ CTRL	RSVD	15:9	R/W	0	Reserved—do not modify.
		CTRL_PRBS_CHECK_ TIMED_CONT_B	8	R/W	0	0 = Selects continuous PRBS check mode 1 = Selects timed PRBS check mode
		RSVD	7:1	R/W	0	Reserved—do not modify.
		CTRL_PRBS_CHECK_ START	0	R/W	0	Set to 1 by host to start a timed operation. Set to 0 by host after completion or abort of the operation (by the device due to LOL) to tell the device that PRBS result has been read by the host. See Section 4.5 PRBS Checker for more details on PRBS checker function.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
52	PRBS_GEN_CTRL	RSVD	15:10	R/W	0	Reserved—do not modify.
		CTRL_PRBS_GEN_ENABLE	9	R/W	0	Selects whether the PRBS generator is enabled or not: 0 = PRBS Generator disabled 1 = PRBS Generator enabled **Note:** enabling the PRBS Generator does not automatically override other device modes such as auto-sleep, auto-output-mute, auto-output-disable, etc. These continue to function normally. The user/host may need to adjust those settings to ensure the part will output the PRBS signal.
		CTRL_PRBS_GEN_SIGNAL_SELECT	8	R/W	1	Select output signal from PRBS Generator as either PRBS7 or divided clock (divided version of the PRBS Generator's clock source): 0 = clock divider (using ratio set by CTRL_PRBS_GEN_CLK_DIVIDER) 1 = PRBS7
		CTRL_PRBS_GEN_CLK_SRC	7:6	R/W	0	Selects clock source for PRBS Generator: 0 = VCO (free running) 1 = Reserved. 2 = Reserved. 3 = Data reference PLL (CDR recovered clock)
		CTRL_PRBS_GEN_CLK_DIVIDER	5:4	R/W	0	Selects clock divider ratio for when host selects divided clock to output on PRBS Generator (CTRL_PRBS_GEN_SIGNAL_SELECT = 0): 0 = Divide by 2 1 = Divide by 4 2 = Divide by 8 3 = Divide by 16
		CTRL_PRBS_GEN_INVERT	3	R/W	0	Controls optional inversion of the generated PRBS pattern: 0 = true sense 1 = inverted

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
52 (Continued)	PRBS_GEN_ CTRL (Continued)	CTRL_PRBS_GEN_ DATA_RATE	2:0	R/W	6	Select PRBS7 data rate when PRBS clock source not recovered clock (CTRL_PRBS_GEN_CLK_SRC ≠ 3) 0 = Reserved—do not use 1 = MADI 2 = SD 3 = HD 4 = 3G 5 = Reserved - do not use 6 = Reserved - do not use 7 = Reserved - do not use. If CTRL_PRBS_GEN_CLK_SRC = 3, then CTRL_PRBS_GEN_DATA_RATE setting has no effect and the CDR rate is used (based on automatic rate detection or manual rate selection). Additionally, if the device is locked to an input signal, only the same rate can be selected for the PRBS Generator.
53	RSVD	RSVD	15:0	R/W	0	Reserved—do not modify.
54	EYE_MON_ INT_CFG_0	CFG_EYE_MON_ TIMEOUT_MS	15:0	R/W	0	CFG_EYE_MON_TIMEOUT[31:16] Most significant 16 bits of the measurement time. This is the time spent measuring bit errors at each point in the eye scan, i.e. the time to measure one point in the eye. Units are in microseconds. The Eye Scanner scans each point twice and there is some overhead, so the actual measurement time is twice the number entered. **Valid range:** 1 to 6555_d 65536_d to 104895_d 131072_d to 3350000_d
55	EYE_MON_ INT_CFG_1	CFG_EYE_MON_ TIMEOUT_LS	15:0	R/W	64	CFG_EYE_MONT_TIMEOUT[15:0] Least significant 16 bits of the measurement time. See CFG_EYE_MON_ TIMEOUT_MS.
56	EYE_MON_ INT_CFG_2	CFG_EYE_BER_ THRESHOLD	15:0	R/W	64	Threshold of bit error counts to define good vs bad points in eye for shape scan. See Section 4.6 for further details.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
57	EYE_MON_INT_CFG_3	CFG_EYE_DEFAULT_VERT_OFFSET	15:8	R/W	80	The vertical offset slice that will be used for eye shape queries. Offset values: 0 to 255_d. 0 represents the most negative slice since 128_d is the 0V slice level and 255_d is the most positive slice level. Default is 128_d.
		RSVD	7:3	R/W	0	Reserved—do not modify.
		CFG_EYE_INIT_RESET	2	R/W	0	Eye monitor initialization bit. Set HIGH during Device Power-up Sequence. See Section 4.10.12 for details.
		RSVD	1:0	R/W	2	Reserved—do not modify.
58 to 59	RSVD	RSVD	15:0	R/W	0	Reserved—do not modify.
5A	EYE_MON_SCAN_CTRL_0	RSVD	15	R/W	0	Reserved—do not modify.
		CTRL_EYE_PHASE_START	14:8	R/W	0	Starting phase offset. Valid range is 0_d to 127_d. Reset value must be used for shape scan.
		RSVD	7	R/W	0	Reserved—do not modify.
		CTRL_EYE_PHASE_STOP	6:0	R/W	7F	Phase offset limit. Valid range is 0_d to 127_d. CTRL_EYE_PHASE_STOP must be greater or equal to CTRL_EYE_PHASE_START. Reset value must be used for shape scan.
5B	EYE_MON_SCAN_CTRL_1	RSVD	15	R/W	0	Reserved—do not modify.
		CTRL_EYE_PHASE_STEP	14:8	R/W	1	Unsigned value for phase step size. Valid values are 1,2, and 4. Reset value must be used for shape scan. Behaviour is undefined for other values. In order to use a step size of 2 or 4, CTRL_EYE_PHASE_START and CTRL_EYE_PHASE_STOP must be set to their default values.
		RSVD	7	R/W	0	Reserved—do not modify.
		CTRL_EYE_VERT_OFFSET_START	6:0	R/W	0	Starting voltage offset. Valid range is 0_d to 255_d.

Table 5-3: Control Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
5C	EYE_MON_ SCAN_CTRL_2	CTRL_EYE_VERT_ OFFSET_STOP	15:8	R/W	FF	Voltage offset limit. Valid range is 0 to 255_d. CTRL_EYE_VERT_OFFSET_STOP must be greater or equal to CTRL_EYE_VERT_OFFSET_START. Reset value must be used for shape scan.
		RSVD	7	R/W	0	Reserved—do not modify.
		CTRL_EYE_VERT_ OFFSET_STEP	6:0	R/W	1	Unsigned value for voltage offset step size. Valid values are 1,2, and 4. Behaviour is undefined for other values. In order to use a step size of 2 or 4, CTRL_EYE_VERT_OFFSET_START and CTRL_EYE_VERT_OFFSET_STOP must be set to their default values.
5D	EYE_MON_ SCAN_CTRL_3	RSVD	15:9	R/W	0	Reserved—do not modify.
		CTRL_EYE_SHAPE_ SCAN_B	8	R/W	0	Selects whether the Eye Monitor should perform an eye scan or eye shape capture: 0 = Selects eye scan (new or continued) 1 = Selects eye shape capture
		RSVD	7:2	R/W	0	Reserved—do not modify.
		CTRL_EYE_MON_ POWER_CTRL	1	R/W	0	Power control for the Eye Monitor: 0 = Power-down the Eye Monitor 1 = Power-up the Eye Monitor Host is permitted to change this any time between eye scans (but not between partial eye scans). This must be set to 1 to run an eye scan. Behaviour is undefined if host sets CTRL_EYE_MON_START = 1 without setting this bit to 1.
		CTRL_EYE_MON_START	0	R/W	0	Part of a four way handshake with STAT_EYE_MON_STATUS: 0 = Set by host to tell the device to clear the status bit 1 = Set by host only in order to begin/continue an eye scan or start an eye shape capture See Section 4.6 for more details on implementing the four way hand shake for this operation.
5E to 5F	RSVD	RSVD	15:0	—	—	Reserved.
Factory Settings						
60 to 7E	RSVD	RSVD	15:0	—	—	Reserved.

5.3.2 Status Register Descriptions

Table 5-4: Status Register Descriptions

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
80	RSVD	RSVD	15:0	RO	—	Reserved—do not modify.
81	VERSION_0	STAT_CONFIG_VER0	15:0	RO	—	This register contains the first part of the device configuration version. Please contact your local technical sales representative for more details.
82	VERSION_1	STAT_CONFIG_VER1	15:0	RO	—	This register contains the second part of the device configuration version. Please contact your local technical sales representative for more details.
83	VERSION_2	STAT_HW_VERSION	15:0	RO	—	This register contains the devices identification, including revision. Please contact your local technical sales representative for more details.
84	STICKY_ COUNTS_0	STAT_CNT_PRI_CD_ CHANGES	15:8	RO	—	Count of primary carrier detection status changes (ignoring CLI squelch in Cable Equalizer Mode). The count saturates at 255_d (0xFF). See Section 4.10.11 for procedure to clear the counts.
		STAT_CNT_SEC_CD_ CHANGES	7:0	RO	—	Count of secondary carrier detection status changes (based on STAT_CLI_ SQUELCH if CFG_SEC_CD_ INCL_ CLI_SQUELCH = 1; otherwise this parameter is based on STAT_PRI_CD). The count saturates at 255_d (0xFF). See Section 4.10.11 for procedure to clear the counts. **Note**: This parameter is only applicable to the cable equalizer input (SDIO).
85	STICKY_ COUNTS_1	STAT_CNT_RATE_ CHANGES	15:8	RO	—	Count of rate changes. The count saturates at 255_d (0xFF). See Section 4.10.11 for procedure to clear the counts.
		STAT_CNT_PLL_ LOCK_CHANGES	7:0	RO	—	Count of PLL lock status changes. The count saturates at 255_d (0xFF). See Section 4.10.11 for procedure to clear the counts.

Table 5-4: Status Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
86	CURRENT_STATUS_0	RSVD	15	RO	—	Reserved—do not modify.
		STAT_CLEAR_COUNTS_STATUS	14:13	RO	—	0 = Idle 1 = Reserved 2 = Indicates device has cleared the sticky counts 3 = Reserved Part of a four way handshake with CTRL_CLEAR_COUNTS. See Section 4.10.11 for more details on implementing the four way handshake for this operation.
		STAT_LOCK	12	RO	—	0 = PLL is unlocked 1 = PLL is locked
		STAT_SLEEP	11	RO	—	0 = Device is not in sleep 1 = Device is currently in sleep
		RSVD	10	RO	—	Reserved—do not modify.
		STAT_ACTIVE_DIRECTION	9	RO	—	Indicates currently selected direction of device: 0 = Cable Equalizer / receiver mode 1 = Cable Driver / transmitter mode
		STAT_CLI_SQUELCH	8	RO	—	Cable Equalizer squelch status. 0 = CLI squelch is de-asserted 1 = CLI squelch is asserted **Note**: This parameter is only applicable to the cable equalizer input (SDIO).
		STAT_OUTPUT1_MODE	7:4	RO	—	DDO output status: 0 = Mission Trace Driver <= SD rate 1 = Mission Trace Driver HD rate 2 = Mission Trace Driver 3G rate 3 = Reserved 4 = Reserved 5 = Reserved 6 = Muted 7 = Disabled **Note**: The device will only indicate 1-4 if the per rate settings are enabled, otherwise, it will always indicate 0 if it is locked to a valid signal and the output is not muted or disabled. See section Section 4.8.3 Output Driver Data Rate Selection for more details.

Table 5-4: Status Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
86 (Continued)	CURRENT_ STATUS_0 (Continued)	STAT_OUTPUT0_MODE	3:0	RO	—	SDIO output status: 0 = Mission Cable Driver SD/MADI slew rate 1 = Mission Cable Driver HD/3G slew rate 2 = Reserved 3 = Reserved 4 = Reserved 5 = Balanced 6 = Muted 7 = Disabled
87	CURRENT_ STATUS_1	STAT_OUTPUT1_ DISABLE	15	RO	—	DDO Disable Status 0 = DDO is not disabled 1 = DDO is disabled
		STAT_OUTPUT0_ DISABLE	14	RO	—	SDIO Disable Status 0 = SDIO is not disabled 1 = SDIO is disabled
		STAT_OUTPUT1_ MUTE	13	RO	—	DDO Mute Status 0 = DDO is not muted 1 = DDO is muted
		STAT_OUTPUT0_MUTE	12	RO	—	SDIO Mute Status 0 = SDIO is not muted 1 = SDIO is muted
		STAT_OUTPUT1_ RETIMER_BYPASS	11	RO	—	DDO Re-timer Status 0 = Retimer path to DDO is not bypassed 1 = Retimer path to DDO is bypassed
		STAT_OUTPUT0_ RETIMER_BYPASS	10	RO	—	SDIO Re-timer Status 0 = Retimer path to SDIO is not bypassed 1 = Retimer path to SDIO is bypassed
		STAT_SEC_CD	9	RO	—	Secondary carrier detection status (based on STAT_CLI_SQUELCH if CFG_SEC_CD_INCL_CLI_SQUELCH=1; otherwise this parameter is based on STAT_PRI_CD). 0 = Secondary carrier is not detected 1 = Secondary carrier is detected **Note:** This status is only applicable to the cable equalizer input (SDIO).

Table 5-4: Status Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
87 (Continued)	CURRENT_ STATUS_1 (Continued)	STAT_PRI_CD	8	RO	—	Primary carrier detection status (ignoring CLI squelch for Cable Equalizer input (SDIO)). 0 = Primary carrier is not detected 1 = Primary carrier is detected
		STAT_CEQ_BYPASS	7	RO	—	Cable Equalizer bypass status: 0 = CEQ is not bypassed 1 = CEQ is bypassed **Note:** This parameter is only applicable to the cable equalizer input (SDIO).
		RSVD	6:5	RO	—	Reserved—do not modify.
		STAT_OUTPUT0_ SLEW_RATE	4:3	RO	—	SDIO slew rate when in Cable Driver Mode. 0 = SD/MADI slew 1 = HD/3G slew 2 = Bypass
		STAT_DETECTED_RATE	2:0	RO	—	Rate at which the CDR is locked. 0 = Unlocked 1 = MADI (125Mb/s) 2 = SD (270Mb/s) 3 = HD (1.485Gb/s) 4 = 3G (2.97Gb/s) 5 = Reserved 6 = Reserved 7 = Reserved
88	EQ_GAIN_IND	RSVD	15:8	RO	—	Reserved—do not modify.
		STAT_CABLE_LEN_ INDICATION	7:0	RO	—	SDIO cable length indication when in Cable Equalizer Mode. Range = 0 to 64_d (64_d is max cable reach determined for specific rate, cable type, and launch swing compensation). 0xFF = Unknown cable length **Note**: This parameter is only applicable to the cable equalizer input (SDIO).
89	PRBS_ CHK_ERR_CNT	STAT_PRBS_CHK_ ERR_CNT	15:0	RO	—	PRBS Checker error count. Cleared to 0 at the start of a measurement. Updated by the device on completion of a measurement. Value is undefined in case of abort due to loss of CDR lock (STAT_PRBS_CHECK_LAST_ABORT = 1).

Table 5-4: Status Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
		RSVD	15:10	RO	—	Reserved—do not modify.
		STAT_PRBS_CHECK_NODATA	9	RO	—	0 = Normal 1 = No data transitions were seen during the previous PRBS check This bit is set to 1 to indicate that the input data was all 0's during a PRBS check. When that happens, the error count will be zero when in fact there was no valid PRBS pattern. This bit is updated by the device on completion of a measurement. It retains its value until the next PRBS check operation is requested. Value is undefined in case of abort (STAT_PRBS_CHECK_LAST_ABORT = 1). Value does not increment during a measurement until it completes.
8A	PRBS_CHK_STATUS	STAT_PRBS_CHECK_LAST_ABORT	8	RO	—	This bit retains its value until the next PRBS operation is requested. 0 = Normal 1 = PRBS check was aborted due to loss of lock or sleep
		RSVD	7:2	RO	—	Reserved—do not modify.
		STAT_PRBS_CHECK_STATUS	1:0	RO	—	Status for PRBS Checker: 0 = PRBS check idle; ready for new operation 1 = PRBS check timed or continuous operation in progress 2 = PRBS check timed operation completed (success) 3 = PRBS check timed or continuous operation aborted (error) Part of a four way handshake with CTRL_PRBS_CHECK_START (Section 4.5). Abort will be reported if loss of lock or sleep occurred during a PRBS check operation or those conditions existed when the operation was requested by the host.
8B	EYE_MON_SCAN_SIZE_OUTPUT	STAT_EYE_IMAGE_SIZE	15:0	RO	—	The size in bytes of the last partial scan segment.

Table 5-4: Status Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
8C	EYE_MON_SHAPE_OUTPUT_0	STAT_EYE_SHAPE_LEFT_EDGE_OFFSET	15:8	RO	—	Left Edge Voltage Offset—Offset values 0 to 255_d, 0 represents most negative voltage, 127_d is 0V 255_d is most positive voltage.
		STAT_EYE_SHAPE_LEFT_EDGE_PHASE	7:0	RO	—	Left Edge Phase of eye shape scan. Phase values 0 to 127_d.
8D	EYE_MON_SHAPE_OUTPUT_1	STAT_EYE_SHAPE_POS_EDGE_OFFSET	15:8	RO	—	Positive (top) Edge Voltage Offset—Offset values 0 to 255_d, 0 represents most negative voltage, 127_d is 0V 255_d is most positive voltage.
		STAT_EYE_SHAPE_POS_EDGE_PHASE	7:0	RO	—	Positive (top) Edge Phase of eye shape scan. Phase values 0 to 127_d.
8E	EYE_MON_SHAPE_OUTPUT_2	STAT_EYE_SHAPE_RIGHT_EDGE_OFFSET	15:8	RO	—	Right Edge Voltage Offset—Offset values 0 to 255_d, 0 represents most negative voltage, 127_d is 0V 255_d is most positive voltage.
		STAT_EYE_SHAPE_RIGHT_EDGE_PHASE	7:0	RO	—	Right Edge Phase of eye shape scan. Phase values 0 to 127_d.
8F	EYE_MON_SHAPE_OUTPUT_3	STAT_EYE_SHAPE_NEG_EDGE_OFFSET	15:8	RO	—	Negative (bottom) Edge Voltage Offset—Offset values 0 to 255_d, 0 represents most negative voltage, 127_d is 0V 255_d is most positive voltage.
		STAT_EYE_SHAPE_NEG_EDGE_PHASE	7:0	RO	—	Negative (bottom) Edge Phase of eye shape scan. Phase values 0 to 127_d.

Table 5-4: Status Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
90	EYE_MON_ STATUS	RSVD	15:9	RO	—	Reserved—do not modify.
		STAT_EYE_SCAN_ PARTIAL_OR_FULL	8	RO	—	0 = Full scan 1 = Partial scan On completion of an Eye Monitor eye scan (CRTL_EYE_SHAPE_SCAN_B = 0), indicates whether the Eye Monitor completed the full scan or a partial scan. Undefined for eye shape scan (CTRL_EYE_SHAPE_SCAN_B = 1).
		RSVD	7:2	RO	—	Reserved—do not modify.
		STAT_EYE_MON_ STATUS	1:0	RO	—	0 = Eye Monitor idle; ready for new operation 1 = Eye Monitor operation in progress 2 = Eye Monitor operation completed (success) 3 = Eye Monitor operation aborted (error) Part of a four way handshake with CTRL_EYE_MON_START, see Section 4.6 for procedure. Abort will be reported by device if loss of lock or sleep occurred during an Eye Monitor operation or those conditions existed when the operation was requested by the host.
91 to BF	RSVD	RSVD	15:0	RO	—	Reserved—do not modify.

6. Application Information

6.1 Typical Application Circuit

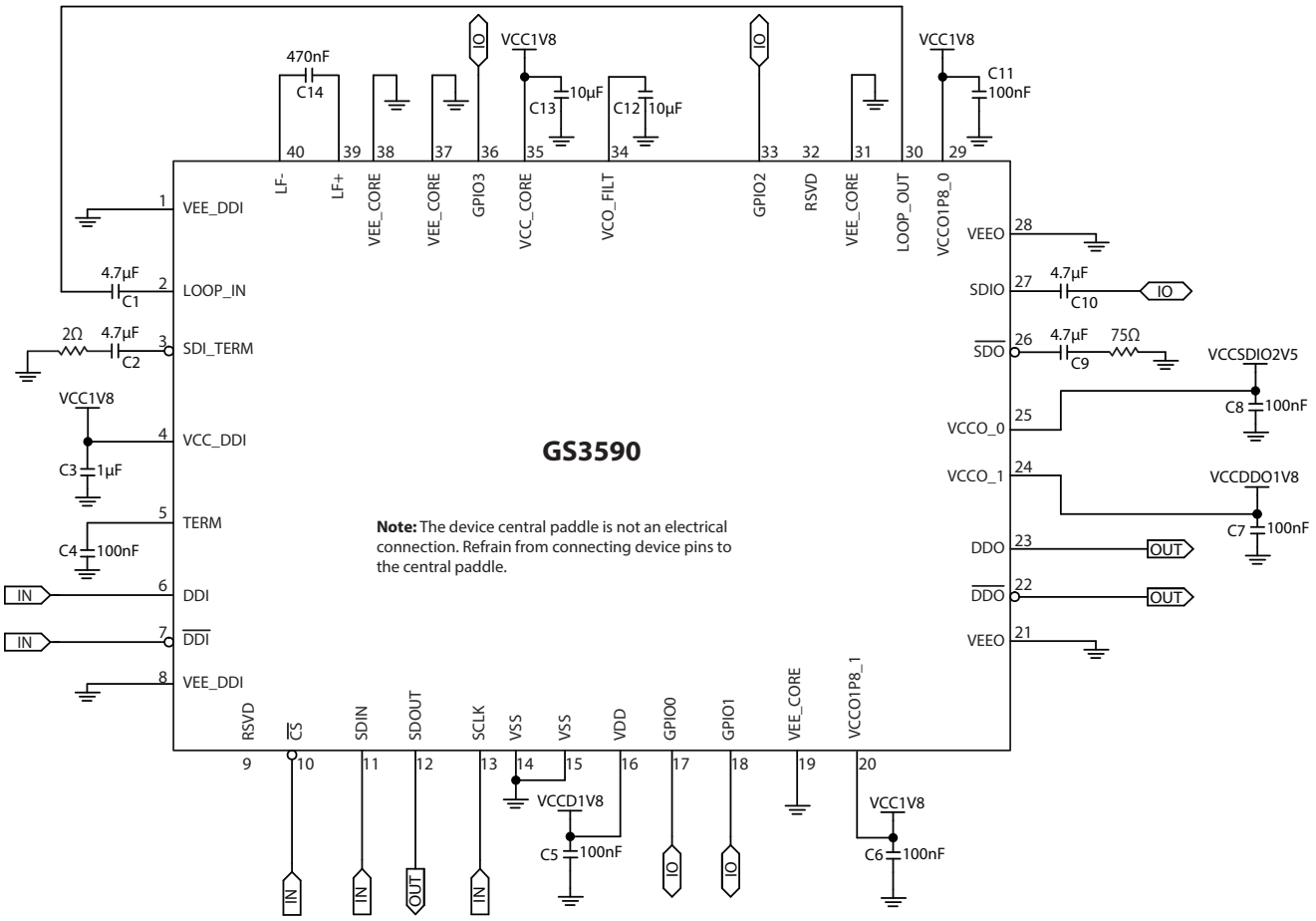


Figure 6-1: Typical Application Circuit

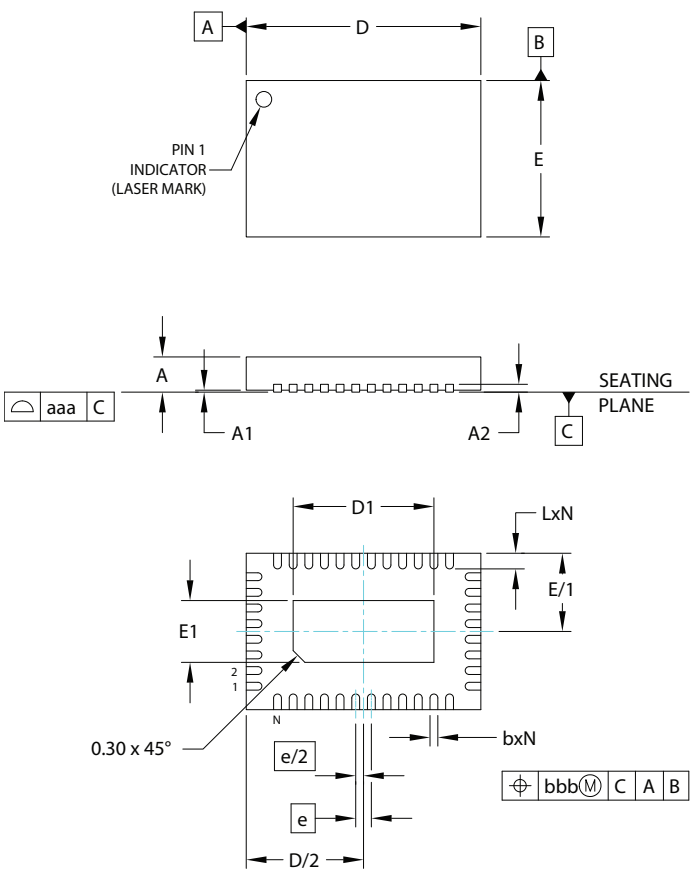
Note 1: 4.7µF AC-coupling capacitors are required on *DDO/$\overline{DDO}$* when the downstream IC has an input common mode range that is incompatible with the output common mode range of the GS3590.

Note 2: Pin 2 must be connected to pin 30 through a 4.7µF capacitor and a carefully designed transmission line for Cable Equalizer mode to be functional.

Note 3: It is recommended that separate filtered supplies are used for the following three groups: (V_{CC_DDI}, V_{CC_CORE}), (V_{CCO1P8_0}, V_{CCO1P8_1}, V_{DD}, V_{CCO_1}*), (V_{CCO_0}).
*Assuming Vcco supply is chosen as 1.8V.
Multiple devices can share the same filtered supply plane.

7. Package & Ordering Information

7.1 Package Dimensions



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		(0.02)	
b	0.15	0.20	0.25
D	5.95	6.00	6.05
D1	3.45	3.60	3.70
E	3.95	4.00	4.05
E1	1.43	1.58	1.68
e	0.40 BSC		
L	0.30	0.40	0.50
N	40		
aaa	0.08		
bbb	0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DIMENSION OF LEAD WIDTH APPLIES TO TERMINAL AND IS MEASURED BETWEEN 0.15 to 0.30mm FROM THE TERMINAL TIP.

Figure 7-1: Package Dimensions

7.2 Recommended PCB Footprint

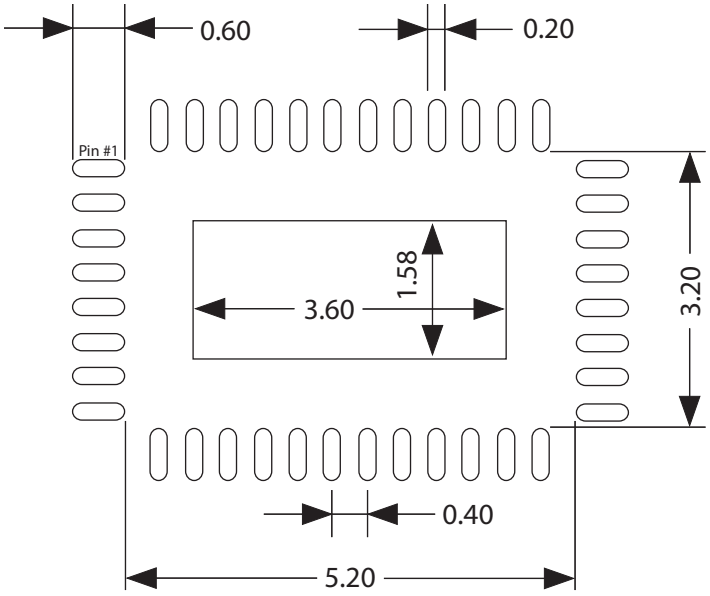


Figure 7-2: Recommended PCB Footprint

7.3 Packaging Data

Table 7-1: Packaging Data

Parameter	Value
Package Type	6mm x 4mm 40-pin QFN
Moisture Sensitivity Level	3
Junction to Air Thermal Resistance, $\theta_{j\text{-}a}$ (at zero airflow)	40.0°C/W
Junction to Board Thermal Resistance, $\theta_{j\text{-}b}$	32.0°C/W
Junction to Case Thermal Resistance, $\theta_{j\text{-}c}$	36.0°C/W
Junction-to-Top Characterization Parameter, Psi, Ψ	<1.0°C/W
Pb-free and RoHS compliant	Yes

7.4 Marking Diagram

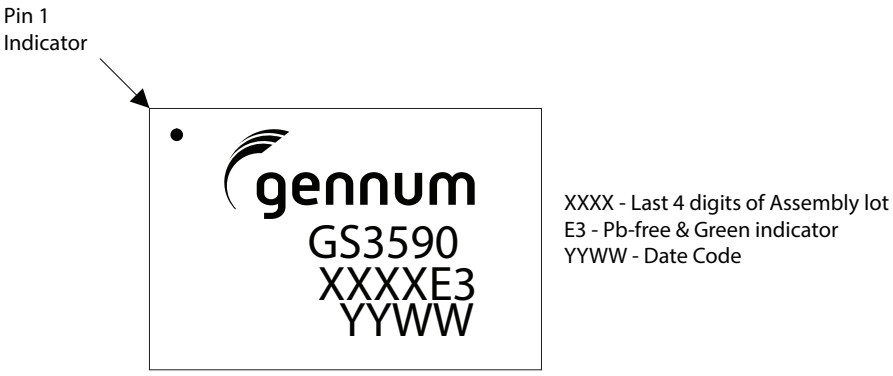


Figure 7-3: Marking Diagram

7.5 Solder Reflow Profiles

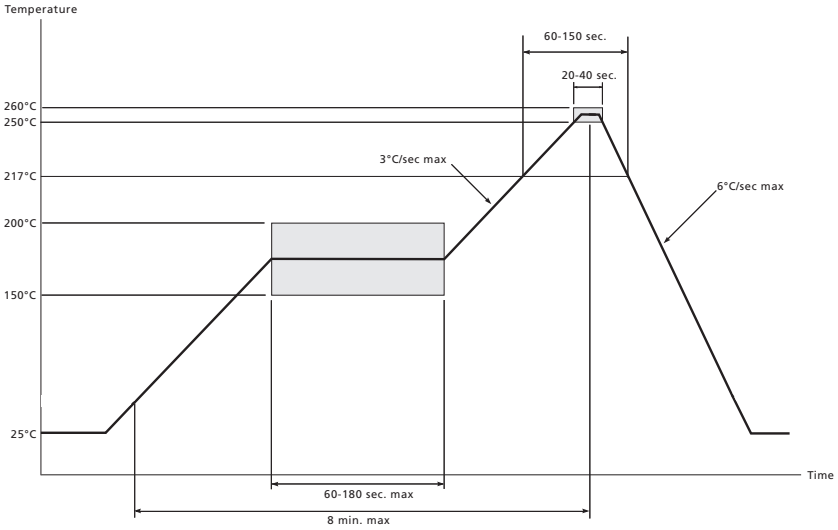


Figure 7-4: Maximum Pb-free Solder Reflow Profile

7.6 Ordering Information

Table 7-2: Ordering Information

Part Number	Minimum Order Quantity	Format
GS3590-INE3	490	Tray
GS3590-INTE3	250	Tape and Reel
GS3590-INTE3Z	2500	Tape and Reel

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