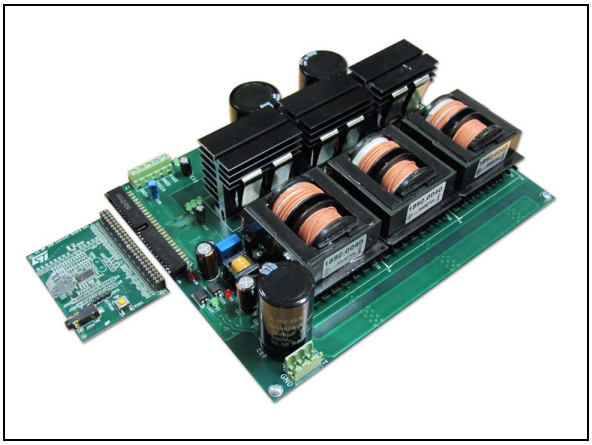
EVLSTNRG-1KW

1 kW SMPS digitally controlled multiphase interleaved converter using STNRG388A

Data brief



Features

- Digital controller: STNRG388A
- 3-phase interleaved DC/DC architecture
- Full load power: 1000 W (scalable up to 3 kW)
- Efficiency: more than 94% from 10% to full load
- Peak efficiency: 96.5% at full load
- Stand-by consumption: 425 mW
- Input voltage range: 350 ÷ 420 V dc
- CC/CV output regulation
- Output voltage regulation: 133 V
- Output current regulation: 7.5 A
- Maximum output current for each phase: 2.5 A
- Modular power and control board

Description

The EVLSTRNG-1KW evaluation board is intended for evaluating the STNRG388A digital controller in offline power conversion applications such as EV battery chargers, UPS and industrial power supplies.

The architecture is based on a multiphase interleaved DC/DC converter using the half bridge SAB (“Single Active Bridge”) topology supporting more than 1000 W of power.

The interleaved topology balances the power through 3 parallel stages. Also, the solution delivers high efficiency during the whole load range by enabling one, two or three stages depending on the load.

The STNRG388A power conversion dedicated peripherals (SMEDs) offer the flexibility to drive the interleaved power stages while guaranteeing the correct phase realignment during the activation and deactivation of each stage.

Thanks to the digital core of the STNRG388A, it is also possible to monitor, control and debug the EVLSTRNG-1KW board via a convenient HyperTerminal control.

For further information contact your local STMicroelectronics sales office. www.st.com

Schematic diagrams

Figure 1. Power board schematic diagram - power section and feedback

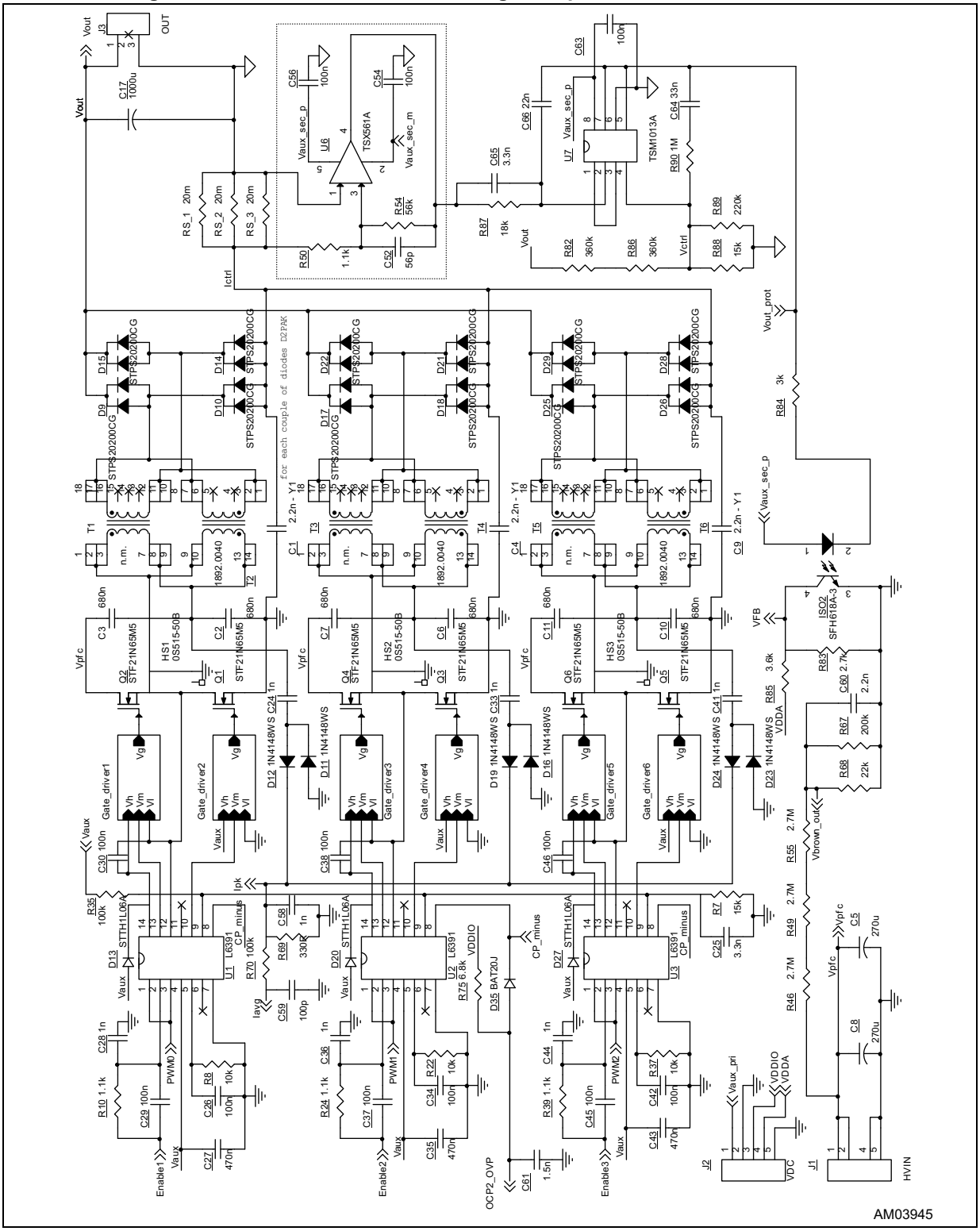


Figure 2. Power board schematic diagram - auxiliary supply and protections

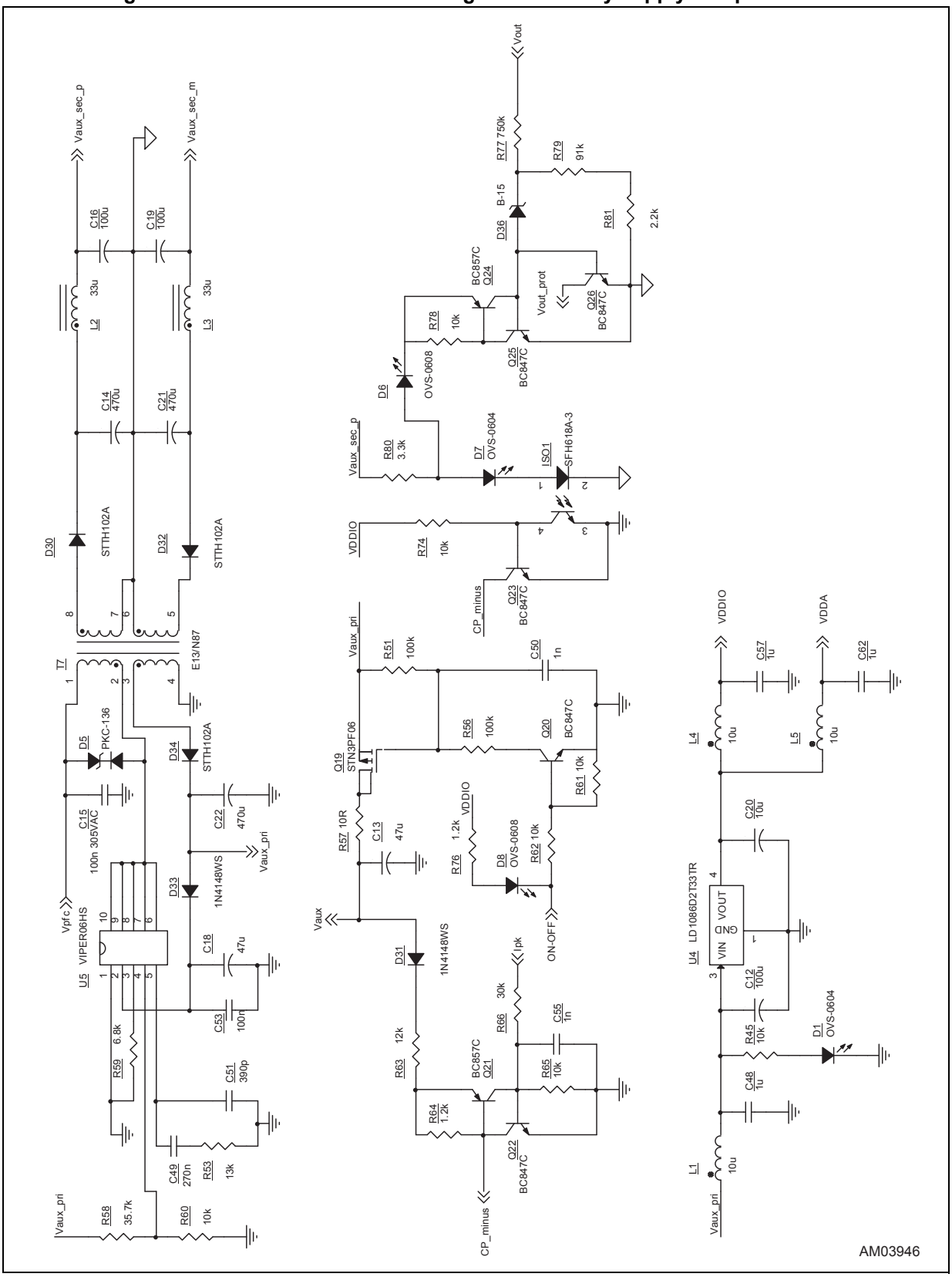


Figure 3. Power board schematic diagram - connector to control board

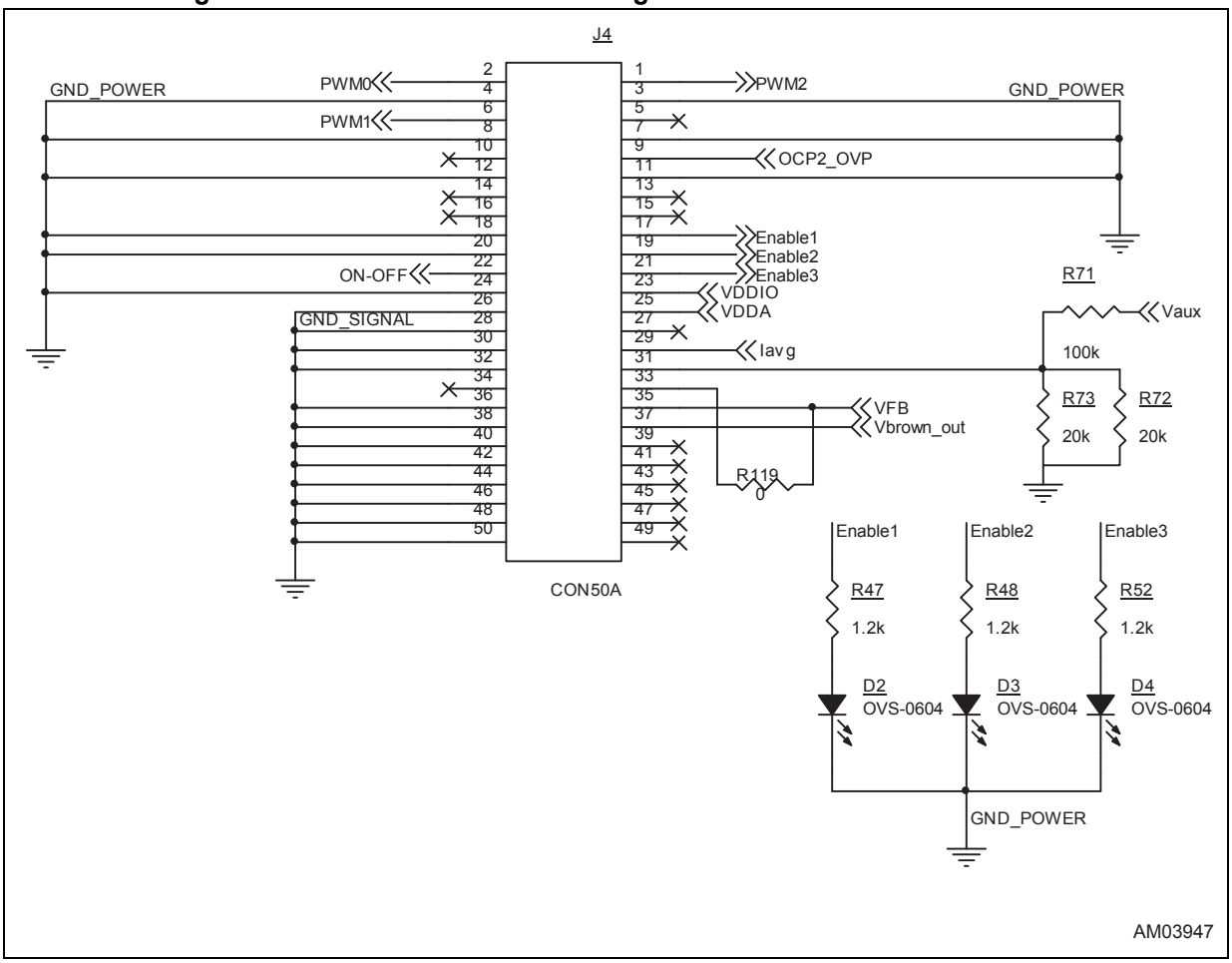


Figure 4. Power board schematic diagram - gate driver subcircuit

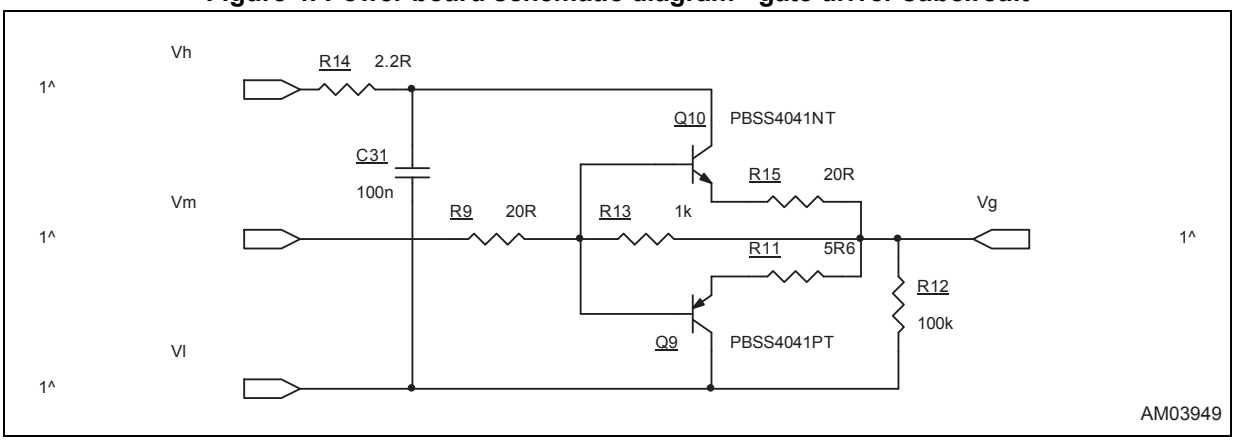
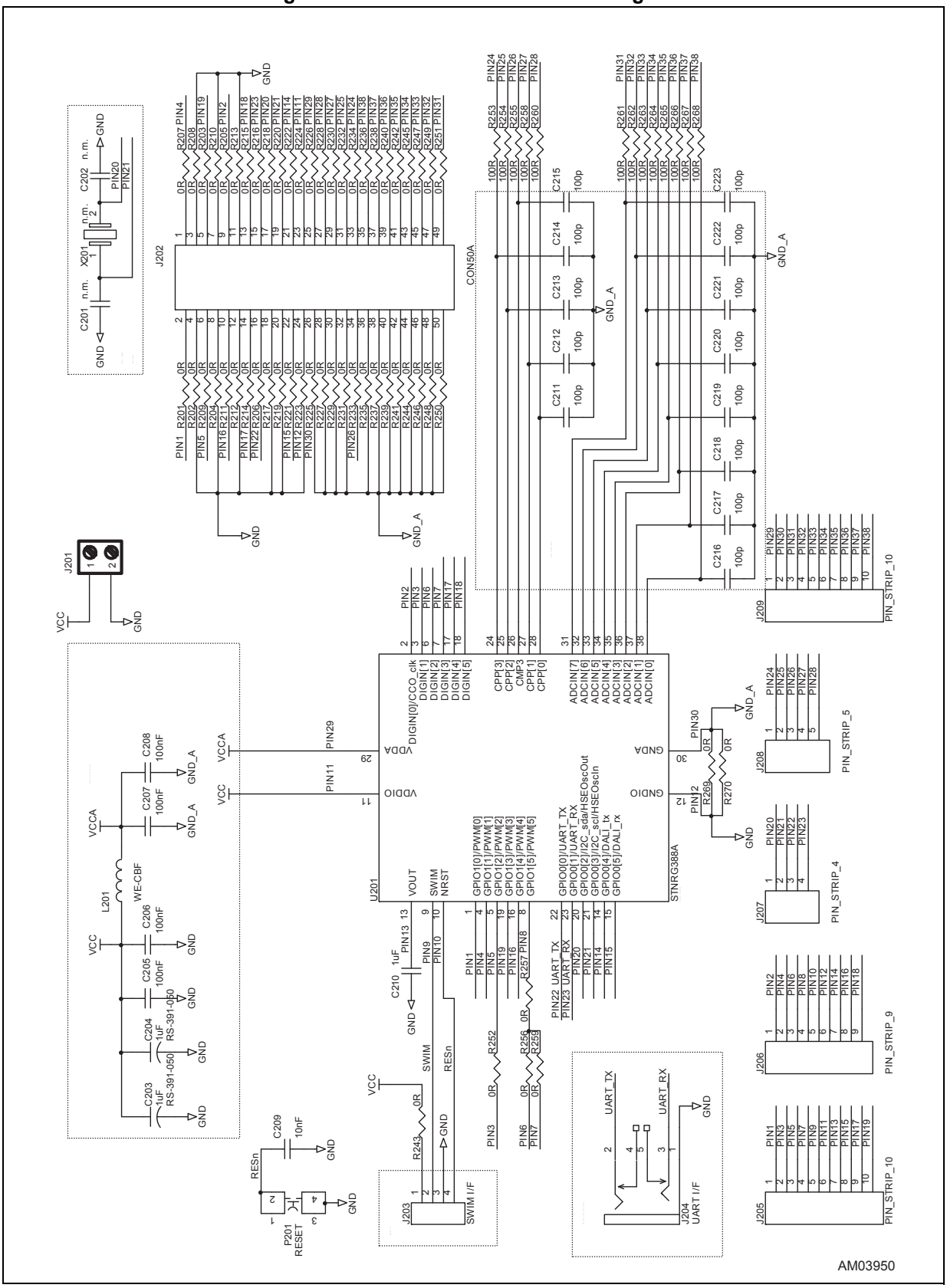


Figure 5. Control board schematic diagram



Revision history

Table 1. Document revision history

Date	Revision	Changes
14-May-2015	1	Initial release.

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