ACPL-P302/W302

0.4-Amp Output Current IGBT Gate Driver Optocouplers

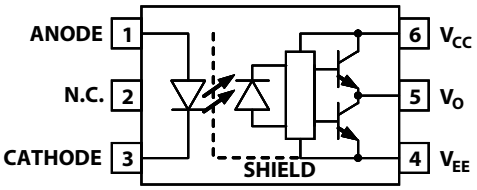
Data Sheet

Description

The ACPL-P302/W302 consists of a GaAsP LED optically coupled to an integrated circuit with a power output stage. These optocouplers are ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and current supplied by this optocoupler makes it ideally suited for directly driving small or medium power IGBTs.

Applications

- Isolated IGBT/Power MOSFET gate drive
- AC and brushless DC motor drives
- Industrial inverters
- Inverter for home appliances
- Induction cooker
- Switching Power Supplies (SPS)



Note: A 1 µF bypass capacitor must be connected between pins V_{CC} and V_{EE}.

Truth Table

LED	V_O
OFF	LOW
ON	HIGH

Features

- High speed response.
- Ultra high CMR.
- Bootstrappable supply current.
- Available in Stretched SO6 package
- Package Clearance/Creepage at 8 mm (ACPL-W302)
- Safety Approval:
  - UL1577 recognized with 3750V_{RMS} for 1 minute for ACPL-P302 and 5000V_{RMS} for 1 minute for ACPL-W302.
  - CSA Approved.
  - IEC/EN/DIN EN 60747-5-5 Approved

    V_{IORM} = 891V_{peak} for ACPL-P302

    V_{IORM} = 1140V_{peak} for ACPL-W302

Specifications

- 0.4A maximum peak output current
- 0.2A minimum peak output current
- 0.7 µs maximum propagation delay over temperature range
- I_{CC} (max.) = 3 mA maximum supply current
- 10 kV/µs minimum common mode rejection (CMR) at V_{CM} = 1000V
- Wide V_{CC} operating range: 10V to 30V over temperature range
- Wide operating temperature range: –40°C to 100°C

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.*

Ordering Information

ACPL-P302 is UL Recognized with 3750V_{RMS} for 1 minute per UL1577. ACPL-W302 is UL Recognized with 3750V_{RMS} for 1 minute per UL1577.

Part Number	Option RoHS Compliant	Package	Surface Mount	Tape and Reel	UL 5000V_{RMS}/ 1 minute rating	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-P302	-000E	Stretched SO-6	X				100 per tube
	-500E		X	X			1000 per reel
	-060E		X			X	100 per tube
	-560E		X	X		X	1000 per reel
ACPL-W302	-000E	Stretched SO-6	X		X		100 per tube
	-500E		X	X	X		1000 per reel
	-060E		X		X	X	100 per tube
	-560E		X	X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-P302-560E to order product of Stretched SO6 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Example 2:

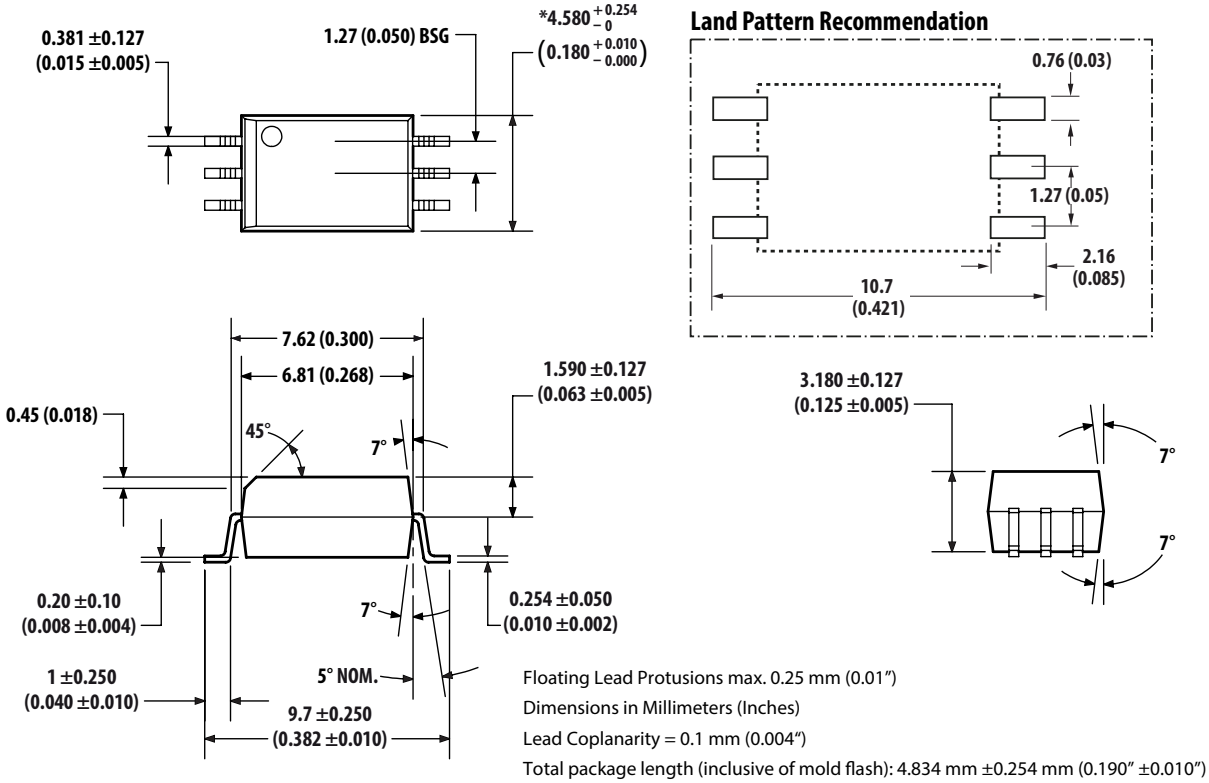
ACPL-P302-000E to order product of Stretched SO6 Surface Mount package in tube packaging and RoHS compliant.

Option datasheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since 15th July 2001 and RoHS compliant option will use '-XXXE'.

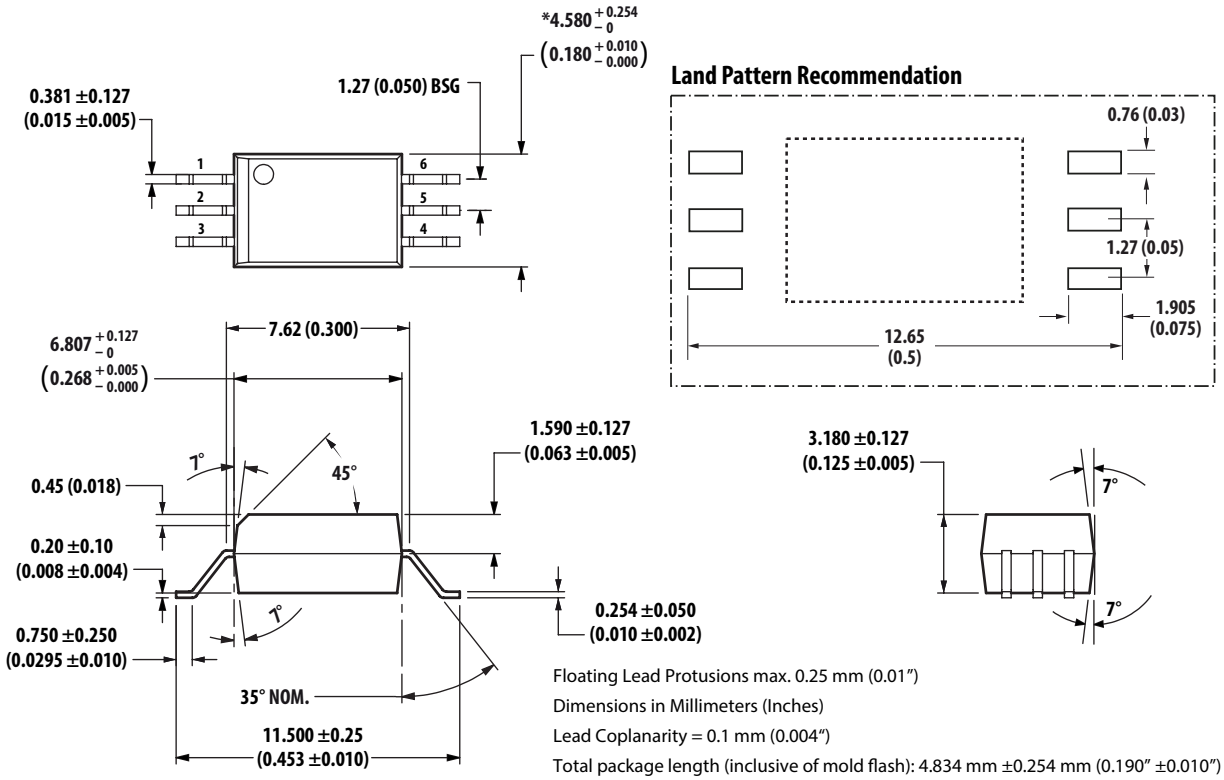
Package Outline Drawing

ACPL-P302 Stretched SO6 Package



Floating Lead Protusions max. 0.25 mm (0.01")
Dimensions in Millimeters (Inches)
Lead Coplanarity = 0.1 mm (0.004")
Total package length (inclusive of mold flash): 4.834 mm ±0.254 mm (0.190" ±0.010")

ACPL-W302 Stretched SO6 Package



Floating Lead Protusions max. 0.25 mm (0.01")
Dimensions in Millimeters (Inches)
Lead Coplanarity = 0.1 mm (0.004")
Total package length (inclusive of mold flash): 4.834 mm ±0.254 mm (0.190" ±0.010")

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The ACPL-P302/W302 is approved by the following organizations:

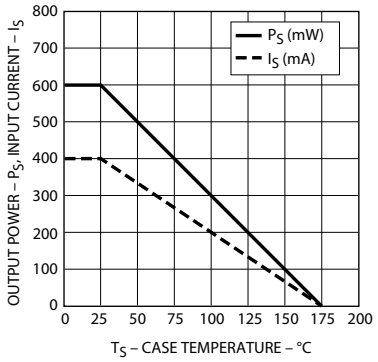
UL	Approval under UL 1577 component recognition program up to V_{ISO} = 3750V_{RMS} for the ACPL-P302 and V_{ISO} = 5000V_{RMS} for the ACPL-W302, File E55361.
CSA	CSA Component Acceptance Notice #5, File CA 88324
IEC/EN/DIN EN 60747-5-5 (Option 060 Only)	Approval under: IEC 60747-5-5:2007

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics* (Option 060)

Description	Symbol	ACPL-W302	ACPL-P302	Unit
Installation classification per DIN VDE 0110/39, Table 1 for rated mains voltage ≤ 150V_{RMS} for rated mains voltage ≤ 300V_{RMS} for rated mains voltage ≤ 450V_{RMS} for rated mains voltage ≤ 600V_{RMS} for rated mains voltage ≤ 1000V_{RMS}		 I-IV I-IV I-IV I-IV I-III	 I-IV I-IV I-III I-III	
Climatic Classification		55/100/21	55/100/21	
Pollution Degree (DIN VDE 0110/39)		2	2	
Maximum Working Insulation Voltage	V_{IORM}	1140	891	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} × 1.875 = V_{PR}, 100% Production Test with t_m =1 sec, Partial discharge < 5 pC	V_{PR}	2137	1670	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m =10 sec, Partial discharge < 5 pC	V_{PR}	1824	1426	V_{peak}
Highest Allowable Overvoltage* (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	8000	6000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure				
Case Temperature	T_S	175	175	°C
Input Current	$I_{S, INPUT}$	230	230	mA
Output Power	$P_{S, OUTPUT}$	600	600	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	≤10^9	≤10^9	Ω

* Refer to IEC/EN/DIN EN 60747-5-5 Optoisolator Safety Standard section of the Broadcom Regulatory Guide to Isolation Circuits, AV02-2041EN for a detailed description of Method a and Method b partial discharge test profiles.

** Refer to the following figure for dependence of P_S and I_S on ambient temperature.



Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-P302	ACPL-W302	Unit	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.0	8.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	8.0	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Minimum Internal Tracking (Internal Creepage)		N/A	N/A	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Note: All Broadcom data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered (the recommended Land Pattern does not necessarily meet the minimum creepage of the device). There are recommended techniques such as grooves and ribs which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	–55	+125	°C	
Operating Temperature	T_A	–40	+100	°C	
Average Input Current	$I_{F(AVG)}$		25	mA	1
Peak Transient Input Current (<1 µs pulse width, 300pps)	$I_{F(TRAN)}$		1.0	A	
Reverse Input Voltage	V_R		5	V	
High Peak Output Current	$I_{OH(PEAK)}$		0.4	A	2
Low Peak Output Current	$I_{OL(PEAK)}$		0.4	A	2
Supply Voltage	$V_{CC} – V_{EE}$	–0.5	35	V	
Output Voltage	$V_{O(PEAK)}$	–0.5	V_{CC}	V	
Output Power Dissipation	P_O		250	mW	3
Input Power Dissipation	P_I		45	mW	4
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane				
Solder Reflow Temperature Profile	See Package Outline Drawings section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Note
Power Supply	$V_{CC} – V_{EE}$	10	30	V	
Input Current (ON)	$I_{F(ON)}$	7	12	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	–3.6	0.8	V	
Operating Temperature	T_A	–40	100	°C	

Electrical Specifications (DC)

Over recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}	0.15			A	$V_O = V_{CC} - 4$		5
		0.2	0.3		A	$V_O = V_{CC} - 10$	2	2
Low Level Output Current	I_{OL}	0.15			A	$V_O = V_{EE} + 2.5$		5
		0.2	0.3		A	$V_O = V_{EE} + 10$	4	2
High Level Output Voltage	V_{OH}	$V_{CC} - 4$	$V_{CC} - 1.8$		V	$I_O = -100$ mA	1	6, 7
Low Level Output Voltage	V_{OL}		0.4	1	V	$I_O = 100$ mA	3	
High Level Supply Current	I_{CCH}		0.7	3	mA	$I_F = 10$ mA	5, 6	15
Low Level Supply Current	I_{CCL}		1.2	3	mA	$I_F = 0$ mA	5, 6	15
Threshold Input Current Low to High	I_{FLH}			6	mA	$I_O = 0$ mA, $V_O > 5V$	7, 13	
Threshold Input Voltage High to Low	V_{FHL}	0.8			V	$I_O = 0$ mA, $V_O > 5V$		
Input Forward Voltage	V_F	1.2	1.5	1.8	V	$I_F = 10$ mA	14	
Temperature Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T_A$		–1.6		mV/°C	$I_F = 10$ mA		
Input Reverse Breakdown Voltage	BV_R	5			V	$I_R = 10$ µA		
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, $V_F = 0V$		

Switching Specifications (AC)

Over recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	0.1	0.2	0.7	µs	$R_g = 75\Omega$, $C_g = 1.5$ nF, f = 10 kHz, Duty Cycle = 50%, $I_F = 7$ mA, $V_{CC} = 30V$	8, 9, 10, 11, 12, 15	14
Propagation Delay Time to Low Output Level	t_{PHL}	0.1	0.3	0.7	µs			14
Propagation Delay Difference Between Any Two Parts or Channels	PDD	–0.5		0.5	µs			11
Rise Time	t_R		50		ns			
Fall Time	t_F		50		ns			
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	10			kV/µs	$T_A = 25°C$, $V_{CM} = 1000V$	16	12
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	10			kV/µs		16	13

Package Characteristics

Parameter	Symbol	Device	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	ACPL-P302	3750			V_{rms}	T_A = 25°C, RH < 50% for 1 min.		8, 10
		ACPL-W302	5000						9, 10
Input-Output Resistance	R_{I-O}			10^{12}			V_{I-O} = 500V		10
Input-Output Capacitance	C_{I-O}			0.6		pF	Freq=1 MHz		

Notes:
1. Derate linearly above 70°C free air temperature at a rate of 0.3 mA/°C.
2. Maximum pulse width = 10 µs, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with I_O peak minimum = 0.2A. See Application section for additional details on limiting I_{OL} peak.
3. Derate linearly above 85°C, free air temperature at the rate of 4.0 mW/°C.
4. Input power dissipation does not require derating.
5. Maximum pulse width = 50 µs, maximum duty cycle = 0.5%.
6. In this test, V_{OH} is measured with a DC load current. When driving capacitive load V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.
7. Maximum pulse width = 1 ms, maximum duty cycle = 20%.
8. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 4500V_{RMS} for 1 second (leakage detection current limit I_{I-O} < 5 µA). This test is performed before 100% production test for partial discharge (method B) shown in the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table, if applicable.
9. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 6000V_{RMS} for 1 second (leakage detection current limit II-O < 5A). This test is performed before 100% production test for partial discharge (method B) shown in the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table, if applicable.
10. Device considered a two-terminal device: pins on input side shorted together and pins on output side shorted together.
11. PDD is the difference between t_{PHL} and t_{PLH} between any two parts or channels under the same test conditions.
12. Common mode transient immunity in the high state is the maximum tolerable |dV_{CM}/dt| of the common mode pulse V_{CM} to assure that the output will remain in the high state (i.e. V_O > 15.0 V).
13. Common mode transient immunity in a low state is the maximum tolerable |dV_{CM}/dt| of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e. V_O < 1.0 V).
14. This load condition approximates the gate load of a 1200 V/20 A IGBT.
15. The power supply current increases when operating frequency and Q_g of the driven IGBT increases.

Typical Performance Plots

Figure 1 V_{OH} vs. Temperature

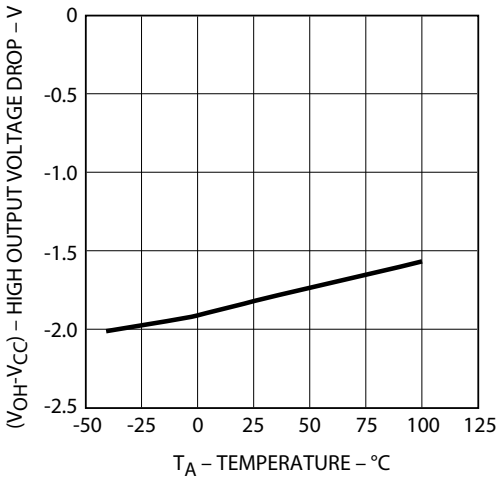


Figure 2 V_{OH} vs. I_{OH}

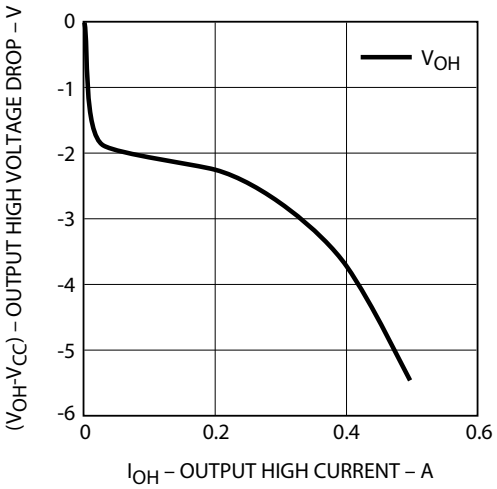


Figure 3 V_{OL} vs. Temperature

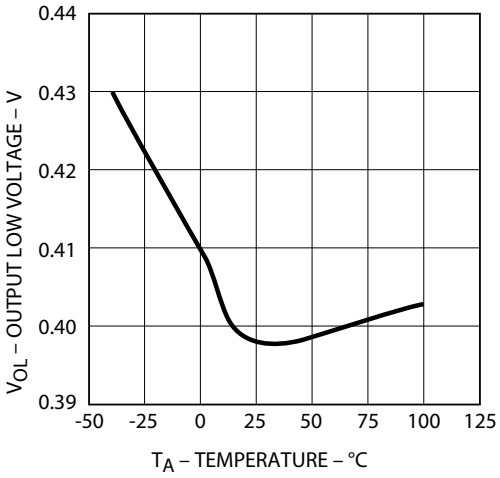


Figure 4 V_{OL} vs. I_{OL}

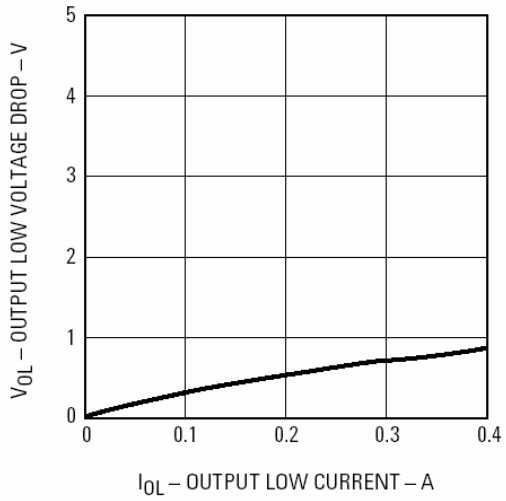


Figure 5 I_{CC} vs. Temperature

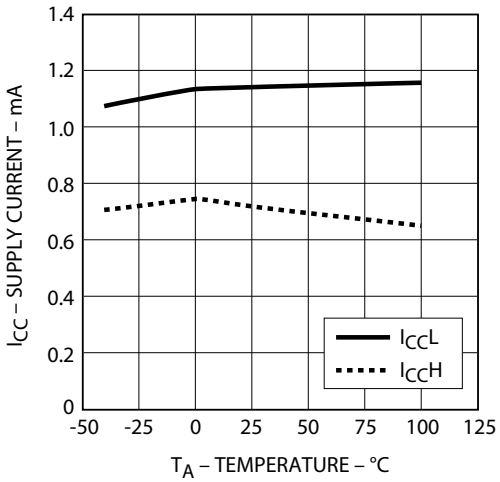


Figure 6 I_{CC} vs. V_{CC}

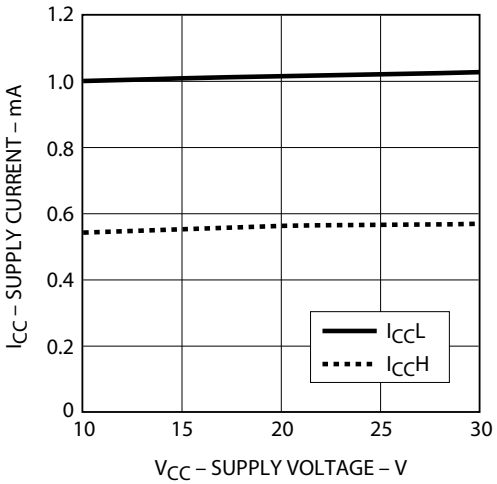


Figure 7 I_{FLH} vs. Temperature

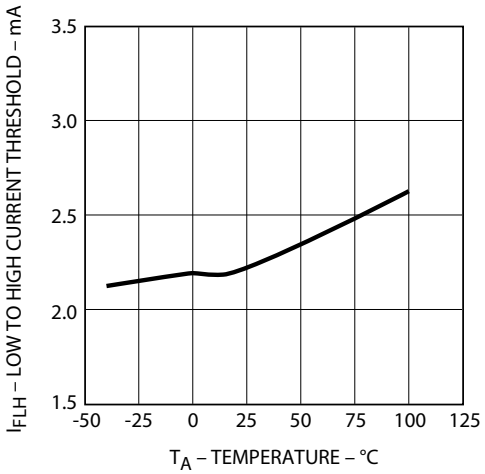


Figure 8 Propagation Delay vs. V_{CC}

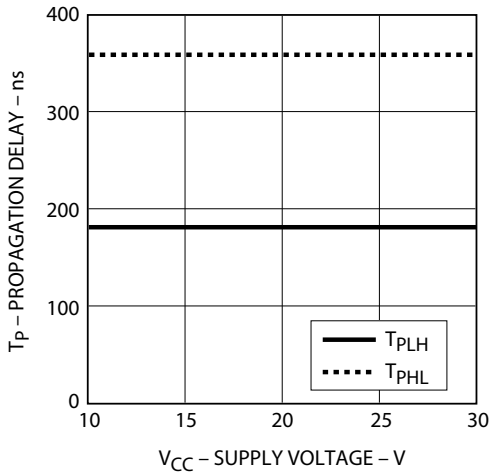


Figure 9 Propagation Delay vs. I_F

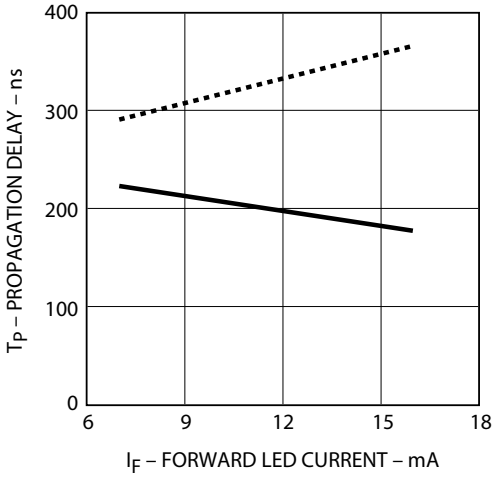


Figure 10 Propagation Delay vs. Temperature

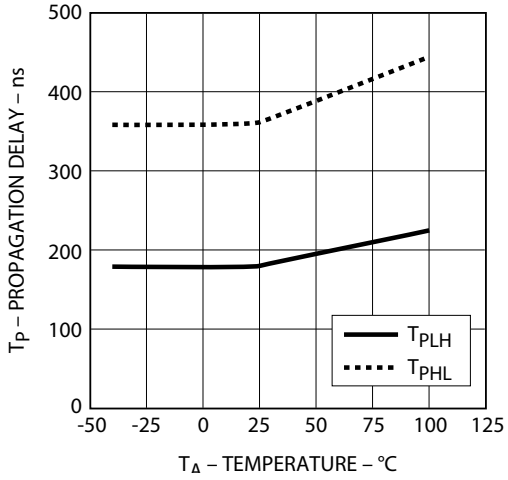


Figure 11 Propagation Delay vs. R_g

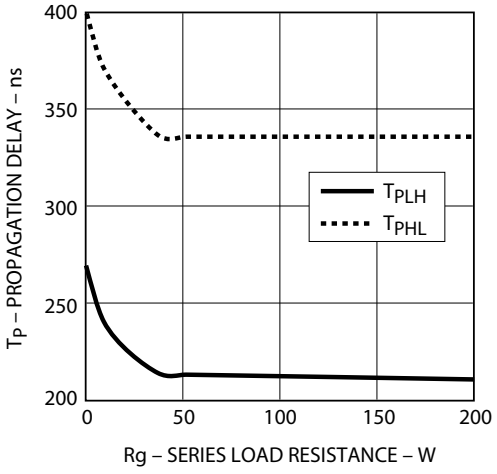


Figure 12 Propagation Delay vs. C_g

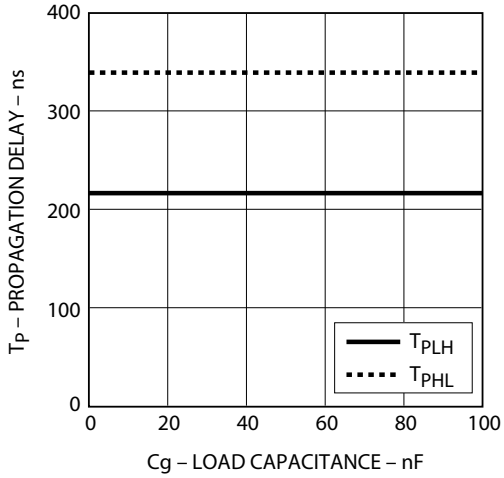


Figure 13 Transfer Characteristics

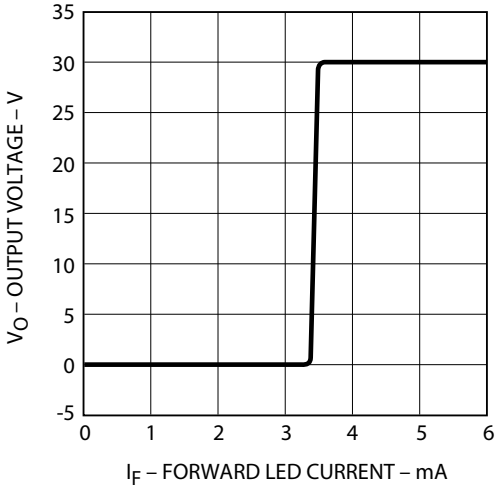


Figure 14 Input Current vs. Forward Voltage

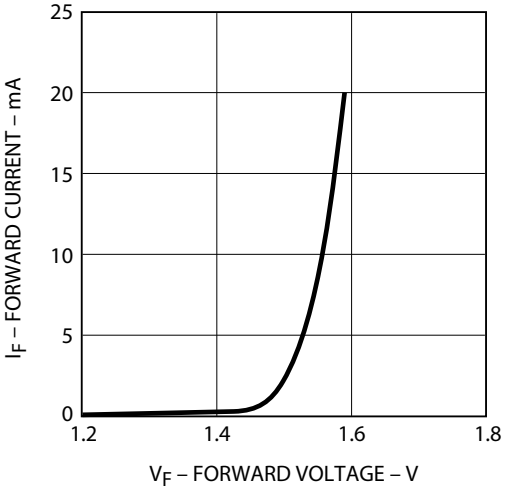


Figure 15 Propagation Delay Test Circuit and Waveforms

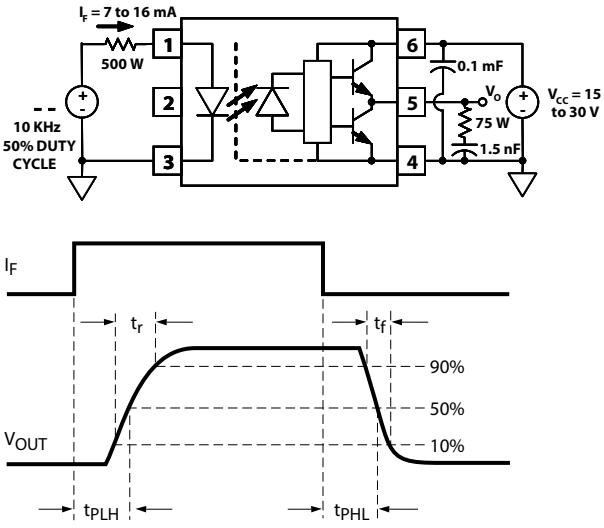
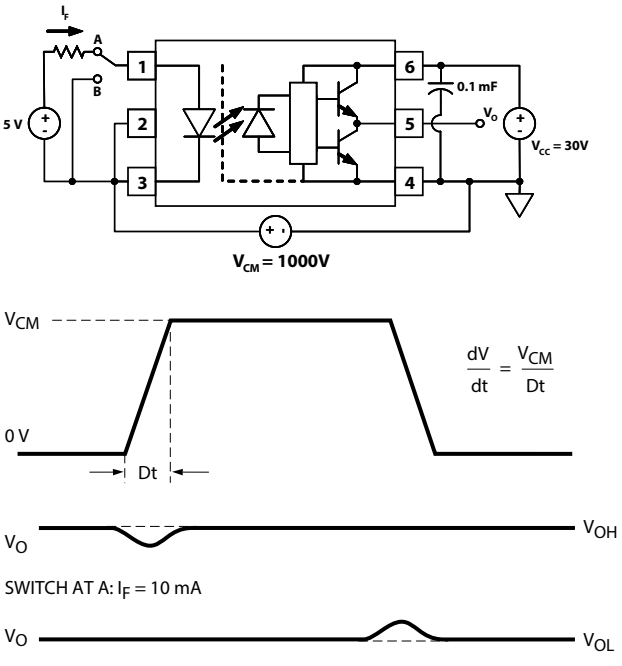


Figure 16 CMR Test Circuit and Waveforms



Applications Information

Eliminating Negative IGBT Gate Drive

To keep the IGBT firmly off, the ACPL-P302/W302 has a very low maximum V_{OL} specification of 1.0 V. Minimizing R_g and the lead inductance from the ACPL-P302/W302 to the IGBT gate and emitter (possibly by mounting the ACPL-P302/W302 on a small PC board directly above the IGBT) can eliminate the need for negative IGBT gate drive in many applications as shown in Figure 17. Care should be taken with such a PC board design to avoid routing the IGBT collector or emitter traces close to the ACPL-P302/W302 input as this can result in unwanted coupling of transient signals into the input of ACPL-P302/W302 and degrade performance. (If the IGBT drain must be routed near the ACPL-P302/W302 input, then the LED should be reverse biased when in the off state, to prevent the transient signals coupled from the IGBT drain from turning on the ACPL-P302/W302.

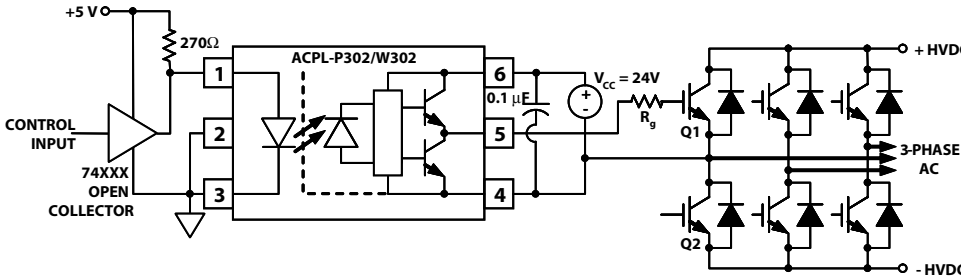
Selecting the Gate Resistor (Rg)

Step 1: Calculate R_g minimum from the I_{OL} peak specification. The IGBT and R_g in Figure 17 can be analyzed as a simple RC circuit with a voltage supplied by the ACPL-P302/W302.

The V_{OL} value of 1 V in the previous equation is the V_{OL} at the peak current of 0.4A. (See Figure 4).

$$R_g \geq \frac{V_{CC} - V_{OL}}{I_{OLPEAK}} = \frac{24 - 1}{0.4} = 57.5\ \Omega$$

Figure 17 Recommended LED Drive and Application Circuit for ACPL-P302/W302



Step 2: Check the ACPL-P302/W302 power dissipation and increase R_g if necessary. The ACPL-P302/W302 total power dissipation (P_T) is equal to the sum of the emitter power (P_E) and the output power (P_O).

$$P_T = P_E + P_O$$

$$P_E = I_F \bullet V_F \bullet DutyCycle$$

$$P_O = P_{O(BIAS)} + P_{O(SWITCHING)} = I_{CC} \bullet V_{CC} + E_{SW}(R_g; Q_g) \bullet f$$

$$= (I_{CCBIAS} + K_{ICC} \bullet Q_g \bullet f) \bullet V_{CC} + E_{SW}(R_g; Q_g) \bullet f$$

where $K_{ICC} \times Q_g \times f$ is the increase in I_{CC} due to switching and K_{ICC} is a constant of 0.001 mA/(nC*kHz). For the circuit in Figure 17 with I_F (worst case) = 10 mA, R_g = 57.5Ω, Max Duty Cycle = 80%, Q_g = 100 nC, f = 20 kHz and T_{AMAX} = 85°C:

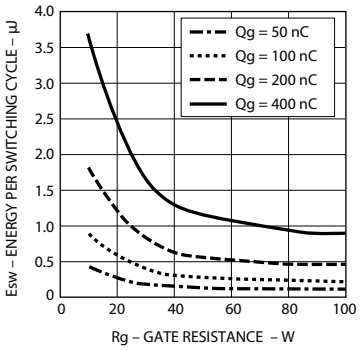
$$P_E = 10\ mA \bullet 1.8V \bullet 0.8 = 14\ mW$$

$$P_O = (3\ mA + (0.001\ mA/nC \bullet kHz) \bullet 20\ kHz \bullet 100\ nC) \bullet 24V + 0.3\ \mu J \bullet 20\ kHz = 126\ mW \leq 250\ mW\ (P_{O(MAX)} @ 85\ °C)$$

The value of 3 mA for I_{CC} in the previous equation is the max. I_{CC} over entire operating temperature range.

Since P_O for this case is less than $P_{O(MAX)}$, R_g = 57.5Ω is alright for the power dissipation.

Figure 18 Energy Dissipated for Each IGBT Switching Cycle



LED Drive Circuit Considerations for Ultra High CMR Performance

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 19. The ACPL-P302/W302 improves CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and optocoupler pins 5-8 as shown in Figure 20. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 17), can achieve 10 kV/µs CMR while minimizing component complexity.

Techniques to keep the LED in the proper state are discussed in the next two sections.

Figure 19 Optocoupler Input to Output Capacitance Model for Unshielded Optocouplers

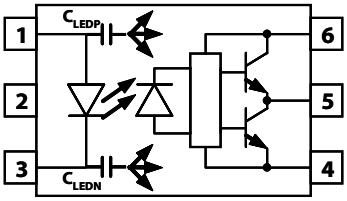
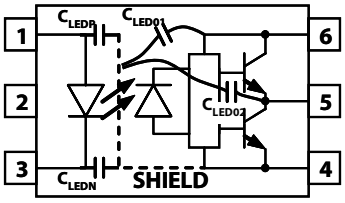


Figure 20 Optocoupler Input to Output Capacitance Model for Shielded Optocouplers



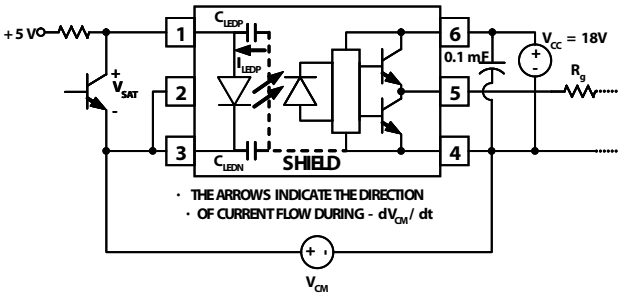
CMR with the LED On (CMR_H)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. A minimum LED current of 7 mA provides adequate margin over the maximum I_{FLH} of 5 mA to achieve 10 kV/µs CMR.

CMR with the LED Off (CMR_L)

A high CMR LED drive circuit must keep the LED off ($V_F \leq V_{F(OFF)}$) during common mode transients. For example, during a $-dV_{CM}/dt$ transient in Figure 21, the current flowing through C_{LEDP} also flows through the R_{SAT} and V_{SAT} of the logic gate. As long as the low state voltage developed across the logic gate is less than $V_{F(OFF)}$ the LED will remain off and no common mode failure will occur.

Figure 21 Equivalent Circuit for Figure 15 During CM Transient



The open collector drive circuit, shown in Figure 22, can not keep the LED off during a $+dV_{CM}/dt$ transient, since all the current flowing through C_{LEDN} must be supplied by the LED, and it is not recommended for applications requiring ultra high CMR_L performance. The alternative drive circuit which like the recommended application circuit (Figure 17), does achieve ultra high CMR performance by shunting the LED in the off state.

Figure 22 Not Recommended Open Collector Drive Circuit

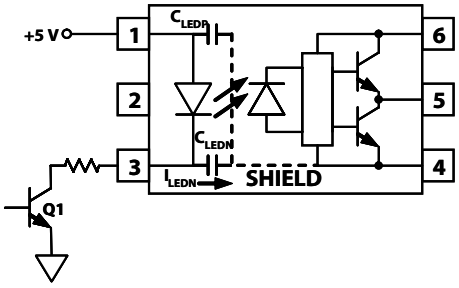
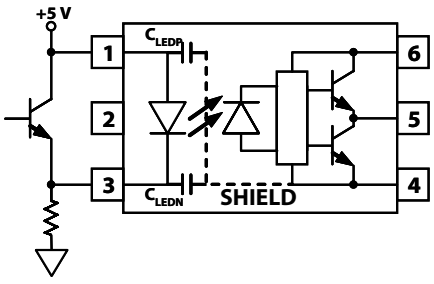


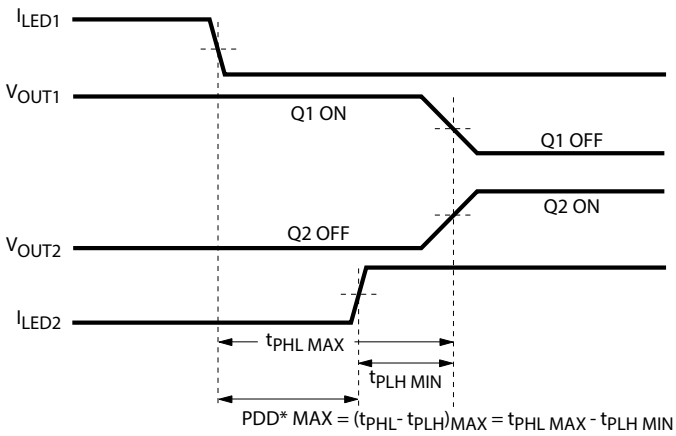
Figure 23 Recommended LED Drive Circuit for Ultra-High CMR Dead Time and Propagation Delay Specifications



Dead Time and Propagation Delay Specifications

The ACPL-P302/W302 includes a Propagation Delay Difference (PDD) specification intended to help designers minimize "dead time" in their power inverter designs. Dead time is the time high and low side power transistors are off. Any overlap in Ql and Q2 conduction will result in large currents flowing through the power devices from the high voltage to the low-voltage motor rails. To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 24. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDD max, which is specified to be 500 ns over the operating temperature range of -40° to 100°C.

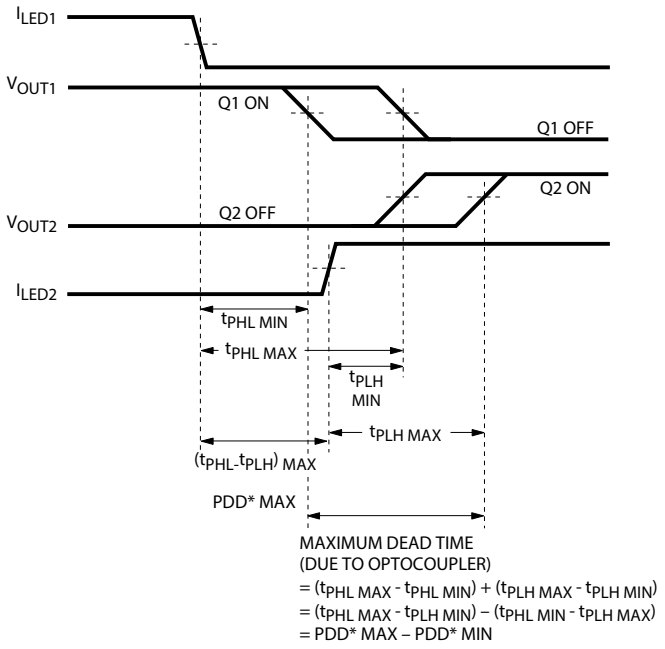
Figure 24 Minimum LED Skew for Zero Dead Time



*PDD = PROPAGATION DELAY DIFFERENCE
NOTE: FOR PDD CALCULATIONS THE PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specification as shown in Figure 25. The maximum dead time for the ACPL-P302/W302 is 1 µs (= 0.5 µs – (–0.5 µs)) over the operating temperature range of –40°C to 100°C.

Figure 25 Waveforms for Dead Time



Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.

Thermal Model for ACPL-P302/W302 Streched-SO6 Package Optocoupler

Definitions

- R_{11}: Junction to Ambient Thermal Resistance of LED due to heating of LED
- R_{12}: Junction to Ambient Thermal Resistance of LED due to heating of Detector (Output IC)
- R_{21}: Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of LED.
- R_{22}: Junction to Ambient Thermal Resistance of Detector (Output IC) due to heating of Detector (Output IC).
- P_1: Power dissipation of LED (W).
- P_2: Power dissipation of Detector / Output IC (W).
- T_1: Junction temperature of LED (˚C).
- T_2: Junction temperature of Detector (˚C).
- T_a: Ambient temperature.
- ΔT_1: Temperature difference between LED junction and ambient (˚C).
- ΔT_2: Temperature deference between Detector junction and ambient.

Ambient Temperature: Junction to Ambient Thermal Resistances were measured approximately 1.25 cm above optocoupler at ~23°C in still air.

Description

This thermal model assumes that an 6-pin single-channel plastic package optocoupler is soldered into a 7.62 cm x 7.62 cm printed circuit board (PCB). The temperature at the LED and Detector junctions of the optocoupler can be calculated using the equations below.

$$T_1 = (R_{11} \times P_1 + R_{12} \times P_2) + T_a \quad \text{-- (1)}$$

$$T_2 = (R_{21} \times P_1 + R_{22} \times P_2) + T_a \quad \text{-- (2)}$$

Jedec Specifications	R_{11}	R_{12}, R_{21}	R_{22}
low K board	357	150, 166	228
high K board	249	76, 79	159

Notes:
1. Maximum junction temperature for above parts: 125 °C.

For product information and a complete list of distributors, please go to our web site:
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AV02-0157EN – May 5, 2017

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product