CMX90G301 1.4 – 7.1GHz Positive Gain-Slope Amplifier +1dB

Description

The CMX90G301 is a low-power 50 Ω cascadable MMIC gain block suitable for a wide variety of wireless applications operating in the 1.4 – 7.1 GHz frequency range.

The gain block has a positive gain-slope of +1dB across the band, eliminating the need for equalisation and compensates for increasing system losses with frequency.

CMX90G301 is highly integrated for ease of use, minimising component count and board area. RF ports are matched on-chip to 50 Ω with DC-blocking capacitors. An active bias circuit allows the device to operate over a wide supply voltage of 2.7V to 5V with typical current of 22 mA.

Using GaAs pHEMT to provide a combination of low DC power, low noise and high gain.

An alternative part, CMX90G302, is available for applications that require more gain-slope compensation.

3x3mm VQFN-16 Package

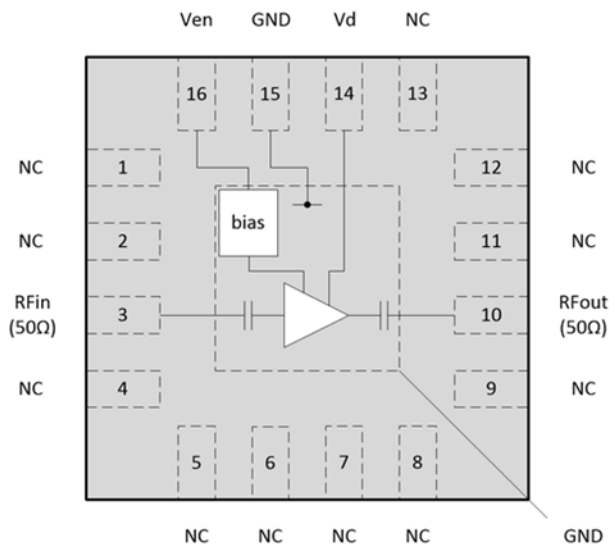
Product Features

- Wide frequency range 1.4 – 7.1 GHz
- Positive gain-slope +1dB
- Small signal gain 14.8 – 16.0 dB
- Single positive DC supply 2.7 – 5 V
- Low noise figure 2 dB
- Input and output matched to 50 Ω
- Output P1dB +11.5 dBm @3.5 GHz
- 1.8 V logic compatible enable
- 105°C operating temperature

Applications

- Tx and Rx systems
- 4G / 5G wireless infrastructure
- TDD and FDD
- IF amplifier
- License-free bands
- General purpose gain block
- Eliminate passive equaliser

Block Diagram



Ordering Information

Part Number	Description
CMX90G301QF-R710	7” Reel with 1,000 pieces
CMX90G301QF-R330	13” Reel with 3,000 pieces
EV90G301	Evaluation board

Absolute Maximum Ratings

Parameter	Rating
RF Input Power	+10dBm
Device Voltage (Vd, Ven)	+5.5V
Case Temperature (Tc)	-40 to +105 °C
Junction Temperature (Tjmax)	165 °C (MTTF = 10^6 hours)
Storage Temperature	-40 to +125 °C
ESD Sensitivity	HBM >175V (Class 0B), CDM >750V (Class C2b)
MSL Level	Level 3

Exceeding the maximum ratings may result in damage or reduced device reliability.

Thermal Characteristics

Parameter	Rating
Thermal Resistance (Rjc)	424 °C/W (Tc = 85˚C) 448 ˚C/W (Tc = 105 ˚C)

Thermal resistance is junction-to-case, where case refers to the exposed die pad on the backside which is in contact with the board.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Operating Frequency Range	1.4		7.1	GHz
Case Temperature (Tc)	-40		+105	°C
Device Voltage (Vd)	2.7		5	V
Enable Voltage (Ven)	0		5	V

The device will be tested under certain conditions, but performance is not guaranteed over the full range of recommended operating conditions.

ESD Caution

CMX90G301 incorporates ESD protection circuitry however ESD precautions are strongly recommended for handling and assembly. Ensure that devices are protected from ESD in antistatic bags or carriers when being transported. Personal grounding is to be worn at all times when handling these devices.

RoHS Compliance

All devices supplied by CML Microcircuits are compliant with RoHS directive (2011/65/EU), containing less than the permitted levels of hazardous substances

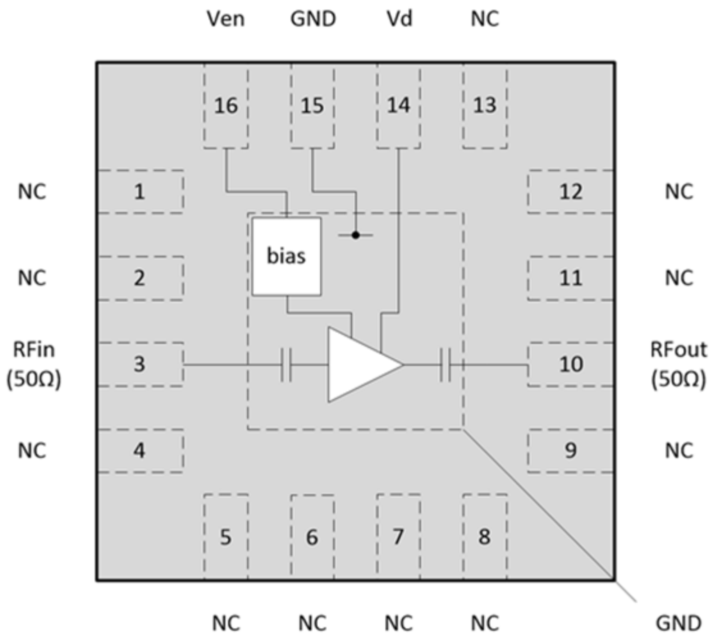
Electrical Specification

Results taken on the EV90A301 EVB, board losses have been de-embedded using the calibration line on the EV90G301.

Zo = 50 Ω, Vd = +5 V, Ven = +5 V, Ta = +25 °C (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Frequency		1.4		7.1	GHz
Small Signal Gain	1.4 GHz		14.8		dB
Small Signal Gain	3.5 GHz		15.3		dB
Small Signal Gain	7.1 GHz		16.0		dB
Gain Slope	1.4 GHz to 7.1 GHz		+1		dB
Reverse Isolation	1.4 GHz to 7.1 GHz		20		dB
P1dB	At 3.5 GHz		11.5		dBm
OIP3	Two-tone test Δf = 10 MHz, at 3.5 GHz, Pin/Tone = -20dBm	-	21	-	dBm
Noise Figure	3.5GHz		1.9		dB
Input Return Loss	1.4 GHz to 7.1 GHz		>10		dB
Output Return Loss	1.4 GHz to 7.1 GHz		>12		dB
Device Current (Id)			22		mA
Ven (Logic 1 = Enabled)	Amplifier normal operation	1.8		5	V
Ven (Logic 0 = Standby)	Amplifier in standby mode	0		0.2	V
Id	Ven = 0 V		<1		uA
Id	Ven = 0.2 V		8		uA
S21	Ven = 0 to 0.2 V		-15		dB
Ven Current (Ien)	Ven = 5 V		0.8		mA
Turn-On Time	RFin = TBC dBm		TBD		ns
Turn-Off Time	RFin = TBC dBm		TBD		ns

Pin Assignments



Top View

Pin	Name	Description
1	NC	Connect to GND
2	NC	Connect to GND
3	RFin	RF input. Internally matched to 50 Ω with integrated DC-blocking capacitor.
4	NC	Connect to GND
5	NC	Connect to GND
6	NC	Connect to GND
7	NC	Connect to GND
8	NC	Connect to GND
9	NC	Connect to GND
10	RFout	RF output. Internally matched to 50 Ω with integrated DC-blocking capacitor.
11	NC	Connect to GND
12	NC	Connect to GND
13	NC	Connect to GND
14	Vd	Voltage supply to amplifier
15	GND	Connect to GND
16	Ven	Amplifier enable input
Die pad	GND	DC and RF ground. Exposed die pad must be connected to GND.

Notes
CML recommends that all no connect (NC) pins are connected to ground.
The bottom exposed die pad must be connected to the ground plane on the board.

Typical Performance

The following plots show typical performance characteristics of CMX90G301 measured on the evaluation board (Part Number EV90G301). Board losses have been de-embedded from the measurement results using the through line that is included on the EV90G301.

Test conditions unless otherwise noted:-
Vd = Ven = 5.0 V, Ta = 25 ˚C, Z0 = 50 Ω

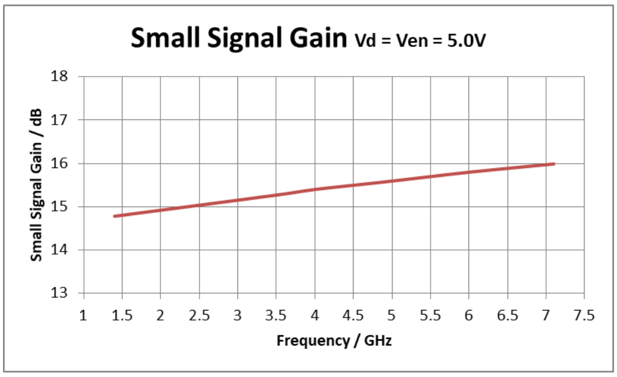


Figure 1: Small Signal Gain Vd = Ven = 5.0V

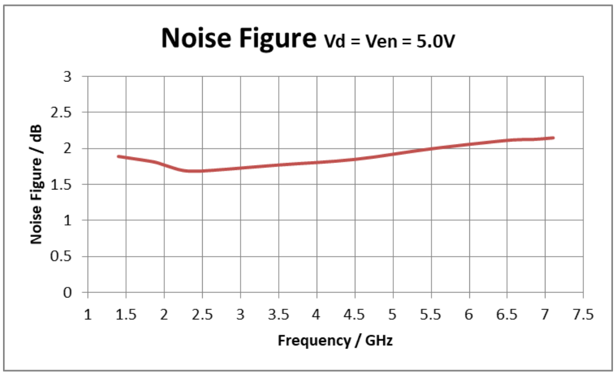


Figure 2: Noise Figure Vd = Ven = 5.0V

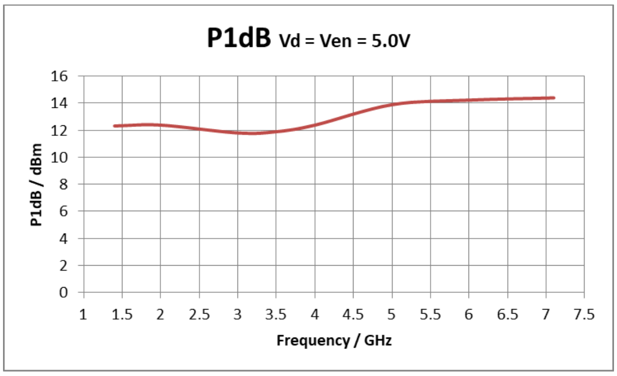


Figure 3: P1dB Vd = Ven = 5.0V

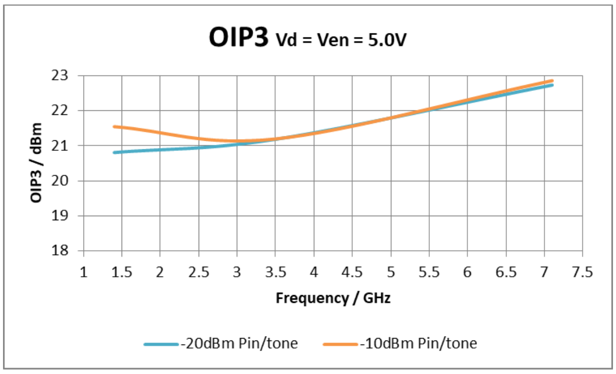


Figure 4: OIP3 Vd = Ven = 5.0V

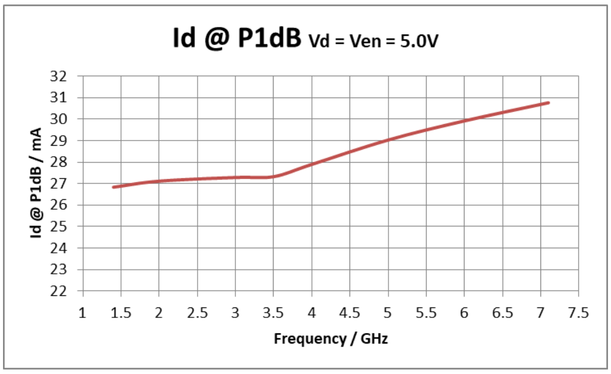


Figure 5: Id @P1dB Vd = Ven = 5.0V

Test conditions unless otherwise noted:-
Vd = Ven = 5.0 V, Z0 = 50 Ω

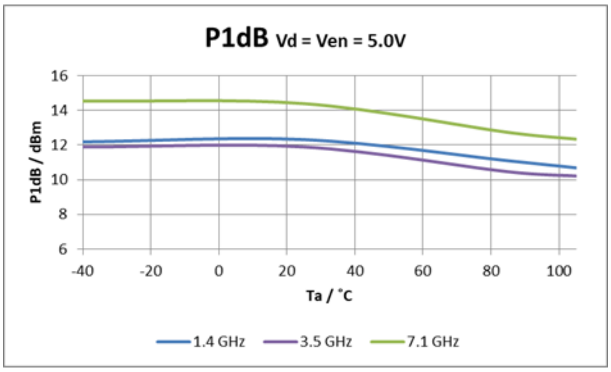


Figure 6: P1dB Vd = Ven = 5.0V

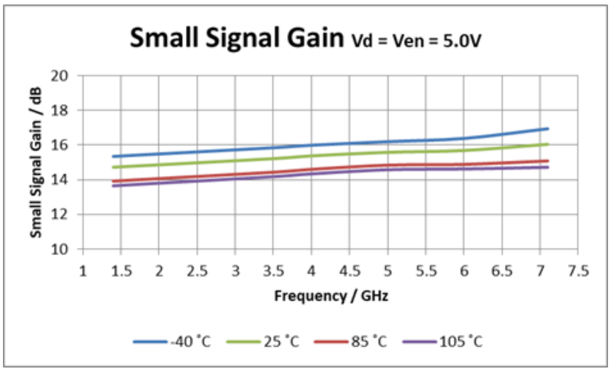


Figure 7: Small Signal Gain Vd = Ven = 5.0V

Test conditions unless otherwise noted:-
Vd = 5.0 V, Ta = 25 ˚C, Z0 = 50 Ω

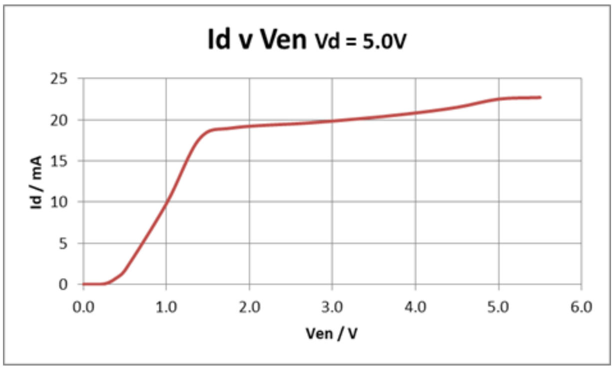


Figure 8: Id v Ven Vd = 5.0V

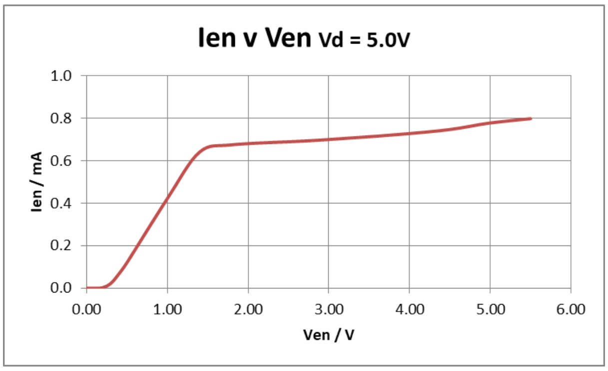


Figure 9: Ien v Ven Vd = 5.0V

Test conditions unless otherwise noted:-
Vd = 5.0 V, Z0 = 50 Ω

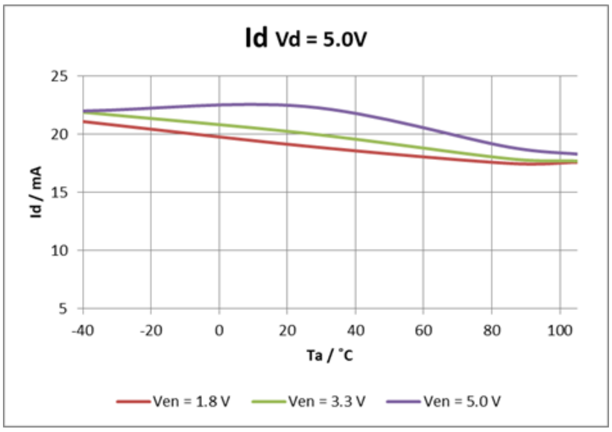


Figure 10: Id Vd = 5.0V

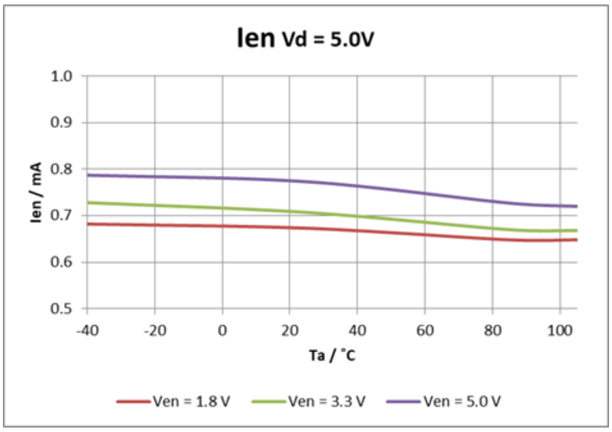


Figure 11: Ien Vd = 5.0V

Test conditions unless otherwise noted:-
Vd = Ven = 5.0 V, Ta = 25 ˚C, Z0 = 50 Ω

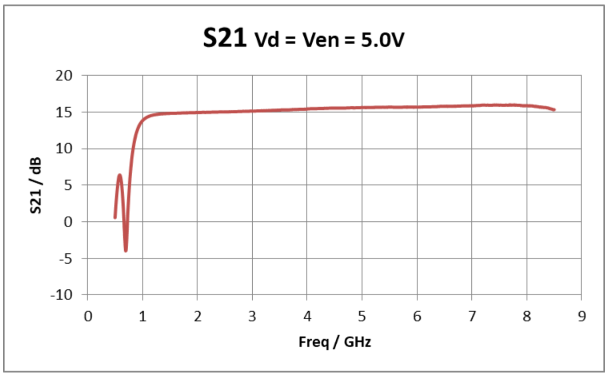


Figure 12: S21 Vd = Ven = 5.0V

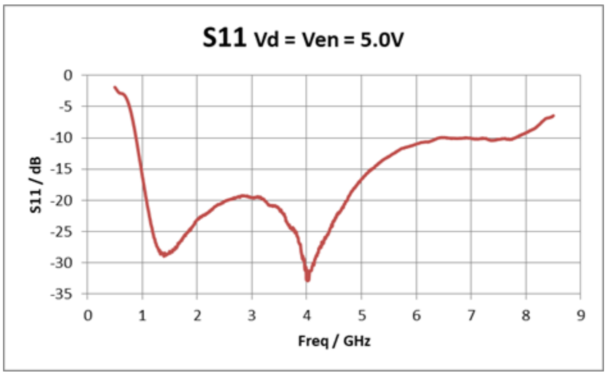


Figure 13: S11 Vd = Ven = 5.0V

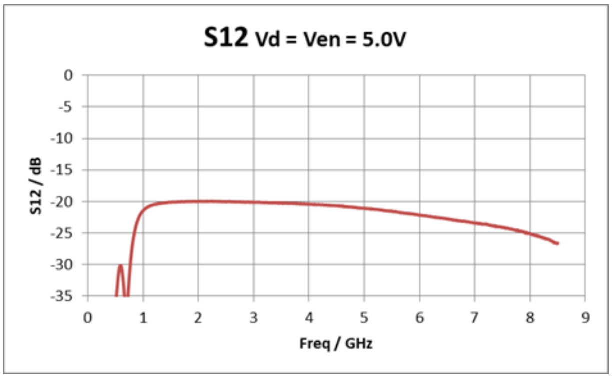


Figure 14: S12 Vd = Ven = 5.0V

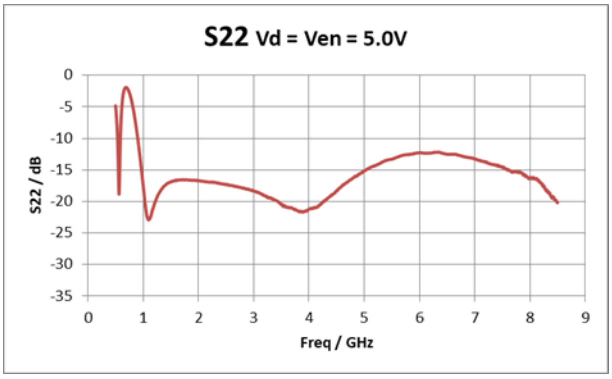


Figure 15: S22 Vd = Ven = 5.0V

Test conditions unless otherwise noted:-
Vd = Ven = 3.3V, Ta = 25 ˚C, Z0 = 50 Ω

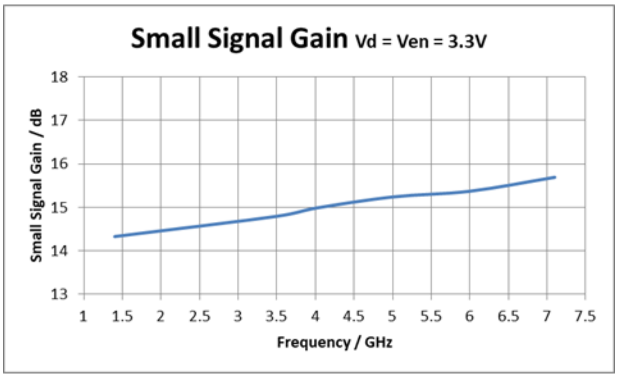


Figure 16: Small Signal Gain Vd = Ven = 3.3V

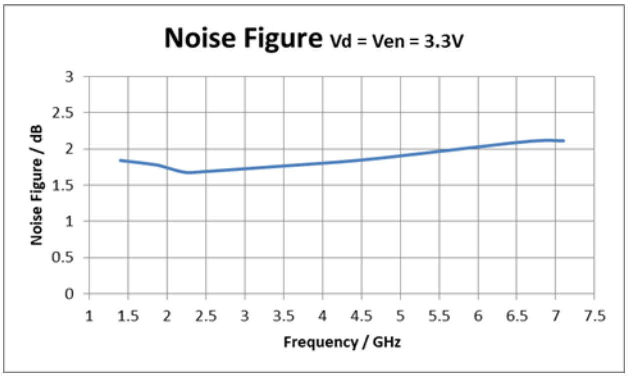


Figure 17: Noise Figure Vd = Ven = 3.3V

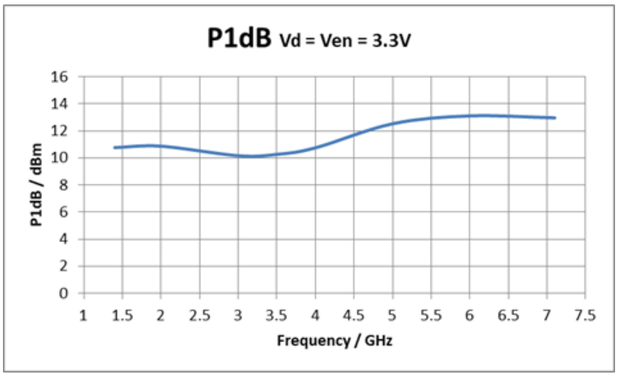


Figure 18: P1dB Vd = Ven = 3.3V

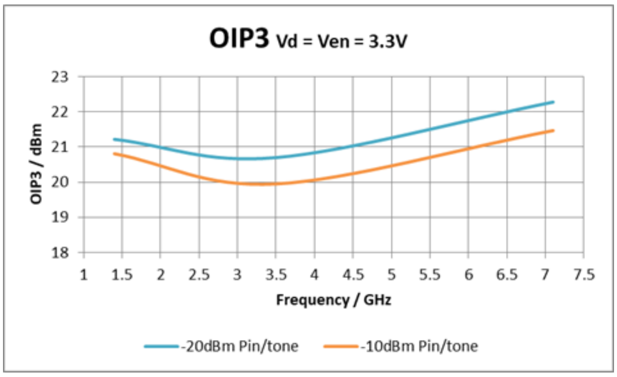


Figure 19: OIP3 Vd = Ven = 3.3V

Test conditions unless otherwise noted:-
Vd = Ven = 3.3 V, Z0 = 50 Ω

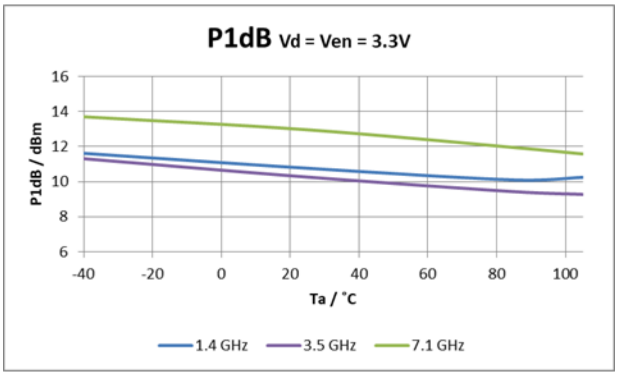


Figure 20: P1dB Vd = Ven = 3.3V

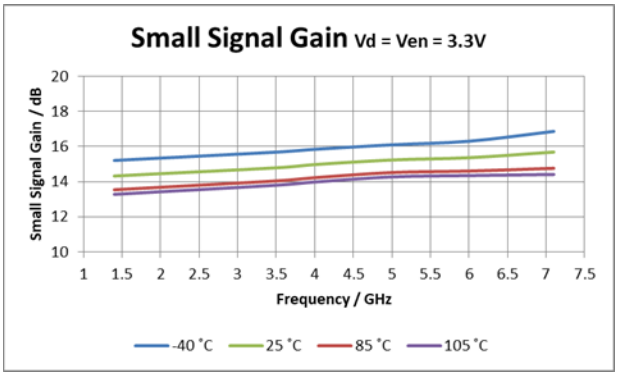


Figure 21: Small Signal Gain Vd = Ven = 3.3V

Test conditions unless otherwise noted:-
Vd = 3.3 V, Ta = 25°C, Z0 = 50 Ω

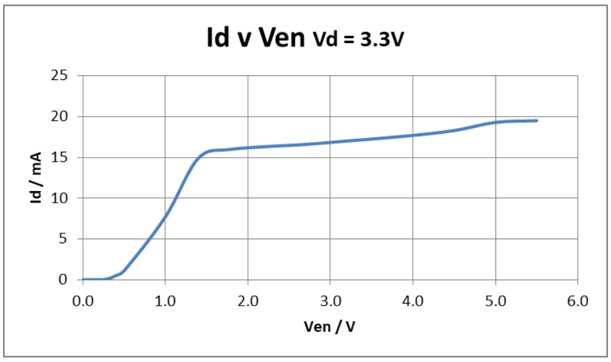


Figure 22: Id v Ven Vd = 3.3V

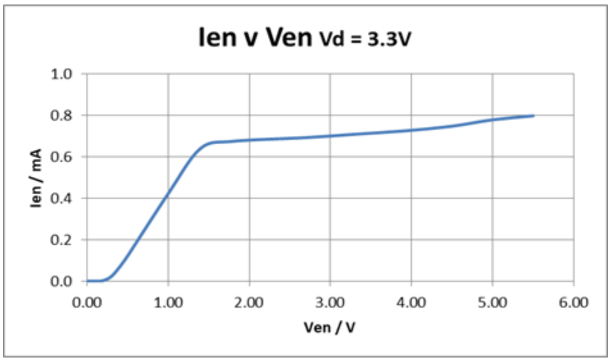


Figure 23: Ien v Ven Vd = 3.3V

Test conditions unless otherwise noted:-
Vd = 3.3 V, Z0 = 50 Ω

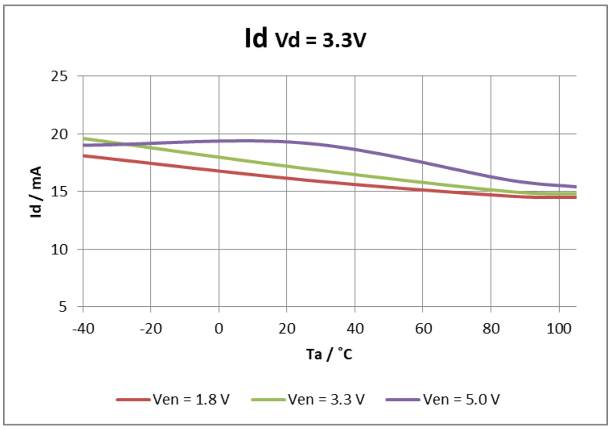


Figure 24: Id Vd = 3.3V

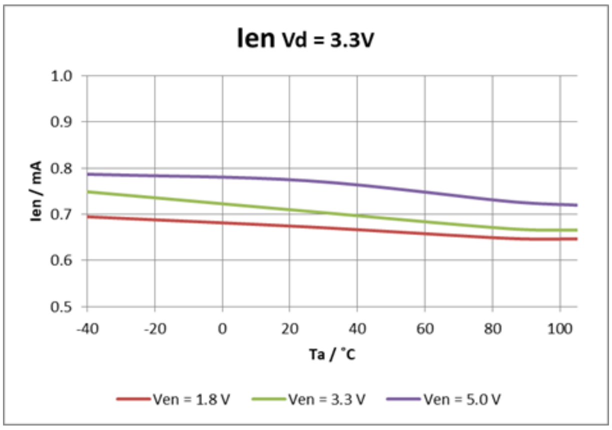


Figure 25: Ien Vd = 3.3V

Test conditions unless otherwise noted:-
Vd = Ven = 3.3 V, Ta = 25 ˚C, Z0 = 50 Ω

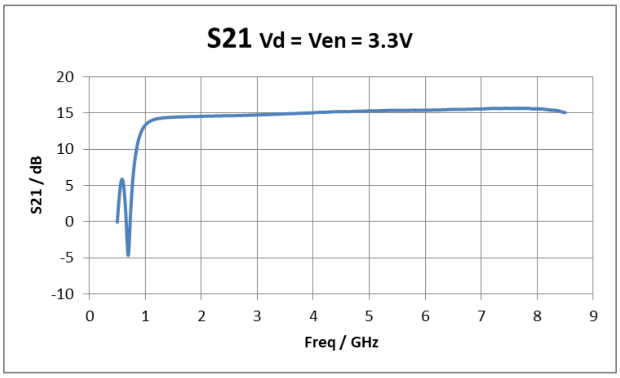


Figure 26: S21 Vd = Ven = 3.3V

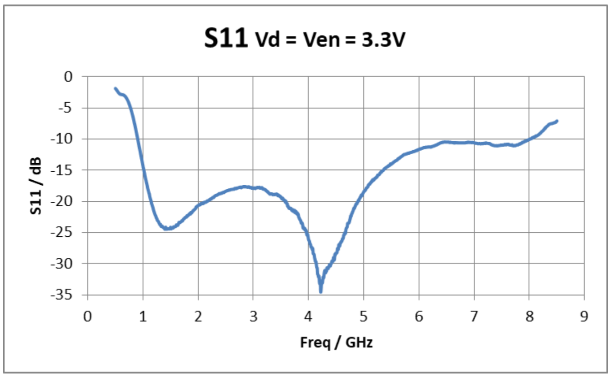


Figure 27: S11 Vd = Ven = 3.3V

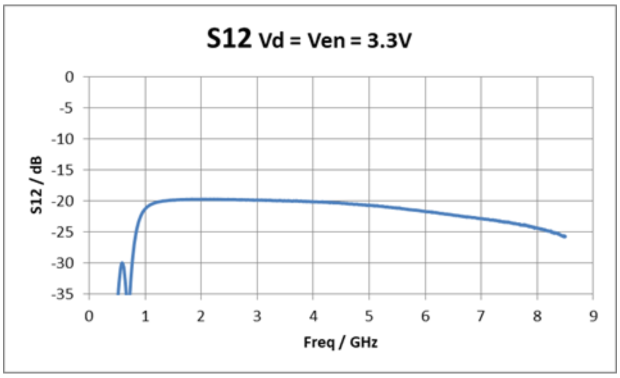


Figure 28: S12 Vd = Ven = 3.3V

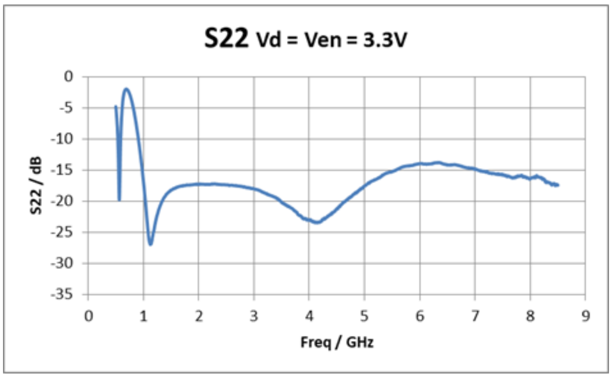


Figure 29: S22 Vd = Ven = 3.3V

Test conditions unless otherwise noted:-
Ta = 25 ˚C, Z0 = 50 Ω

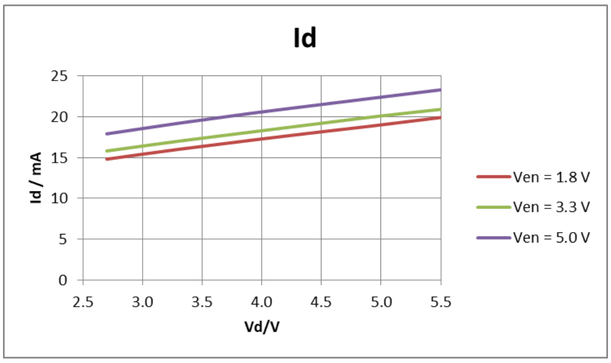


Figure 30: Id

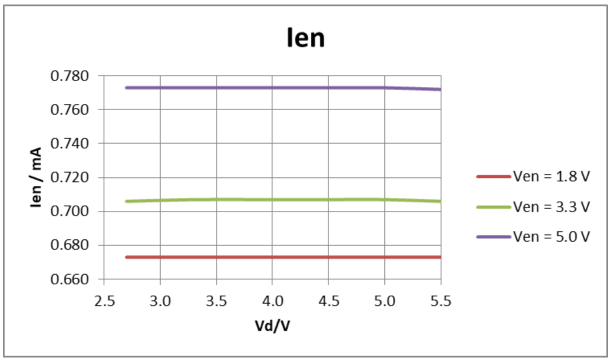


Figure 31: Ien

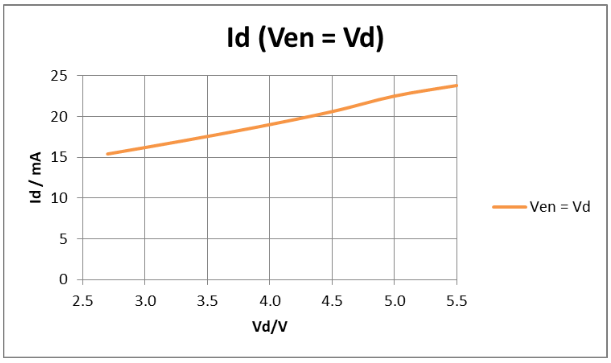


Figure 32: Id (Ven = Vd)

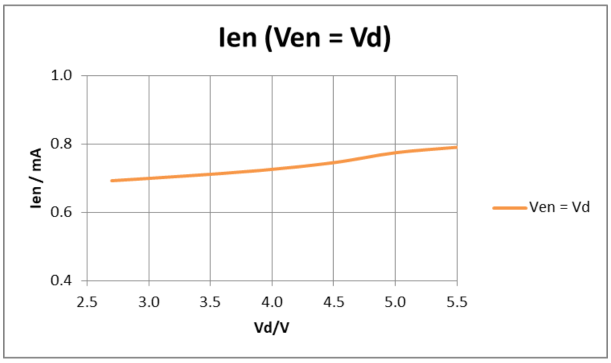


Figure 33: Ien (Ven = Vd)

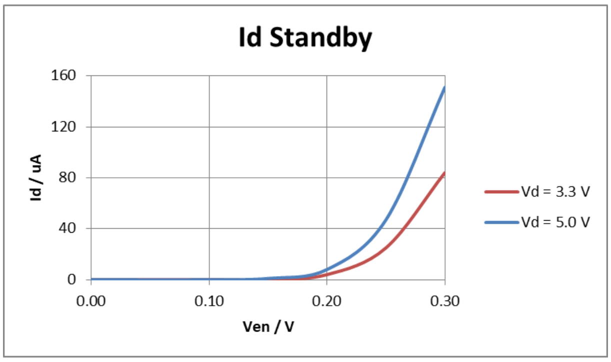


Figure 34: Id Standby

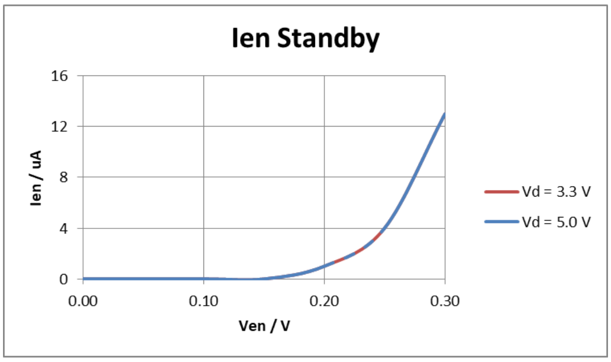


Figure 35: Ien Standby

Application Information

Schematic Diagram

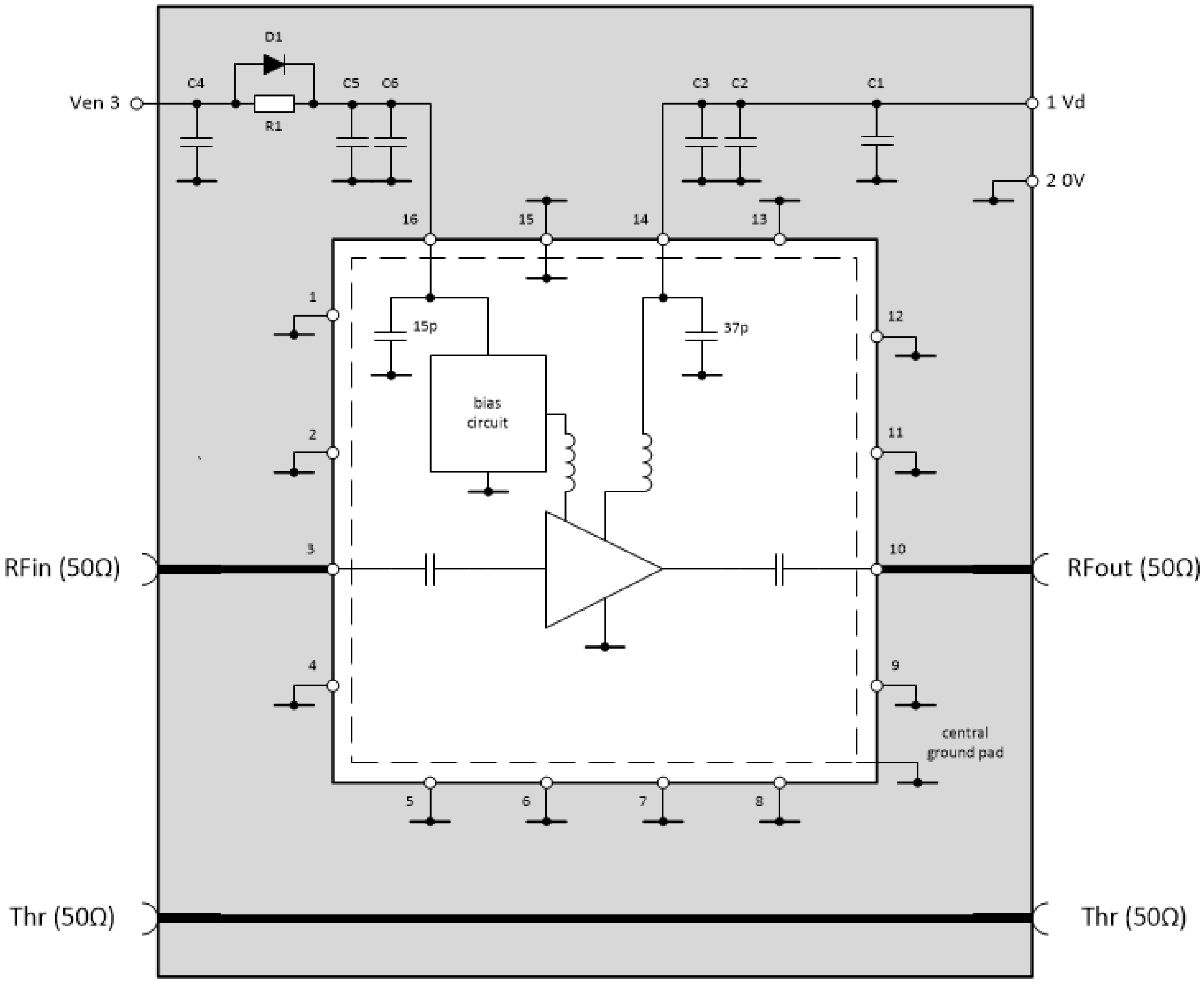


Figure 31: EV90G301 Schematic

Bill Of Materials (BOM)

Reference Designator	Value	Size	Description
C1	1 uF	0603	16V, +/- 10 %
C2	10 nF	0402	16V, +/- 10%
C3	DNF	0402	
C4	10 nF	0402	16V, +/- 10%
C5	1nF	0402	25V, +/- 5%
C6	DNF	0402	
R1	0R	0402	0.063W
D1	DNF	SOD-523F	

Notes

- DNF = Do not fit component

PCB Layout

Careful layout of the printed circuit board (PCB) is essential for optimum RF and thermal performance. The recommended layout, including ground via pattern underneath the device, may be taken from the evaluation board (Part Number EV90G301).

The PCB consists of a top layer of R04350 backed by 2 layers of FR-4 with a total thickness of 1.606 mm (Figure 32) and the EV90G301 PCB (Figure 33) is 20 mm x 45 mm. The coplanar RF transmission lines have a width of 0.525 mm with a gap of 0.27 mm to ground either side. The through line length has been reduced by 3mm to account for the length of the device.

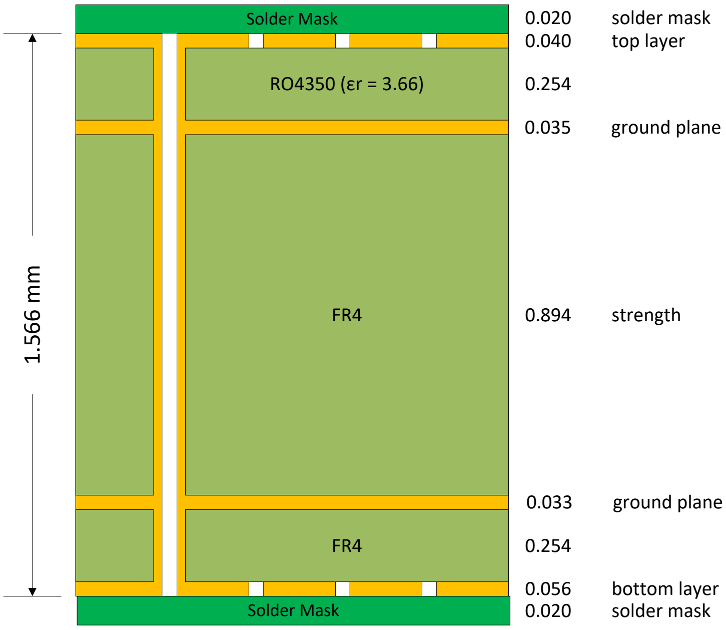


Figure 32: EV90G301 Layer Stack

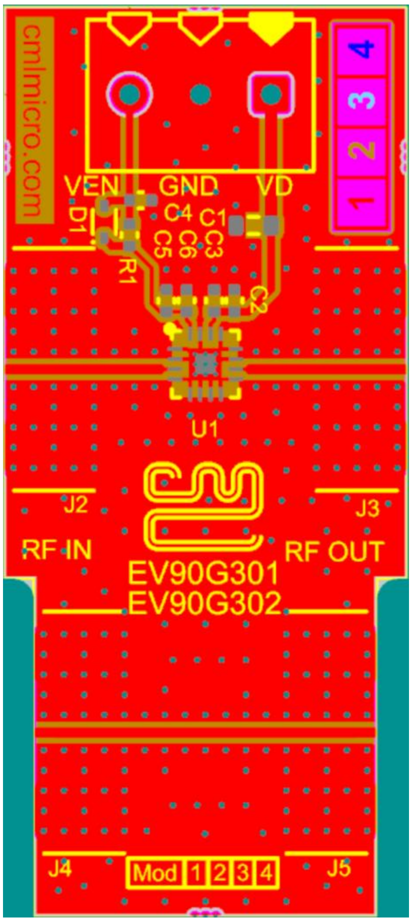


Figure 33: EV90G301 PCB Top Layer View

Thermal Design

The primary RF/DC ground and thermal path is via the exposed die pad on the backside of the package, which must be connected to the PCB ground plane. An array of plated through-hole vias directly underneath the die pad area is essential to conduct heat away and minimise ground inductance. A typical solution will have 9 grounding vias connecting the top layer to the bottom layer, with inner diameter of 0.2 mm (and 0.025 mm plating) on 0.5 mm grid pattern. The vias do not need to be filled. The PCB layout should provide a thermal radiator appropriate for the intended operation, adding as much copper to inner and outer layers as possible to avoid excessive junction temperature.

Device junction temperature (Tj) can be calculated using Tj = Tc + (Pdiss x Rjc) where Pdiss = Pdc + Pin – Pout and Tc is the case temperature on the backside of the package (die pad) in contact with the PCB.

Ven Input

The device is enabled by applying a voltage between 1.8 V and 5.0 V to pin 16 (Ven). The resulting Id taken by the device is relatively independent of the Ven voltage applied. If the enable feature is not required, the Ven pin can be connected to the same voltage as Vd.

The device can be placed into standby mode when not in use by setting Ven low (<0.2V) to disable all circuitry.

If lower Ien and Id leakage current and/or if the highest forward isolation is needed in standby mode, a diode can be used in series with the Ven pin to increase the switch-on threshold of the device. This can be particularly important at elevated temperatures. Some suggested diodes in suitable packages (SOD-523F) for the evaluation board are:

- 1N914BWT-D PN fast switching diode
- BAT43XV2-D Schottky diode

Evaluation Board & Bias Procedure

In general, sequencing of the Vd and Ven supplies is not necessary however applying Vd before or simultaneously with Ven is recommended.

The separate through line can be used to measure the evaluation board and connector losses. These results can then be used to de-embed the device performance from evaluation board measurements.

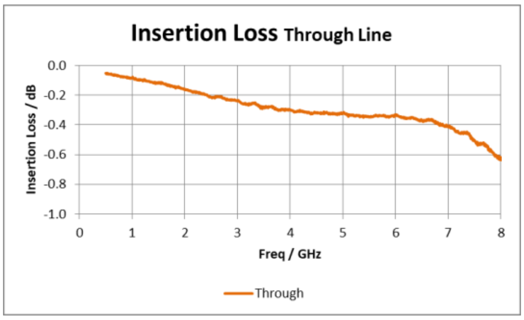


Figure 34: Insertion Loss – through line

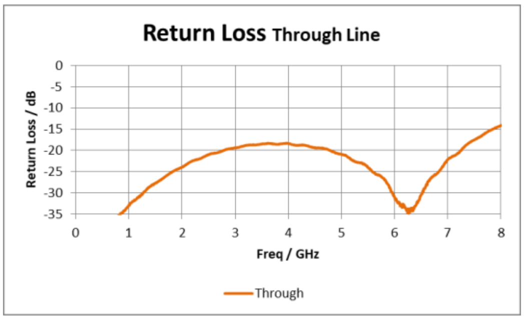
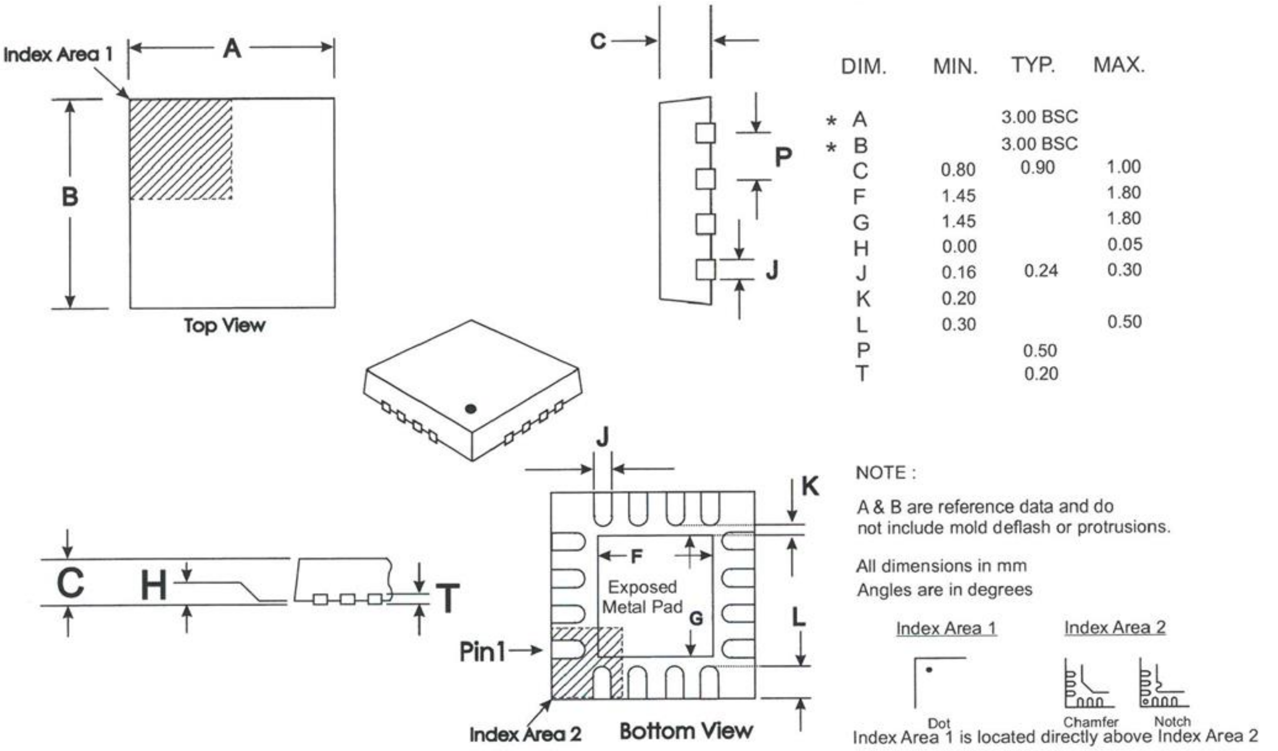


Figure 35: Return Loss – through line

Package Outline

16-lead 3x3mm VQFN Package (QF)



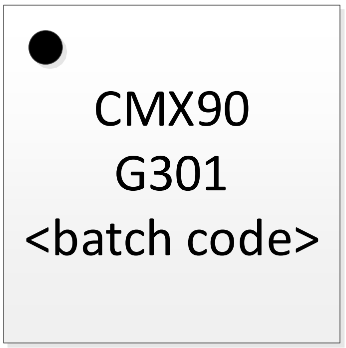
DIM.	MIN.	TYP.	MAX.
* A		3.00 BSC	
* B		3.00 BSC	
C	0.80	0.90	1.00
F	1.45		1.80
G	1.45		1.80
H	0.00		0.05
J	0.16	0.24	0.30
K	0.20		
L	0.30		0.50
P		0.50	
T		0.20	

NOTE :
A & B are reference data and do not include mold deflash or protrusions.
All dimensions in mm
Angles are in degrees

Index Area 1 is located directly above Index Area 2

Package Marking

Pin 1 indicator (dot) and 3 rows of text for device identification.



Line 1: CMX90 SμRF series

Line 2: 4-character part code

Line 3: Batch code

Revision History

Issue	Description	Date
3	First full release	September 2022
2	Advance Information. Added data to Electrical Specification and Typical Performance	June 2021
1	Advance Information	March 2021

Contact Information

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