AN3118
Application note

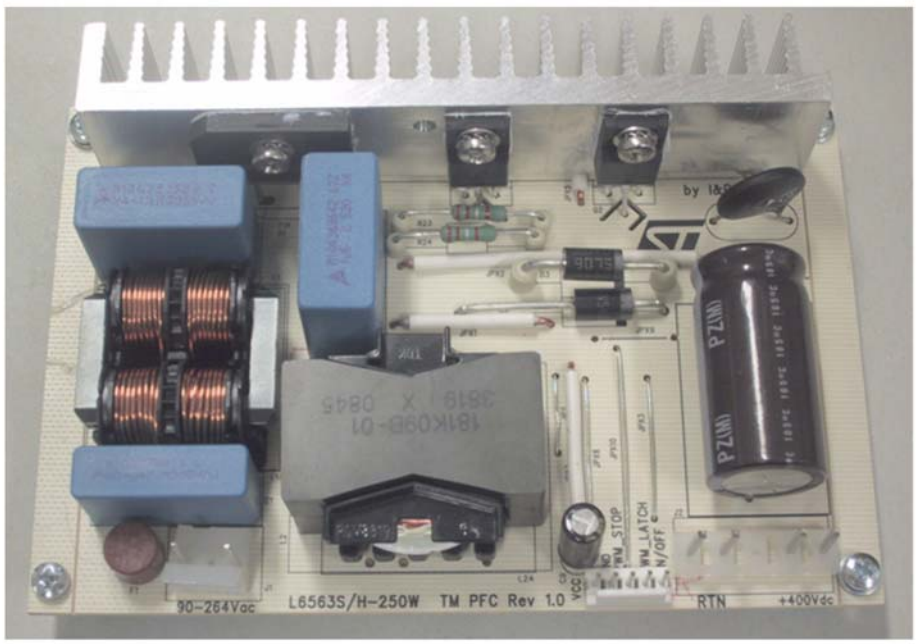
250 W transition-mode PFC pre-regulator with the new L6563H

Introduction

This application note describes a demonstration board based on the new L6563H transition-mode PFC controller and presents the results of its bench evaluation.The board implements an 250 W, wide-range mains input PFC pre-conditioner suitable for desktop PCs, high power adapters, flat screen displays, and all SMPS having to meet the IEC61000-3-2 or the JEITA-MITI regulation.

The L6563H is a new current-mode PFC controller operating in transition mode (TM) and implementing an internal high voltage startup circuitry.

Figure 1. EVL6563H-250W: L6563H 250 W TM PFC demonstration board



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1 Main characteristics and circuit description

The main characteristics of the SMPS are listed below:

- Line voltage range: 90 to 265 Vac
- Line frequency (f_L): 47 to 63 Hz
- Regulated output voltage: 400 V
- Rated output power: 250 W
- Maximum $2f_L$ output voltage ripple: 22 V pk-pk
- Hold-up time: 10 ms (V_{DROP} after hold-up time: 300 V)
- Minimum switching frequency: 46 kHz
- Minimum estimated efficiency: 93 % (@ Vin=90 Vac, Pout=250 W)
- Maximum ambient temperature: 50 °C
- PCB type and size: single side, 35 µm, CEM-1, 88 x 116 mm

This demonstration board implements a power factor correction (PFC) pre-regulator, 250 W continuous power, delivering a regulated 400 V rail from a wide range mains voltage and providing for the reduction of the mains harmonics, therefore meeting the European EN61000-3-2 or the Japanese JEITA-MITI standard. The regulated output voltage is typically the input for the cascaded isolated DC-DC converter that will provide the output rails required by the load.

The power stage of the PFC is a conventional boost converter, connected to the output of the D1 rectifier bridge. It is completed by the L2 coil, the D3 diode, and the C5 capacitor. The boost switch is represented by the power Q1 and Q2 MOSFETs, connected in parallel. The NTC R1 limits the inrush current at switch on. It is connected on the DC rail, in series to the output electrolytic capacitor, in order to improve the efficiency during low line operation. In fact the RMS current flowing into the output stage is lower than current flowing into the input stage at the same input voltage. The board is equipped with an input EMI filter necessary to filter the switching noise coming from the boost stage.

At startup the L6563H (U1) is powered by the Vcc electrolytic capacitor C9 which is charged via High Voltage Start up (HVS) pin #9. The HVS pin, able to withstand 700V, is connected directly to the rectified mains voltage. A 0.85 mA (typ.) internal current source charges the C9 capacitor connected between Vcc pin #16 and GND pin #14 until the voltage on the Vcc pin reaches the startup threshold. The L2 secondary winding and the charge pump circuit (C6, R2, D4 and D5) generate the Vcc voltage, powering the L6563H during normal operations. The L2 secondary winding is also connected to the L6563H pin #13 (ZCD) through the R14 resistor. Its purpose is to supply the information which L2 has demagnetized, needed by the internal logic to trigger a new switching cycle.

The divider R4, R8, R12 and R15 provides to the L6563H multiplier the information of the instantaneous mains voltage that is used to modulate the peak current of the boost.

The R3, R6, R7 with R9 and R10 resistors are dedicated to sensing the output voltage and feed to the L6563H the feedback information necessary to regulate the output voltage. The C7, R13, and C10 components are the error amplifier compensation network necessary to get the required loop stability.

The peak current is sensed by R23 and R24 resistors in series to the MOSFET and the signal is fed into pin #4 (CS) of the L6563H via the filter by R20 and C14.

C12, R27 and R28 are connected to pin # 5 (V_{FF}), they complete an internal peak-holding circuit which obtains the information on the RMS mains voltage. The voltage signal at this pin, a DC level equal to the peak voltage on pin #3 (MULT), is fed to a second input to the multiplier for $1/V^2$ function necessary to compensate the control loop gain dependence on the mains voltage. Additionally, pin #12 (RUN) is connected to pin# 5 (V_{FF}) through the R27 and R28 resistor divider providing a voltage level for brown-out (AC mains under voltage) protection. A voltage on the RUN pin below 0.8V shuts down (not latched) the IC and brings its consumption to a considerably lower level. The L6563H restarts as the voltage at the pin rises above 0.88 V.

The R21, R25, R26 and R33 dividers provide the information regarding the output voltage level to the L6563H pin #7 (PFC_OK). It is required by the L6563H output voltage monitoring and disable functions used for PFC protection purposes.

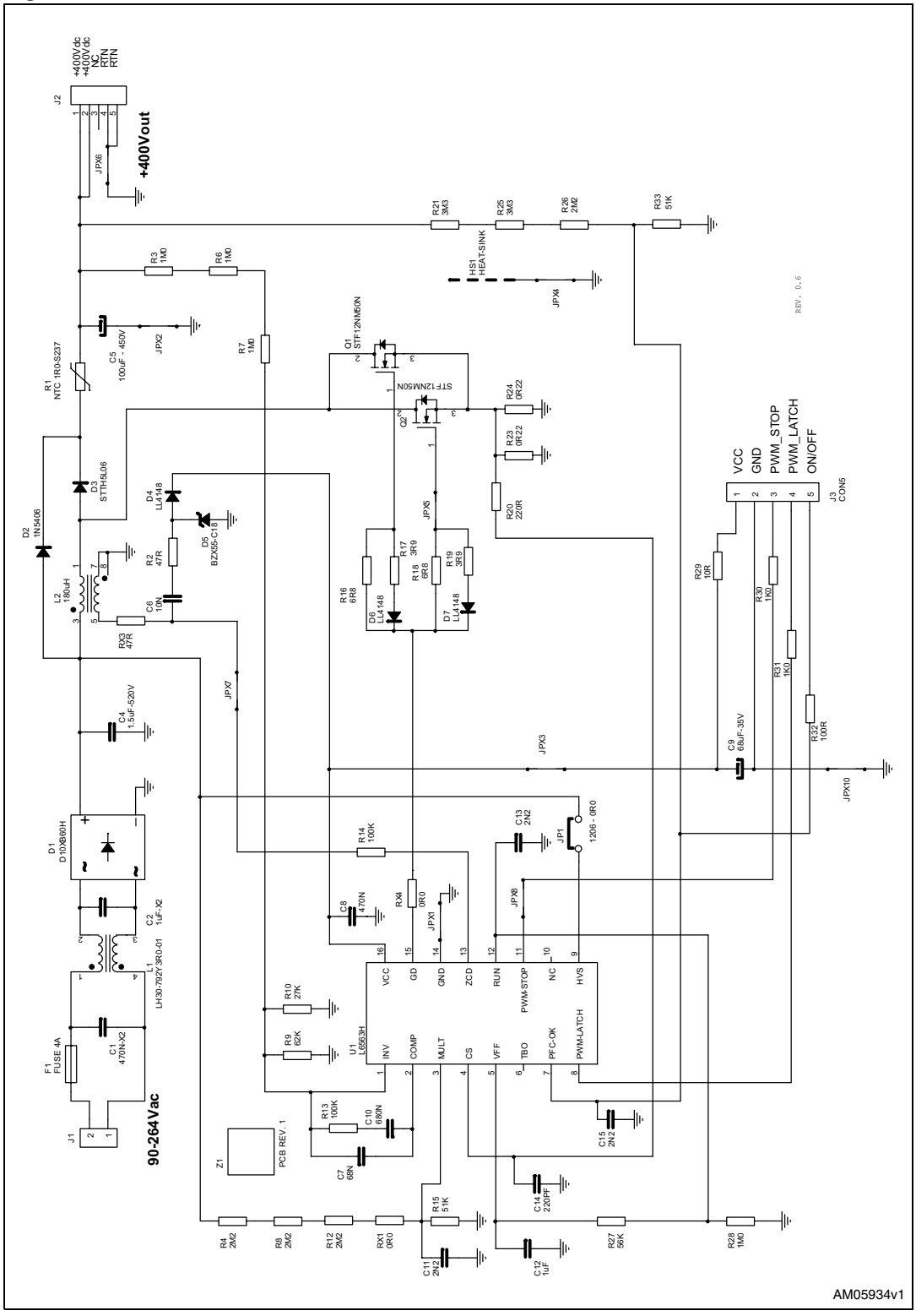
If the voltage on pin #7 exceeds 2.5 V the IC stops switching and restarts as the voltage on the pin falls below 2.4 V, realizing the so called dynamic OVP, preventing the output voltage from becoming excessive in case of transient, due to the slow response of the error amplifier. However, if contemporaneously the voltage of the INV pin falls below 1.66 V (typ.), a feedback failure is assumed. In this case the device is latched off. Normal operation can be resumed only by cycling Vcc, bringing its value lower than 6 V before moving up to turn-on threshold.

Additionally, if the voltage on pin #7 (PFC_OK) is tied below 0.23V, the L6563H is shut down. To restart the L6563H operation the voltage on pin #7 (PFC_OK) must increase above 0.27 V. This function can be used as a remote on/off control input.

To allow the interfacing of the board with a D2D converter the J3 connector allows the powering of the L6563H with an external Vcc. It also gives the opportunity to manage failure or abnormal conditions via the PWM_LATCH (#8) and PWM_STOP (#11) pins. The L6563H operation can be also disabled or enabled to properly manage light load or failure conditions by the D2D via the PFC_OK pin (#7), still available at pin #5 of J3 (ON/OFF). For further details please see *Section 4.6*.

2 Electrical diagram

Figure 2. EVL6563H-250W: demonstration board TM PFC electrical schematic



3 Bill of material

Table 1. EVL6563H-250W TM PFC bill of material

Des.	Part type/ part value	Case style/ package	Description	Supplier
C1	470 N-X2	6X26.5 mm	X2 - FLM CAP - B32923A3474M	EPCOS
C10	680 N	0805	25 V CERCAP - general purpose	AVX
C11	2N2	0805	50 V CERCAP - general purpose	AVX
C12	1 µF	0805	25 V CERCAP - general purpose	AVX
C13	2N2	0805	50 V CERCAP - general purpose	AVX
C14	220PF	0805	50 V CERCAP - general purpose	AVX
C15	2N2	0805	50 V CERCAP - general purpose	AVX
C2	1 µF-X2	11X26.5 mm	X2 - FLM CAP - B32923C3105+***	EPCOS
C4	1.5 µF-520 V	12X26.5 mm	520 V - FLM CAP - B32673Z5155	EPCOS
C5	100 µF - 450 V	Dia. 18X35 mm	450 V, aluminium ELCAP - TXW series,105 °C	RUBYCON
C6	10 N	1206	100 V CERCAP - general purpose	AVX
C7	68 N	0805	50 V CERCAP - general purpose	AVX
C8	470 N	1206	50 V CERCAP - general purpose	AVX
C9	68 µF-35 V	Dia. 6.3X11 mm	35 V, aluminium ELCAP - FM series, 105 °C	PANASONIC
D1	D10XB60H	DWG	Single phase bridge rectifier	SHINDENGEN
D2	1N5406	DO-201	Rectifier - general purpose	VISHAY
D3	STTH5L06	DO-201	Ultrafast high voltage rectifier	STMicroelectronics
D4	LL4148	MINIMELF	High speed signal diode	VISHAY
D5	BZX55-C18	MINIMELF	Zener diode	VISHAY
D6	LL4148	MINIMELF	High speed signal diode	VISHAY
D7	LL4148	MINIMELF	High speed signal diode	VISHAY
F1	FUSE 4A	DWG	Fuse T4A - time delay	WICHMANN
HS1	HEAT-SINK	DWG	Heat sink for D1& Q1, Q2 - H=23 mm	
J1	CON2-IN		Input connector - pitch 7.62 MM - 2 pins	MOLEX
J2	CON5	DWG	Output connector - pitch 5.08 MM - 5 pins	MOLEX
J3	CON5		PCB term. block, PITCH 2.5MM - 5 W	MOLEX
JP1	1206 - 0R0	1206	SMD standard film res, 1/4 W - 5 %, 250 ppm/°C	VISHAY
JPX1	Wire jumper		Insulated wire jumper	
JPX10	Wire jumper		Wire jumper	
JPX2	Wire jumper		Insulated wire jumper	

Table 1. EVL6563H-250W TM PFC bill of material (continued)

Des.	Part type/ part value	Case style/ package	Description	Supplier
JPX3	Wire jumper		Wire jumper	
JPX4	Wire jumper		Wire jumper	
JPX5	Wire jumper		Insulated wire jumper	
JPX6	Wire jumper		Wire jumper	
JPX7	Wire jumper		Insulated wire jumper	
JPX8	Wire jumper		Wire jumper	
L1	LH30-792Y3R0-01	DWG	Input EMI filter - 7.9 mH-3 A	TDK
L2	180 µH	DWG	PFC inductor PFC3819QM-181K09B-01	TDK
Q1	STF12NM50N	TO-220FP	N-channel power MOSFET	STMicroelectronics
Q2	STF12NM50N	TO-220FP	N-channel power MOSFET	STMicroelectronics
R1	NTC 1R0-S237	DWG	NTC resistor P/N B57237S0109M000	EPCOS
R10	27 kΩ	0805	SMD STD film res - 1/8 W - 1 % - 100 ppm/°C	VISHAY
R12	2.2 MΩ	1206	SMD STD film res - 1/4 W - 1 % - 100 ppm/°C	VISHAY
R13	100 kΩ	0805	SMD STD film res - 1/8 W - 5 % - 250 ppm/°C	VISHAY
R14	100 kΩ	1206	SMD STD film res - 1/4 W - 1 % - 100 ppm/°C	VISHAY
R15	51 kΩ	0805	SMD STD film res - 1/8 W - 5 % - 250 ppm/°C	VISHAY
R16	6.8 Ω	0805	SMD STD film res - 1/8 W - 5 % - 250 ppm/°C	VISHAY
R17	3.9 Ω	0805	SMD STD film res - 1/8 W - 5 % - 250 ppm/°C	VISHAY
R18	6.8 Ω	0805	SMD STD film res - 1/ 8W - 5 % - 250 ppm/°C	VISHAY
R19	3.9 Ω	0805	SMD STD film res - 1/8 W - 5 % - 250 ppm/°C	VISHAY
R2	47 Ω	1206	SMD STD film res - 1/4 W - 5 % - 250 ppm/°C	VISHAY
R20	220 Ω	1206	SMD STD film res - 1/4 W - 5 % - 250 ppm/°C	VISHAY
R21	3.3 MΩ	1206	SMD STD film res - 1/4 W - 1 % - 100 ppm/°C	VISHAY
R23	0.22 Ω	PTH	SFR25 AX. STD. film res, 0.4 W, 5 %, 250 ppm/°C	VISHAY
R24	0.22 Ω	PTH	SFR25 AX. STD. film res, 0.4 W, 5 %, 250 ppm/°C	VISHAY
R25	3.3 Ω	1206	SMD STD film res - 1/4 W - 1 % - 100 ppm/°C	VISHAY
R26	2.2 Ω	1206	SMD STD film res - 1/4 W - 1 % - 100 ppm/°C	VISHAY
R27	56 kΩ	0805	SMD STD film res - 1/8 W - 1 % - 100 ppm/°C	VISHAY
R28	1M0	0805	SMD STD film res - 1/8 W - 1 % - 100 ppm/°C	VISHAY
R29	10 Ω	0805	SMD STD film res - 1/8 W - 5 % - 250 ppm/°C	VISHAY
R3	1M0	1206	SMD STD film res - 1/4 W - 1 % - 100 ppm/°C	VISHAY
R30	1K0	0805	SMD STD film res - 1/8 W - 5 % - 250 ppm/°C	VISHAY
R31	1K0	0805	SMD STD film res - 1/8 W - 5 % - 250 ppm/°C	VISHAY

Table 1. EVL6563H-250W TM PFC bill of material (continued)

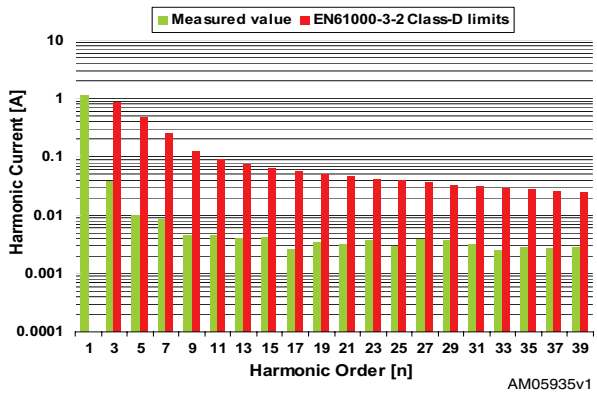
Des.	Part type/ part value	Case style/ package	Description	Supplier
R32	100 Ω	0805	SMD STD film res - 1/8 W - 5 % - 250 ppm/°C	VISHAY
R33	51 kΩ	0805	SMD STD film res - 1/8 W - 1 % - 100 ppm/°C	VISHAY
R4	2.2 Ω	1206	SMD STD film res - 1/4 W - 1 % - 100 ppm/°C	VISHAY
R6	1M0	1206	SMD STD film res - 1/4 W - 1 % - 100 ppm/°C	VISHAY
R7	1M0	1206	SMD STD film res - 1/4 W - 1 % - 100 ppm/°C	VISHAY
R8	2.2 MΩ	1206	SMD STD film res - 1/4 W - 1 % - 100 ppm/°C	VISHAY
R9	62 kΩ	0805	SMD STD film res - 1/4 W - 1 % - 100 ppm/°C	VISHAY
RX1	0R0	1206	SMD STD film res - 1/4 W - 5 % - 250 ppm/°C	VISHAY
RX3	47 Ω	1206	SMD STD film res - 1/4 W - 5 % - 250 ppm/°C	VISHAY
RX4	0R0	1206	SMD STD film res - 1/4 W - 5 % - 250 ppm/°C	VISHAY
U1	L6563H	SO16	HV startup TM PFC controller	STMicroelectronics
Z1	PCB REV. 1			

4 Test results and significant waveforms

4.1 Harmonic content measurement

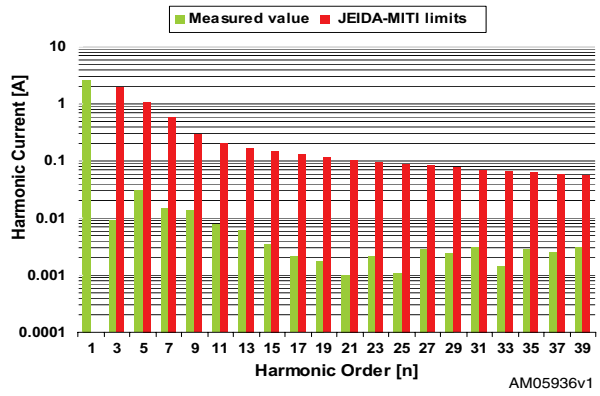
One of the main purposes of a PFC pre-conditioner is the correction of input current distortion, decreasing the harmonic contents below the limits of the relevant regulations. Therefore, this demonstration board has been tested according to the European standard EN61000-3-2 Class-D and Japanese standard JEITA-MITI class-D, at full load and 70 W output power, at both the nominal input voltage mains. As shown in the following images, the circuit is able to reduce the harmonics well below the limits of both regulations from full load down to light load. 70 W of output power has been chosen because it is almost the lowest power limit at which the harmonics have to be limited according to the mentioned standards. Measurements are given in *Figure 3* to *6*.

Figure 3. EVL6563H-250W TM PFC compliance to EN61000-3-2 standard at 250W



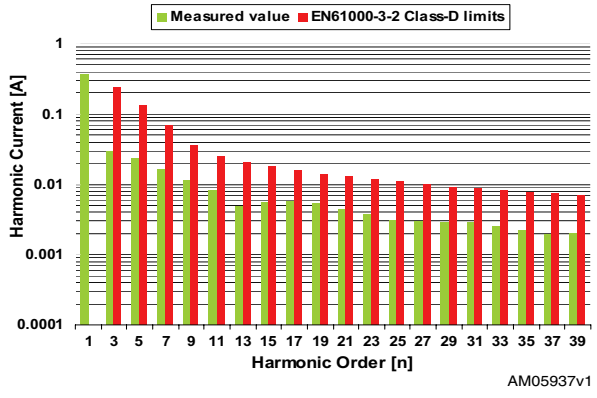
Vin = 230 Vac - 50 Hz, Pout = 250 W, THD = 4.02 %, PF = 0.986

Figure 4. EVL6563H-250W TM PFC compliance to JEITA-MITI standard at 250 W



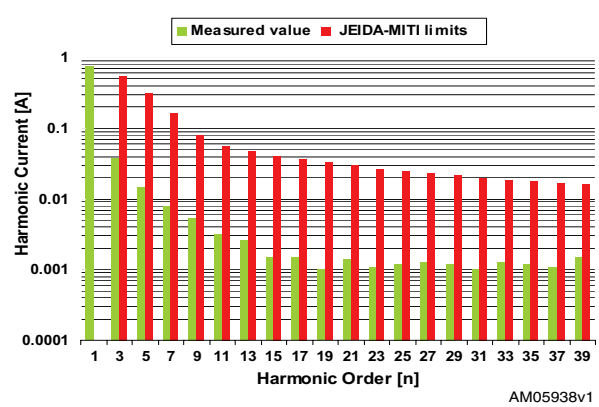
Vin = 100 Vac - 50 Hz, Pout = 250 W, THD = 3.65 %, PF = 0.999

Figure 5. EVL6563H-250W TM PFC compliance to EN61000-3-2 standard at 70 W



Vin = 230 Vac - 50 Hz, Pout = 70 W, THD = 11.94 %, PF = 0.87

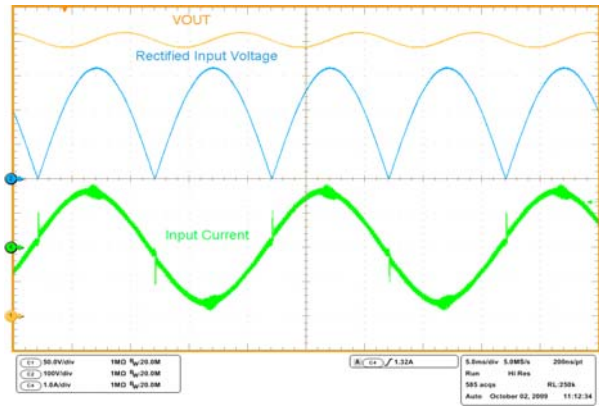
Figure 6. EVL6563H-250W TM PFC compliance to JEITA-MITI standard at 70 W



Vin = 100 Vac - 50 Hz, Pout = 70 W, THD = 5.46 %, PF = 0.995

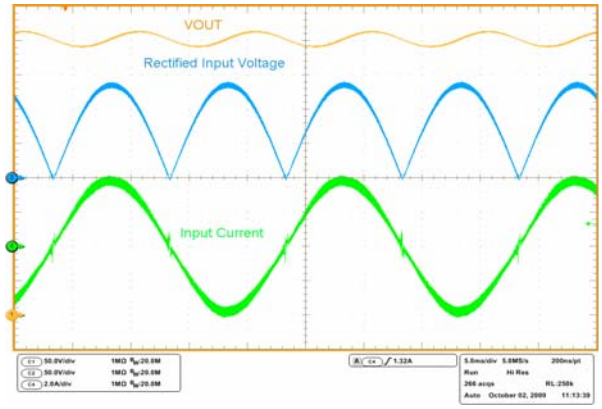
For user reference, waveforms of the input current and output voltage at 230 Vac and 100 Vac input voltage mains during nominal and 70 W load operation, are reported in *Figure 7* and *8*.

Figure 7. EVL6563H-250W TM PFC input current waveform @230 V - 50 Hz - 250 W load



CH1: Vout
CH2: V bridge
CH4: I_AC

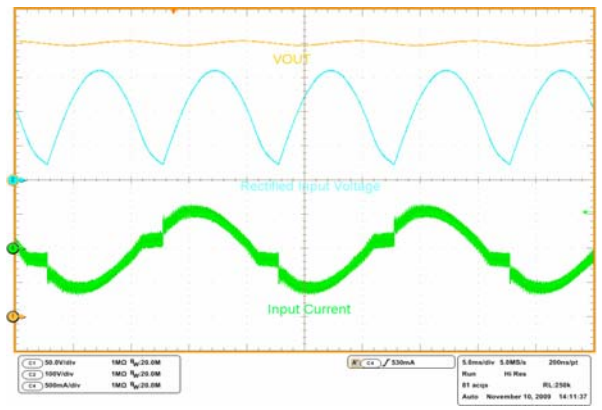
Figure 8. EVL6563H-250W TM PFC input current waveform @100 V - 50 Hz - 250 W load



CH1: Vout
CH2: V bridge
CH4: I_AC

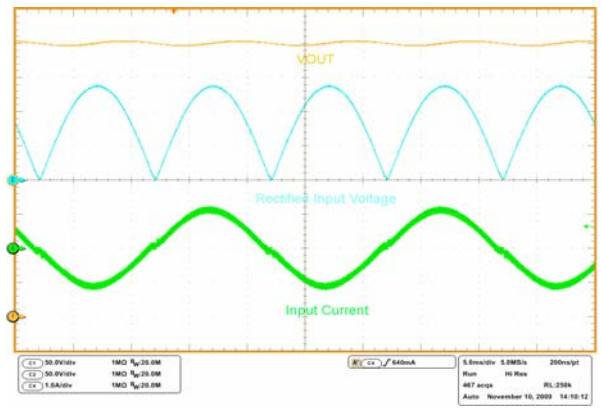
As shown in the images, the current shape is very good, and sinewave has very low distortion as confirmed by the low THD in all line and load conditions.

Figure 9. EVL6563H-250W TM PFC input current waveform @230 V - 50 Hz - 70 W load



CH1: Vout
CH2: V bridge
CH4: I_AC

Figure 10. EVL6563H-250W TM PFC input current waveform @100 V - 50 Hz - 70 W load



CH1: Vout
CH2: V bridge
CH4: I_AC

The power factor (PF) and the total harmonic distortion (THD) have also been measured and the results are reported in the graphs of *Figure 11* and *12*. As seen, the PF remains close to unity throughout the input voltage mains and the total harmonic distortion is very low over all the load range during operation at low mains. THD increases and PF decreases during European mains operation at light load because the circuit begins working in burst mode to maintain good efficiency, preventing from operating at a too high switching frequency. In case the burst mode operation cannot be accepted, a compromise with efficiency must be found. The burst mode threshold can be slightly adjusted by modifying the multiplier divider ratio and/or the compensation network.

Figure 11. EVL6563H-250W TM PFC power factor vs. output power

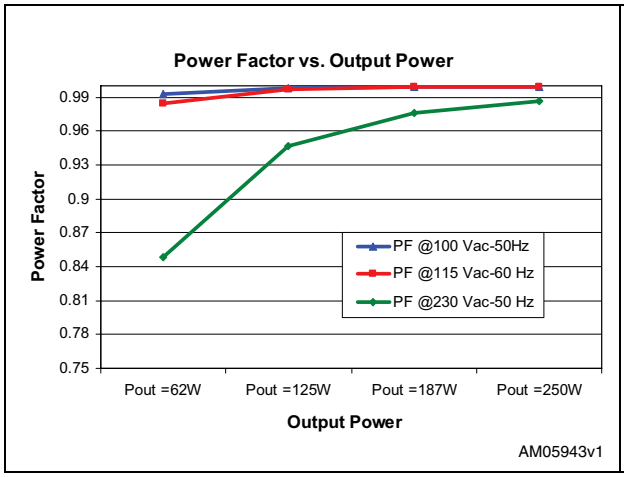
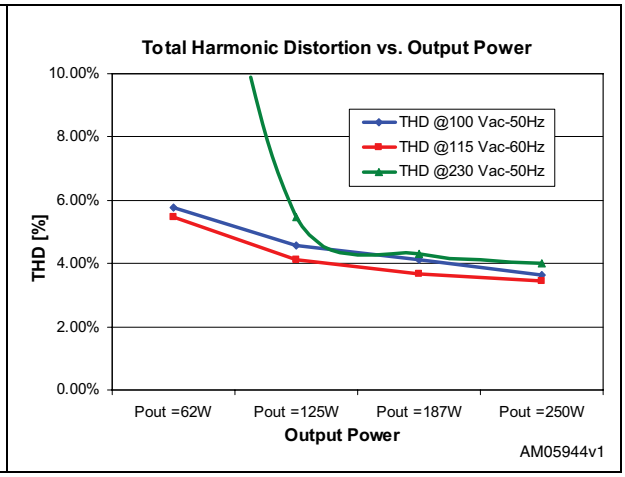


Figure 12. EVL6563H-250W TM PFC THD vs. output power



The efficiency, measured according to the ES-2 requirements, is shown in *Figure 13*; it is excellent at all load and line conditions. At full load it is always higher than 95 %, making this design suitable for high efficiency power supplies. The average efficiency calculated according to the ES-2 requirements at different nominal mains voltages is shown in *Figure 14*.

Figure 13. EVL6563H-250W TM PFC efficiency vs. output power

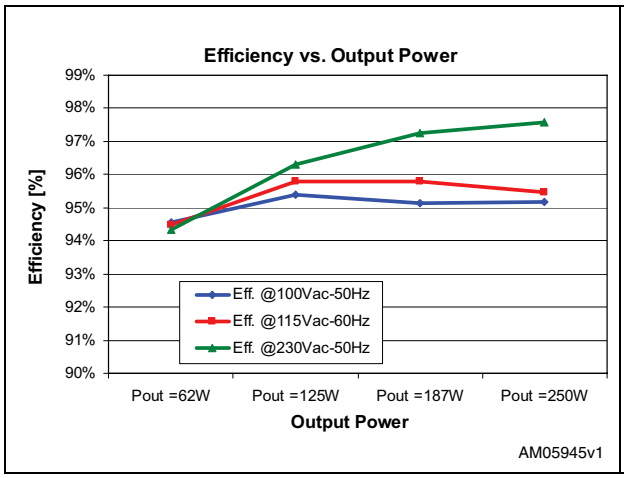


Figure 14. EVL6563H-250W TM PFC average efficiency acc. to ES-2

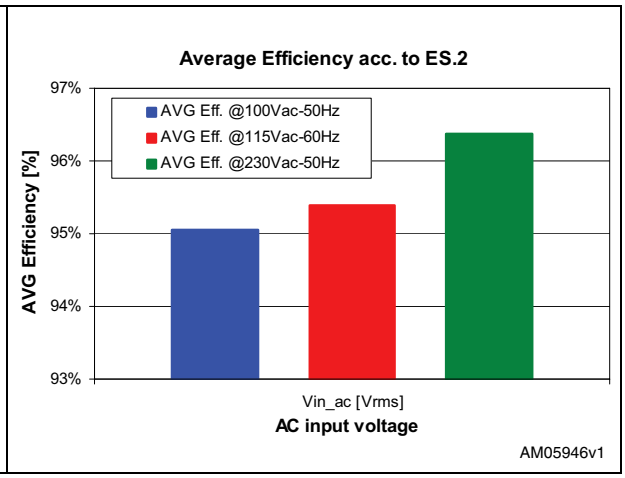
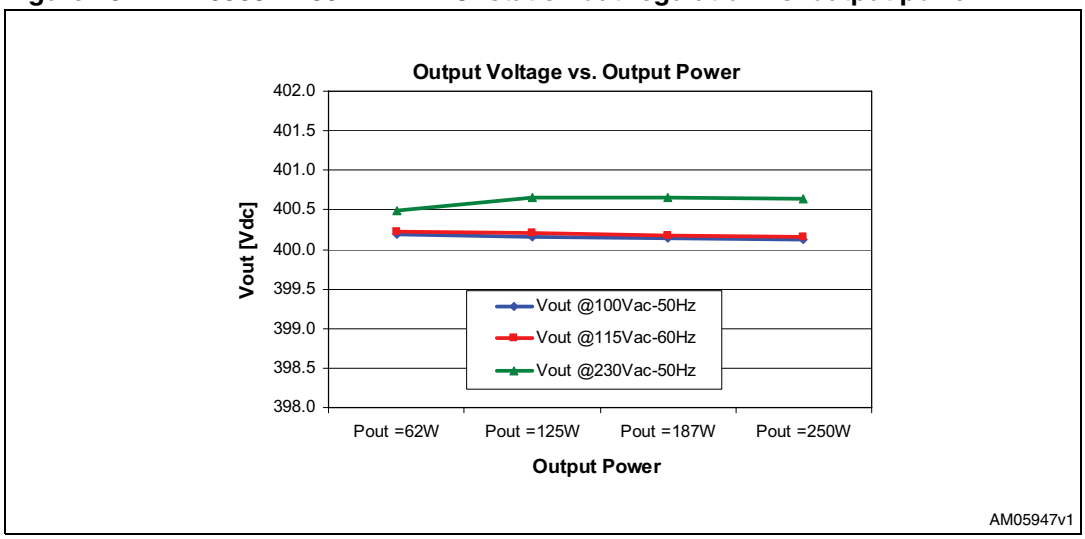


Figure 15. EVL6563H-250W TM PFC: static Vout regulation vs. output power



The measured output voltage at different line and load conditions is reported in *Figure 15*. As shown, the voltage is very stable over all the input voltage and output load range.

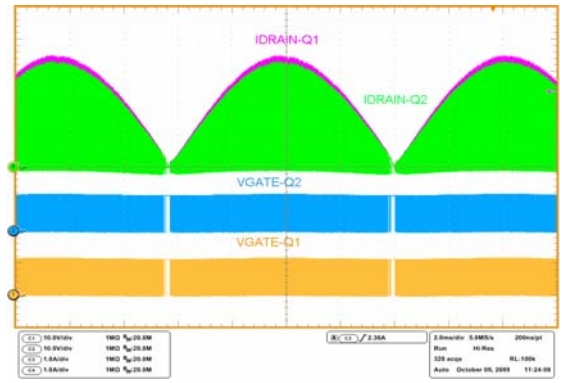
4.2 MOSFET current, TM signals, and L6563H THD optimizer

In the following images the waveforms relevant to the switch current at 100 Vac voltage mains are reported; in *Figure 16* and *17* it can be noted that the current peaks in the two MOSFETs in parallel are very close to each other, demonstrating perfect current sharing between the two devices. The two MOSFETs in parallel allow the total thermal resistance junction-heat sink to decrease, therefore the same peak current can be managed using two smaller and cheaper MOSFETs instead of one bigger one.

In *Figure 16*, close to the zero crossing points of the sinewave, it is possible to note the action of the THD optimizer embedded in the L6563H. It is a circuit which minimizes the conduction dead-angle occurring to the AC input current near the zero-crossings of the line voltage (crossover distortion). In this way, the THD of the current is considerably reduced. A major cause of this distortion is the inability of the system to transfer energy effectively when the instantaneous line voltage is very low. This effect is magnified by the high frequency filter capacitor placed after the bridge rectifier, which retains some residual voltage that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop. To overcome this issue the device forces the PFC pre-regulator to process more energy near the line voltage zero-crossings as compared to that commanded by the control loop. This results in both minimizing the time interval where energy transfer is lacking, and fully discharging the high-frequency filter capacitor after the bridge. Essentially, the circuit artificially increases the ON-time of the power switch with a positive offset added to the output of the multiplier in the proximity of the line voltage zero-crossings. This offset is reduced as the instantaneous line voltage increases, so that it becomes negligible as the line voltage moves toward the top of the sinusoid. Furthermore, the offset is modulated by the voltage on the V_{FF} pin so as to have little offset at low line, where energy transfer at zero crossings is typically quite good, and a larger offset at high line where the energy transfer worsens.

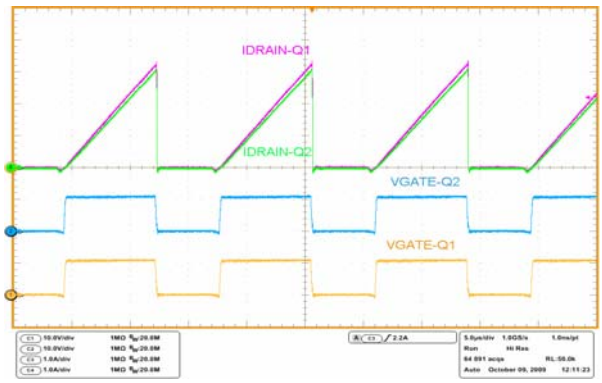
To take maximum benefit from the THD optimizer circuit, the high-frequency filter capacitors, after the bridge rectifier, should be minimized, maintaining compatibility with EMI filtering needs. A large capacitance, in fact, introduces a conduction dead-angle of the AC input current in itself, therefore reducing the effectiveness of the optimizer circuit.

Figure 16. EVL6563H-250W TM PFC MOSFET current at 100 Vac - 50 Hz - full load



CH1: Q1 gate voltage, CH2: Q2 gate voltage,
CH3: Q1 drain current
CH4: Q2 drain current

Figure 17. EVL6563H-250W TM PFC MOSFET current at 100 Vac - 50 Hz - full load

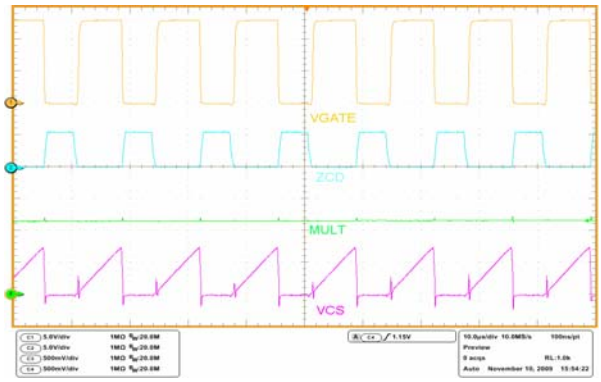


CH1: Q1 gate voltage, CH2: Q2 gate voltage,
CH3: Q1 drain current
CH4: Q2 drain current

In *Figure 18*, the detail of the waveforms at switching frequency shows the operation of the transition mode control; once the inductor has transferred all the energy stored a falling edge on the ZCD pin (#13) is detected and it will trigger a new on-time, by setting the gate drive high. Once the current signal on the CS pin (#4) has reached the level programmed by the internal multiplier circuitry according to the input mains instantaneous voltage and the error amplifier output level, the gate drive is set low and MOSFET conduction is stopped. During the following off-time the energy stored in the inductor is transferred into the output capacitor and the load. At the end of the current conduction a new demagnetization will be detected by the ZCD that will provide for a new on-time of the MOSFET.

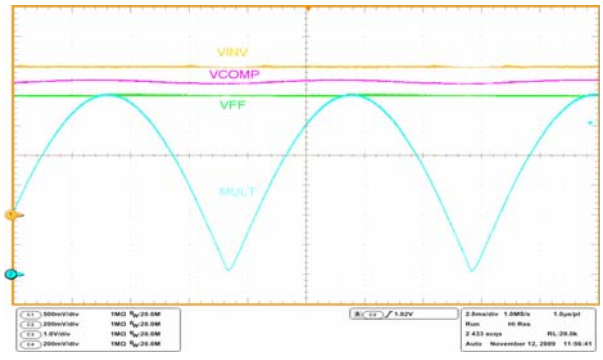
In *Figure 19* waveforms of the MULT, V_{FF}, INV and COMP pins are captured for user reference.

Figure 18. EVL6563H-250W TM PFC L6563H control pins-1 at 115 Vac - 60 Hz - full load



CH1: GD - pin #15, CH2: ZCD - pin #13, CH3: CS - pin #4
CH4: MULT - pin #3

Figure 19. EVL6563H-250W TM PFC L6563H control pins-2 at 115 Vac - 60 Hz - full load



CH1: INV - pin #1, CH2: MULT - pin #3,
CH3: COMP - pin #2 CH, 4: V_{FF} - pin #5

4.3 Voltage feed-forward and brown-out function

The power stage gain of PFC pre-regulators varies with the square of the RMS input voltage. As does the crossover frequency fc of the overall open-loop gain because the gain has a single pole characteristic. This leads to large trade-offs in the design. For example, setting the gain of the error amplifier to get fc = 20 Hz @ 264 Vac means having fc 4 Hz @ 88 Vac, resulting in sluggish control dynamics. Additionally, the slow control loop causes large transient current flow during rapid line or load changes that are limited by the dynamics of the multiplier output. This limit is considered when selecting the sense resistor to let the full load power pass under minimum line voltage conditions, with some margin. But a fixed current limit allows excessive power input at high line, whereas a fixed power limit requires the current limit to vary inversely with the line voltage.

Voltage feed-forward can compensate for the gain variation with the line voltage and overcome all of the above mentioned issues. It consists of deriving a voltage proportional to the input RMS voltage, feeding this voltage into a squarer/divider circuit ($1/V^2$ corrector) and providing the resulting signal to the multiplier that generates the current reference for the inner current control loop.

In this way a change of the line voltage will cause an inversely proportional change of the half-sine amplitude at the output of the multiplier (if the line voltage doubles the amplitude of the multiplier, output is halved and vice versa) so that the current reference is adapted to the new operating conditions with (ideally) no need for invoking the slow dynamics of the error amplifier. Additionally, the loop gain will be constant throughout the input voltage range, which improves dynamic behavior at low line significantly and simplifies loop design.

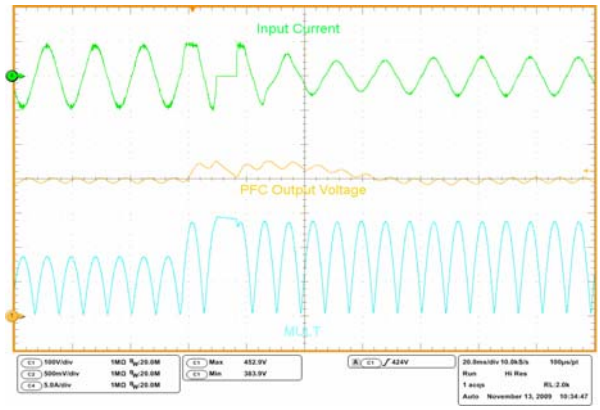
Actually, with another PFC embedding the voltage feed-forward, deriving a voltage proportional to the RMS line voltage implies a form of integration, which has its own time constant. If it is too small the voltage generated is affected by a considerable amount of ripple at twice the mains frequency that causes distortion of the current reference (resulting in high THD and poor PF); if it is too large there is a considerable delay in setting the right amount of feed-forward, resulting in excessive overshoot and undershoot of the pre-regulator's output voltage in response to large line voltage changes. Clearly a trade off was required.

The L6563H realizes an innovative voltage feed-forward which, with a technique that overcomes this time constant trade off issue whichever voltage change occurs on the mains, both surges and drops. A C_{FF} (C12) capacitor and a RFF (R27 + R28) resistor, both connected to the V_{FF} pin (#5), complete an internal peak-holding circuit that provides a DC voltage equal to the peak of the rectified sinewave applied on the MULT pin (#3). In this way, in case of sudden line voltage rise, C_{FF} is rapidly charged through the low impedance of the internal diode; in case of line voltage drop, an internal “mains drop” detector enables a low impedance switch which suddenly discharges C_{FF}, avoiding a long settling time before reaching the new voltage level. Consequently an acceptably low steady-state ripple and low current distortion can be achieved without any considerable undershoot or overshoot on the pre-regulator's output, like in systems with no feed-forward compensation.

In *Figure 21* the behavior of the EVL6563H-250W demonstration board, in case of an input voltage surge from 90 to 140 Vac, is shown; in the image it is evident that the V_{FF} function provides for the stability of the output voltage which is not affected by the input voltage surge. In fact, thanks to the V_{FF} function, the compensation of the input voltage variation is very fast and the output voltage remains stable at its nominal value. The opposite is confirmed in *Figure 20*; the behavior of a PFC using the L6562A and delivering the same output power is shown; in case of a mains surge the controller cannot compensate it and the output voltage stability is guaranteed by the feedback loop only. Unfortunately, as previously stated, its bandwidth is narrow and therefore the output voltage has a significant deviation

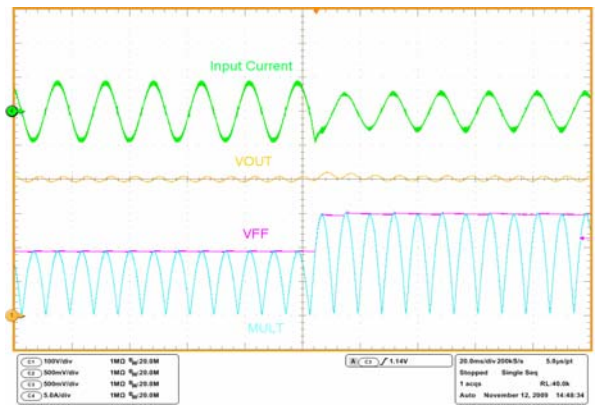
from the nominal value. The circuit has the same behavior in the case of mains surge at any input voltage, and it is not affected if the input mains surge happens at any point of the input sinewave.

Figure 20. L6562A input mains surge 90 Vac to 140 Vac - no V_{FF} input



CH1: Vout, CH2: MULT (pin #3), CH4: I_AC

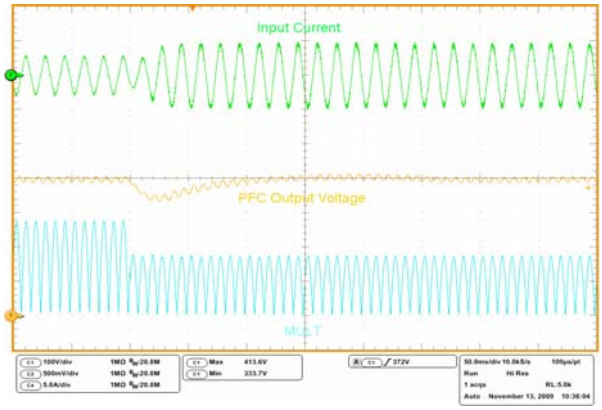
Figure 21. EVL6563H-250W TM PFC input mains surge 90 Vac to 140 Vac



CH1: Vout, CH3: V_{FF} (pin #5), CH2: MULT (pin #3)
CH4: I_AC

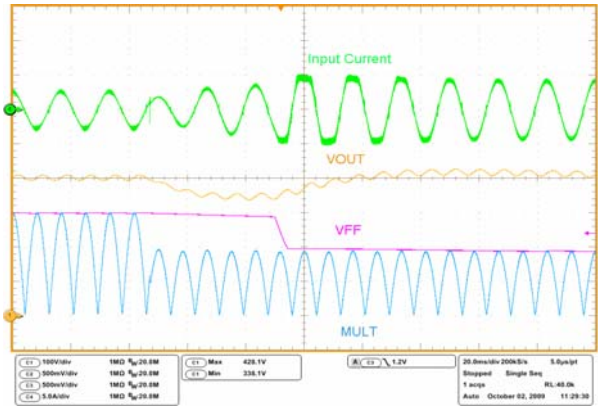
In *Figure 23* the circuit behavior in case of mains dip is shown; as previously described, the internal circuitry has detected the decrease of the mains voltage and it has activated the C_{FF} internal fast discharge. As seen, in this case the output voltage changes but in a few mains cycles it returns to the nominal value. The situation is different if we compare it with the performance of a controller without the V_{FF} function. In *Figure 22*, the behavior of a PFC using the L6562A delivering similar output power is shown; in the case of a mains dip from 140 Vac to 90 Vac the output voltage variation is not very different but the output voltage requires a longer time to restore the original value. In tests with a wider voltage variation (e.g. 265 Vac to 90 Vac), the output voltage variation of a PFC without the voltage feed-forward fast discharging is much more emphasized.

Figure 22. L6562A: input mains dip 140 Vac to 90 Vac - no V_{FF} input



CH1: Vout, CH2: MULT (pin #3), CH4: I_AC

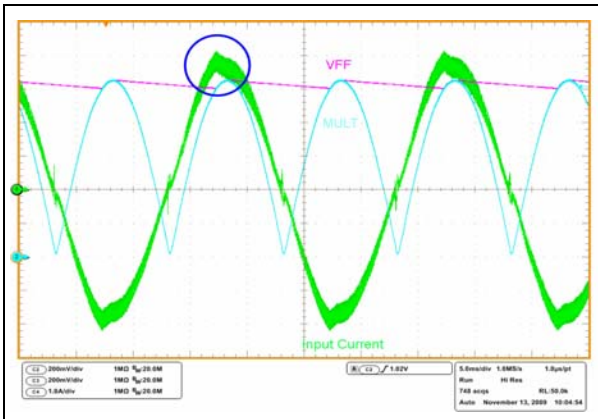
Figure 23. EVL6563H-250W TM PFC input mains dip 140 Vac to 90 Vac



CH1: Vout, CH2: MULT (pin #3), CH3: V_{FF} (pin #5), CH4: I_AC

It is also possible to see, comparing *Figure 24* and *25*, that the input current of the latter has a better shape and the 3rd harmonic current distortion is not noticeable; this demonstrates the benefits of the new voltage feed-forward circuit integrated in the L6563H, allowing a fast response to mains disturbances to be obtained but using a reasonably long V_{FF} time constant also provides very low THD and high PF at the same time, as confirmed by the measurements in *Figure 24* and *25*:

Figure 24. L6563 input current at 100 Vac - 50 Hz C_{FF}=0.47 µF, RFF=390 kΩ



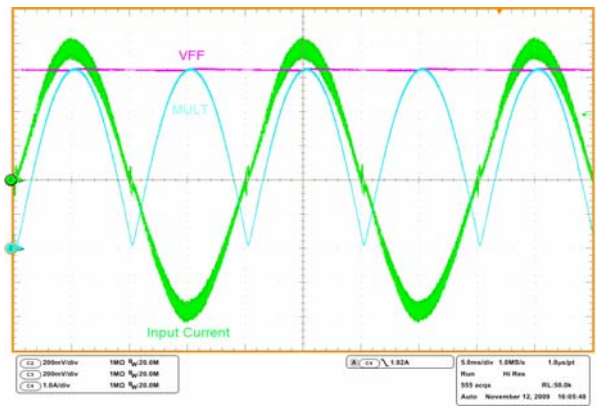
THD= 4.36 %, 3rd harmonic=94.6 mA

CH2: MULT (pin #3)

CH3: V_{FF} (pin #5)

CH4: I_AC

Figure 25. EVL6563H-250 W TM PFC input current at 100 Vac - 50 Hz C_{FF}=1 µF, RFF=1 MΩ



THD= 2.94 %, 3rd harmonic=30.5 mA

CH2: MULT (pin #3)

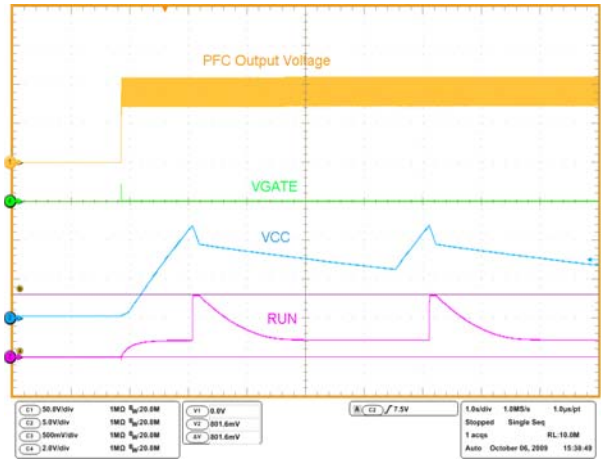
CH3: V_{FF} (pin #5)

CH4: I_AC

Another function integrated in the L6563H is brown-out protection, which is basically a not-latched shutdown function that must be activated when a mains under voltage condition is detected. This abnormal condition may cause overheating of the primary power section due to an excess of RMS current. Brown-out can also cause the PFC pre-regulator to work open-loop and this could be dangerous to the PFC stage itself and the downstream converter, should the input voltage return abruptly to its rated value. Another problem is the spurious restarts that may occur during converter power down and that cause the output voltage of the converter not to decay to zero monotonically. For these reasons it is usually preferable to shutdown the device in case of brown-out.

Brown-out function is done by sensing the input mains through an internal comparator connected to the RUN pin (#12), connected via a divider to the V_{FF} pin (#5), which delivers a voltage signal proportional to the input mains. The enable and disable thresholds at which the L6563H starts or stops the operation can be adjusted by modifying that divider ratio. For additional information please see [*2*].

Figure 26. EVL6563S-250W TM PFC: startup attempt at 80 Vac-60 Hz - full load

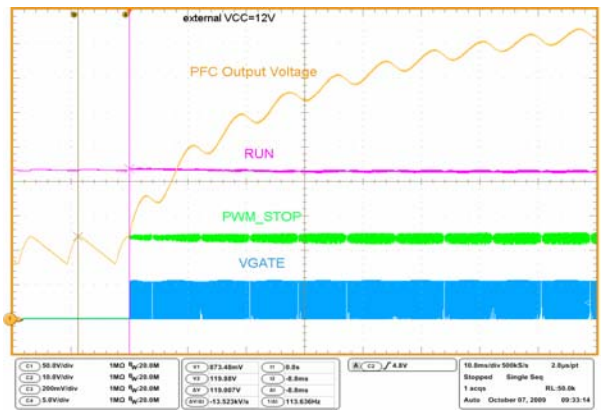


CH1: PFC output voltage
CH2: Vcc voltage (pin #16)
CH3: RUN (pin #12)
CH4: gate drive (pin #15)

In *Figure 26* a startup tentative below the threshold is captured. As seen, at startup the RUN pin does not allow the PFC startup even if the Vcc has reached the turn-on threshold. PFC output voltage remains at the peak of the input sinewave.

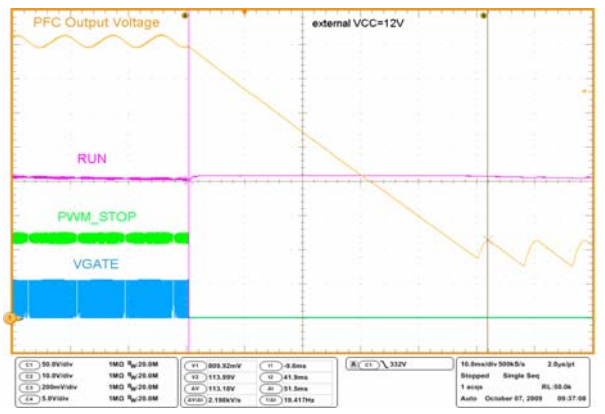
In *Figure 27* and *28* circuit waveforms during brown-out protection operation are shown. In both cases the mains voltage was increased or decreased slowly; as visible both at turn-on or turn-off there are no bouncing or starting attempts by the PFC converter.

Figure 27. EVL6563H-250W TM PFC: startup with slow input voltage increasing - full load



CH1: PFC output voltage
CH2: gate drive (pin #15)
CH3: RUN (pin #10)
CH4: PWM_stop (pin #11)

Figure 28. EVL6563H-250W TM PFC: turn-off with slow input voltage decreasing - full load



CH1: PFC output voltage
CH2: gate drive (pin #15)
CH3: RUN (pin #10)
CH4: PWM_stop (pin #11)

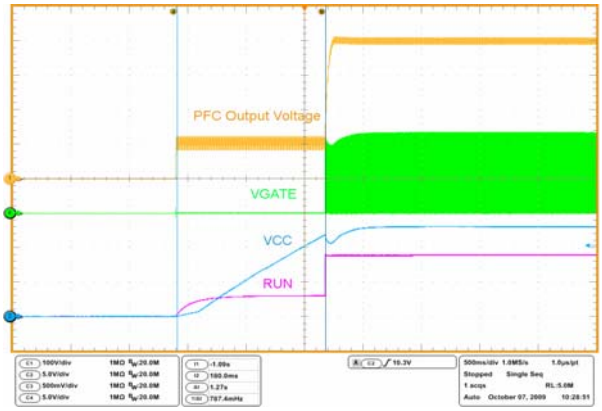
4.4 Startup operation

In the L6563H, a high voltage startup function is implemented. The HVS pin (#9), is directly connected after the rectifier bridge. At startup, an internal high voltage current source is activated and charges C8 and C9 until the L6563H turn-on voltage threshold is reached, then the high voltage current source is automatically turned off. Once the L6563H starts switching it is initially supplied by the Vcc capacitor, and then the transformer auxiliary winding provides the voltage to power the IC. Because the L6563H integrated HV startup circuit is turned off it is not dissipative during the normal operation, therefore it has a significant role to reduce the power consumption when the power supply operates at light load.

In *Figure 29* and *30*, the waveforms during the startup of the circuit at mains plug-in are shown. Notice that the Vcc voltage rises up to the turn-on threshold, and the L6563H starts the operation. Because the high voltage current source delivers a constant current, the wake-up time is almost independent to the input mains voltage.

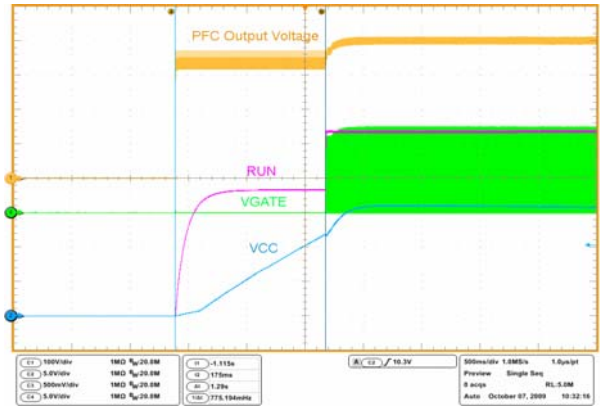
As mentioned previously, for a short time the energy is supplied by the Vcc capacitor, and then the auxiliary winding with the charge pump circuit takes over. At the same time, the output voltage rises from peak value of the rectified mains to the nominal value of the PFC output voltage. The good phase margin of the compensation network allows a clean startup, without any large overshoot.

Figure 29. EVL6563H-250W TM PFC: startup at 90 Vac - 60 Hz - full load



CH1: PFC output voltage
CH2: Vcc voltage (pin #16)
CH3: RUN (pin #12)
CH4: gate drive (pin #15)

Figure 30. EVL6563H-250W TM PFC: startup at 265 Vac - 50 Hz - full load



CH1: PFC output voltage
CH2: Vcc voltage (pin #16)
CH3: RUN (pin #12)
CH4: gate drive (pin #15)

4.5 PFC_OK pin and feedback failure (open-loop) protection

During normal operation, the voltage control loop provides for the output voltage (V_{out}) of the PFC pre-regulator close to its nominal value, set by the resistor ratio of the feedback output divider. In the L6563H the PFC_OK pin (#7) has been dedicated to monitor the output voltage with a separate resistor divider made up of R21, R25, R26 (high) and R33 (low), see *Figure 2*. This divider is selected so that the voltage at the pin reaches 2.5 V if the output voltage exceeds a preset value (VOVP), usually larger than the maximum V_{out} that can be expected, including also worst-case load/line transients.

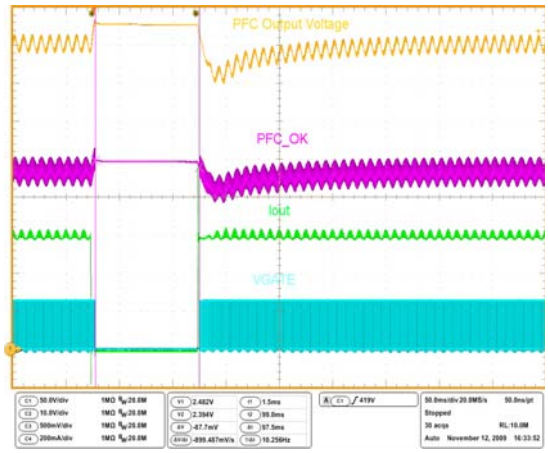
For the EVL6563H-250W we have:

Vo = 400 V, Vovp = 434 V. Select: R21+R25+R26=8.8 MΩ; then:
R33=8.8 MΩ·2.5/(434-2.5)=51 kΩ.

Once this function is triggered, the gate drive activity is immediately stopped until the voltage on the PFC_OK pin drops below 2.4 V. An example is seen in *Figure 31*. Notice that both feedback dividers connected to the L6563H pin (#1) and the PFC_OK pin (#7) can be selected without any constraints. The unique criterion is that both dividers have to sink a current from the output bus which needs to be significantly higher than the current biasing the error amplifier and PFC_OK comparator.

The OVP function described above is able to handle “normal” over voltage conditions, i.e. those resulting from an abrupt load/line change or occurring at startup. In a case where the overvoltage is generated by a feedback disconnection, for instance, when one of the upper resistors of the output divider fails to open, an additional circuitry detects the voltage drop of the INV pin. If the voltage on pin INV is lower than 1.66 V and at the same time the OVP is active, a feedback failure is assumed. Therefore, the gate drive activity is immediately stopped, the device is shut down, its quiescent consumption is reduced below 180 µA and the condition is latched as long as the supply voltage of the L6563H is above the UVLO threshold. To restart the system it is necessary to recycle the input power, so that the Vcc voltage of the L6563H goes below $V_{ccrestart}$. Note that this function offers a complete protection against not only feedback loop failures or erroneous settings, but also against a failure of the protection itself. Either resistor of the PFC_OK divider failing (short or open), or a PFC_OK pin floating, results in shutting down the IC and stopping the pre-regulator. Moreover, the PFC_OK pin doubles its function as a not-latched IC disable; a voltage below 0.23 V shuts down the IC, reducing its consumption below 2 mA. To restart the IC simply let the voltage at the pin go above 0.27 V.

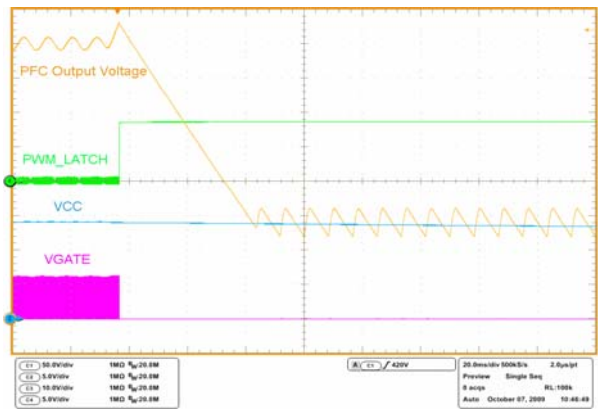
Figure 31. EVL6563H-250W load transient at 115 Vac - 60 Hz - full load to no-load



CH1: PFC output voltage,
CH2: PFC_OK (pin #7),
CH3: gate drive (pin #15),
CH4: Iout

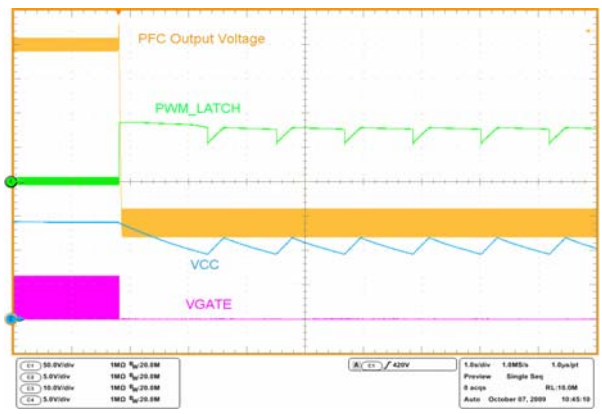
The event of an open-loop is shown in *Figure 32* and *33*; notice the protection intervention latching the operation of the L6563H. In order to keep the L6563H latched after the open-loop detection, in *Figure 33* it is possible to note the activation of the HVS circuit, it's necessary to keep the L6563H correctly supplied, sustaining the Vcc value above the $V_{ccrestart}$ voltage. As mentioned previously, to restart the system it is necessary to recycle the input power. The connection of the HVS pin after the rectifier bridge allows a faster restart in the case of latch than connecting the pin to the bulk capacitor. In that case, in fact, to restart the operation it is necessary to wait the time needed by the HVS to discharge the bulk below the minimum start voltage of the HVS pin ($V_{HVstart}$ on the data sheet) before the Vcc drops below the $V_{ccrestart}$ to resume the operation.

Figure 32. EVL6563H-250W TM PFC: open=-loop at 115 Vac - 60 Hz - full load



CH1: PFC output voltage, CH2: Vcc (pin #16)
CH3: gate drive (pin #15)
CH4: PWM_LATCH (pin#8)

Figure 33. EVL6563H-250W TM PFC: open-loop at 115 Vac - 60 Hz - full load - long acquisition



CH1: PFC output voltage, CH2: Vcc (pin #16)
CH3: gate drive (pin #15)
CH4: PWM_LATCH (pin#8)

4.6 Power management and housekeeping functions

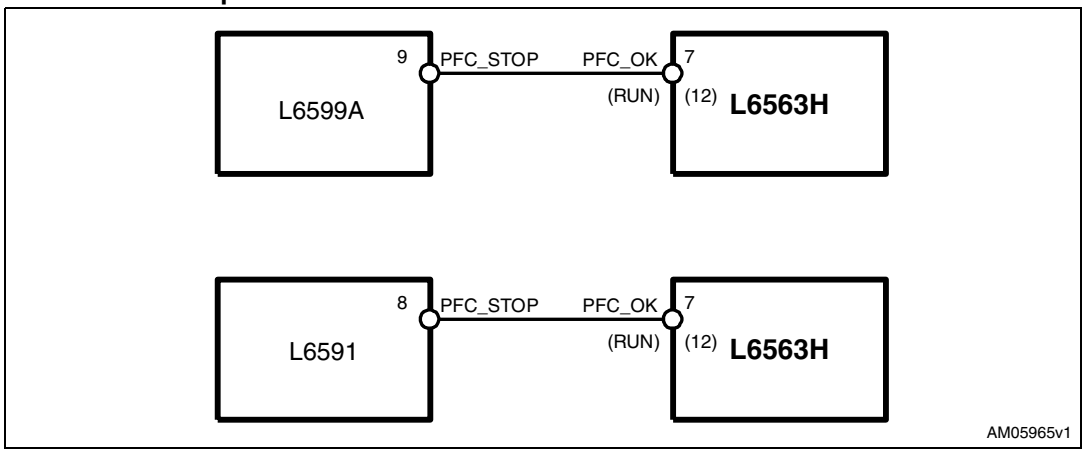
A special feature of the L6563H is that it facilitates the implementation of the “housekeeping” circuitry needed to coordinate the operation of the PFC stage to that of the cascaded DC-DC converter. The functions realized by the housekeeping circuitry ensure that transient conditions like power-up or power-down sequencing or failures of either power stage be properly handled. The L6563H provides some pins to do that.

As already mentioned, one communication line between the L6563H and the PWM controller of the cascaded DC-DC converter is the PWM_LATCH pin (pin #8), which is normally open when the PFC works properly. It goes high if the L6563H loses control of the output voltage (because of a failure of the control loop) with the aim of also latching-off the PWM controller of the cascaded DC-DC converter.

A second communication line can be established via the disable function included in the RUN pin. Typically, this line is used to allow the PWM controller of the cascaded DC-DC converter to shut down the L6563H in case of light load, to minimize the no-load input consumption of the power supply.

Examples of intefacing some ST half-bridges controllers are shown in *Figure 34*.

Figure 34. L6563H on/off control by a cascaded converter controller via PFC_OK or RUN pin



The third communication line is the PWM_STOP pin (#11), which works in conjunction with the RUN pin (#12). The purpose of the PWM_STOP pin is to inhibit the PWM activity of both the PFC stage and the cascaded DC-DC converter. The pin is an open collector, normally open, that goes low if the device is disabled by a voltage lower than 0.8 V on the RUN pin (#12). It is important to point out that this function works correctly in systems where the PFC stage is the master and the cascaded DC-DC converter is the slave or, in other words, where the PFC stage starts first, powers both controllers and enables/disables the operation of the DC-DC stage. This function is quite flexible and can be used in different ways. In systems comprising an auxiliary converter and a main converter (e.g. desktop PC's, silver box or hi-end flat-TVs, or monitors), where the auxiliary converter also powers the controllers of the main converter, the RUN pin (#12) can be used to start and stop the main converter. In the simplest case, to enable/disable the PWM controller the PWM_STOP pin (#11) can be connected to either the output of the error amplifier or, if the chip is provided, with it, to its soft-start pin. The EVL6563H-250W offers the possibility to test these function by connecting it to the cascaded converter via the R30, R31, R32 series resistors. Regarding the PWM_STOP pin (#11) which is an open collector type, if it needs a pull-up resistor, please connect it close to the cascaded PWM for better noise immunity.

Figure 35. Interface circuits that allow the L6563H to switch on or off a PWM controller - not latched

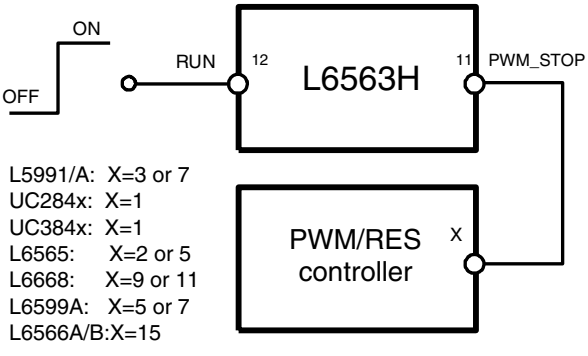
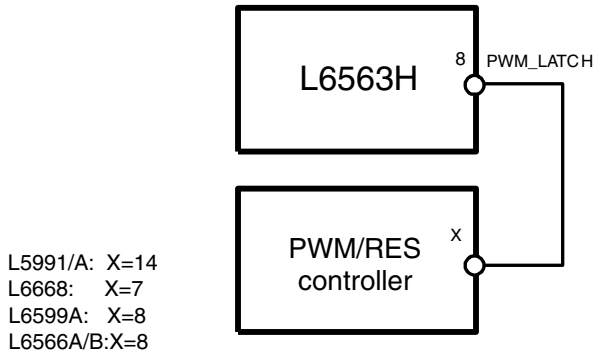


Figure 36. Interface circuits that allow the L6563H to switch on or off a PWM controller - latched



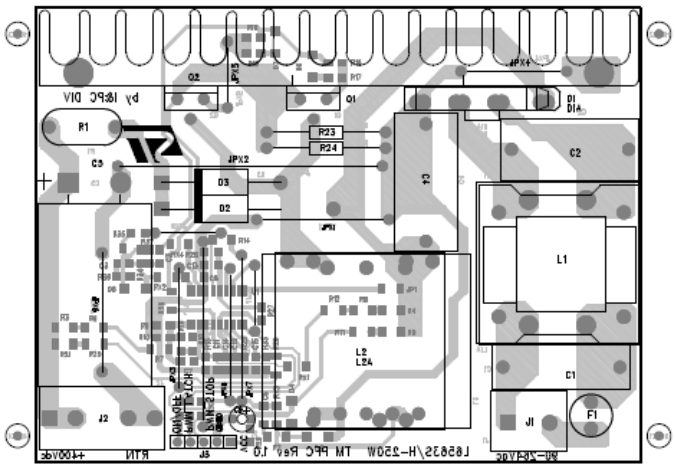
5 Layout hints

The layout of any converter is a very important phase in the design process needing attention by the design engineers as any other design phase. Even if the layout phase looks sometimes time consuming, a good layout surely saves time during the functional debugging and the qualification phases. Additionally, a power supply circuit with a correct layout needs smaller EMI filters or less filter stages and so it allows a consistent cost saving.

Converters using the L6563H do not need any special or specific layout rule to be followed; just the general layout rules for any power converter which must be applied carefully. the basic rules are listed below; they can be used for other PFC circuits having any power level, working either in transition mode or with a fixed off-time control.

1. Keep power and signal RTN separated. Connect the return pins of components carrying high current, such as input filter capacitors, sensing resistors, output capacitors as close as possible. This point is the RTN star point. A downstream converter will have to be connected to this return point.
2. Minimize the length of the traces relevant to the boost inductor, MOSFET drain, boost rectifier and output capacitor.
3. Keep signal components as close as possible to each L6563H relevant pin. to specify, keep the tracks relevant to the pin #1 (INV) net as short as possible. Components and traces relevant to the Error Amplifier must be placed far from traces and connections carrying signals with high dV/dt, like the MOSFET drain. For high power converters or very compact PCB layout a 10 nF capacitor connected to pin #8 (PWM_LATCH) and pin #14 (GND) might be required to decrease the noise picked-up by this pin while it is in its high impedance status.
4. Please connect heat sinks to power GND
5. Add an external copper shield around the boost inductor and connect it to power GND. This shield helps a lot against conducted and radiated noise also
6. Please connect the RTN of the signal components including the feedback, PFC_OK and MULT dividers close to the L6563H pin #14 (GND)
7. Connect a ceramic capacitor (100÷470 nF) to pin #16 (Vcc) and pin #14 (GND), close to the L6563H. Connect this point to the RTN star point (see *1*).

Figure 37. EVL6563H-250W TM PFC: PCB layout (SMT side view)



6 Thermal map

In order to check the design reliability, a thermal mapping by means of an IR camera was done. The thermal measures of the board, component side, at nominal input voltage are shown in *Figure 38* and *39*. Some pointers, visible in the images, have been placed across key components or components showing high temperature. The ambient temperature during both measurements was 27 °C. It is possible to note that the PFC part has different temperatures depending on the input mains.

Figure 38. Thermal map at 115 Vac - 60 Hz - full load - PCB top side

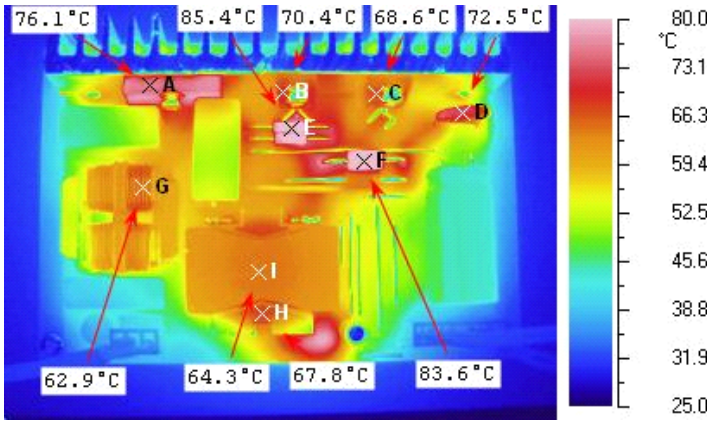


Figure 39. Thermal map at 230 Vac - 50 Hz - full load - PCB top side

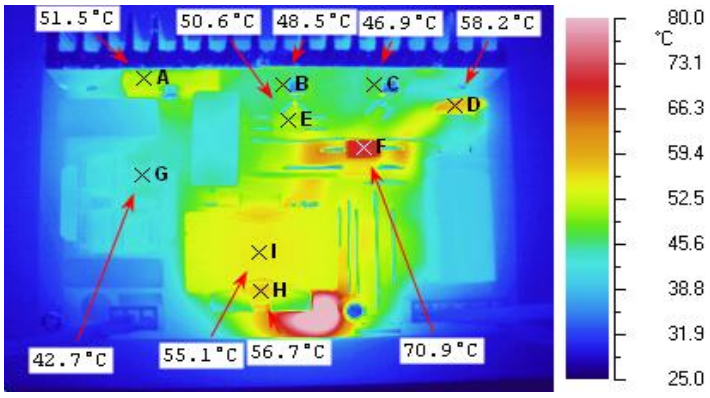


Table 2. Thermal maps reference points - PCB top side

Point	Reference	Description
A	D1	Bridge rectifier
B	Q1	PFC MOSFET
C	Q2	PFC MOSFET
D	R1	NTC thermistor
E	R23 and R24	Sense resistors
F	D3	PFC boost rectifier
G	L1	EMI filtering inductor
H	L2	PFC inductor - core
I	L2	PFC inductor - winding

7 EMI filtering and conducted EMI pre-compliance measurements

The following figures show the measurement in average mode of the conducted noise at full load and nominal mains voltages for both mains lines. The limits shown in the diagrams are EN55022 class-B which is the most popular regulation for domestic equipment using a two-wire mains connection.

It is worth remembering that typically a PFC produces a significant differential mode noise with respect to other topologies. In case an additional margin, with respect to the limits, is needed, increasing the differential attenuation by increasing the across the line (X) capacitors or the C4 capacitor after the rectifier bridge is suggested. Sometimes a differential mode coil connected as a pi-filter placed after, between the bridge rectifier and the boost stage, is more effective and cheaper than increasing the size of the common mode filter coil that would only filter the differential mode noise by the leakage inductance between the two windings.

To recognize if the circuit is affected by common mode or differential mode noise, it is sufficient to compare the spectrum of phase and neutral line measurements; if the two measurements are very similar, the noise is almost totally common mode. If there is a significant difference between the two measurement spectrums, their difference represents the amount of differential mode noise. Of course to get a reliable comparison the two measurements must be done in the same conditions.

Because the differential mode produces common mode noise by the magnetic field induced by the current, decreasing the differential mode consequently limits the second one.

As visible in the diagrams, in all test conditions there is at least a 6dB margin of the measurements with respect to the limits. The measurements have been done in AVG detection to evaluate the benefit of the jittering effect of the TM control.

Figure 40. EVL6563H-250W CE AVG measurement at 115 Vac-60 Hz - full load - phase wire

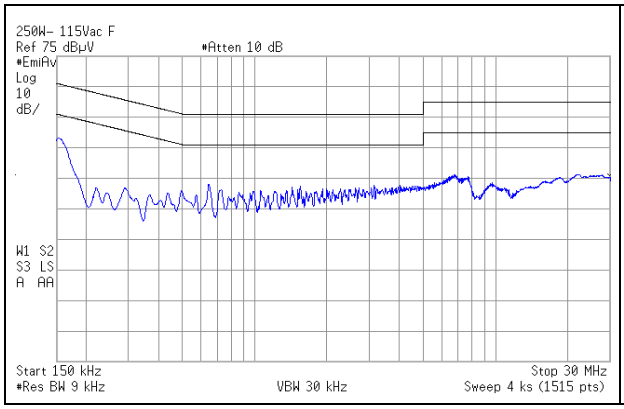


Figure 41. EVL6563H-250W CE AVG measurement at 115 Vac-60 Hz - full load - neutral wire

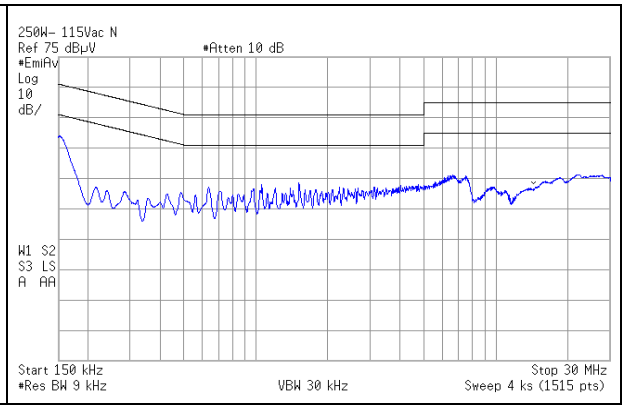


Figure 42. EVL6563H-250W CE AVG measurement at 230 Vac-50 Hz - full load - phase wire

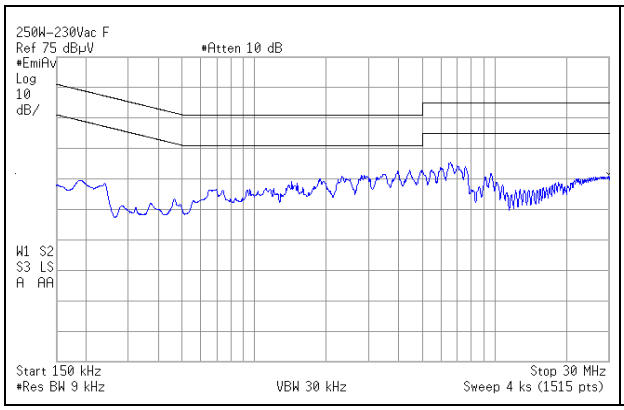
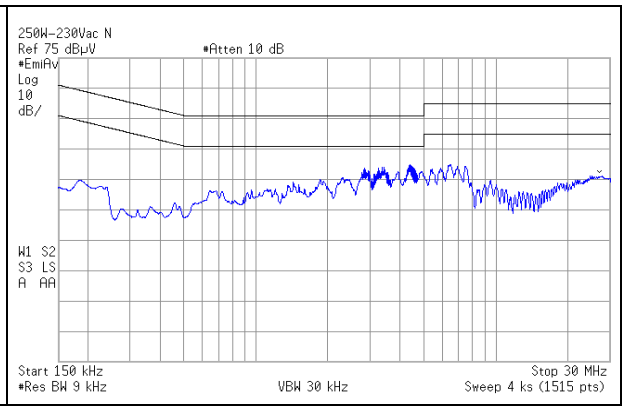


Figure 43. EVL6563H-250W CE AVG measurement at 230 Vac-50 Hz - full load - neutral wire



8 References

1. L6563H datasheet
2. AN3027 “How to design a TM PFC pre-regulator with L6563S and L6563H”

9 Revision history

Table 3. Document revision history

Date	Revision	Changes
29-Jun-2010	1	Initial release.
26-Nov-2010	2	Update *Chapter 1 on page 4*, *Chapter 4.5 on page 20*.

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