

## ACML-7400, ACML-7410, and ACML-7420

### 3.3V/5V 100-MBd High-Speed CMOS Digital Isolator

#### Description

The Broadcom® ACML-7400, ACML-7410, and ACML-7420 are multi-channel, high-speed CMOS digital isolators. Using magnetic coupling through a thick insulation barrier, the isolators enable high speed transmissions without compromise in isolation performance. These isolators consume low power even at high data rates, yet provide excellent transient immunity performance in compact surface-mount packages. The devices are qualified to a maximum propagation delay of 36 ns and a maximum pulse width distortion of 3 ns. They are capable of running at a 100 MBaud data rate.

ACML-7400, ACML-7410, and ACML-7420 are available in 16-pin SOIC wide-body packages. They operate at dual 3.3V/5V supply voltages. The DC and timing specifications are specified over the temperature range of  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ . ACML-7400, ACML-7410, and ACML-7420 are built using CMOS input buffers and CMOS output drivers to eliminate the need for both input limiters and output pull-up resistors. Refresh circuitry is built in to ensure DC-correctness.

#### Applications

- Isolated data interfaces
- Data acquisition
- Digital oscilloscopes
- Power meters
- High speed video transmission

#### Features

- Dual supply voltage compatible – 3.3V and 5V
- Wide operating temperature range ( $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ )
- Support high speed data rate of at least 100 MBd
- Lower power consumption – 15 mA per channel typical
- Low propagation delay: 36 ns max.
- Low propagation delay skew
  - Channel-to-channel: 4 ns max.
  - Part-to-part: 8 ns max.
- Low pulse width distortion: 3 ns max.
- Safety and regulatory approvals
  - UL Recognised
    - 5600  $V_{\text{RMS}}$  for 1 min. per UL1577
    - CSA Component Acceptance Notice #5
  - IEC 60950-1
    - Basic Insulation, 800  $V_{\text{RMS}}$  max. working voltage
    - Reinforced Insulation, 400  $V_{\text{RMS}}$  max. working voltage
  - IEC 61010-1
    - Basic Insulation, 800  $V_{\text{RMS}}$  max. working voltage
    - Reinforced Insulation, 400  $V_{\text{RMS}}$  max. working voltage
  - IEC 60601-1
    - Two means of patient protection, 250  $V_{\text{RMS}}$  max. working voltage
    - Two means of operator protection, 400  $V_{\text{RMS}}$  max. working voltage
- High common mode transient immunity: 75 kV/ $\mu\text{s}$  min.
- CMOS buffer input and output
- DC correctness
- Lead-free

**CAUTION!** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation that may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Device Selection Guide

| Device Number | Channel Configuration     | Package                         |
|---------------|---------------------------|---------------------------------|
| ACML-7400     | Quad, All-in-One          | 16-pin Small Outline, Wide Body |
| ACML-7410     | Quad, Bi-directional, 3/1 | 16-pin Small Outline, Wide Body |
| ACML-7420     | Quad, Bi-directional, 2/2 | 16-pin Small Outline, Wide Body |

Ordering Information

ACML-7400, ACML-7410, and ACML-7420 are UL Recognized with 5600 V<sub>RMS</sub> for 1 minute per UL1577.

| Part Number | Option         | Package         | Surface Mount | Tape and Reel | UL 5600 V <sub>RMS</sub> / 1 Minute rating | Quantity     |
|-------------|----------------|-----------------|---------------|---------------|--------------------------------------------|--------------|
|             | RoHS Compliant |                 |               |               |                                            |              |
| ACML-7400   | -000E          | Wide Body SO-16 | X             |               | X                                          | 45 per tube  |
| ACML-7410   | -500E          |                 | X             | X             | X                                          | 850 per reel |
| ACML-7420   |                |                 |               |               |                                            |              |

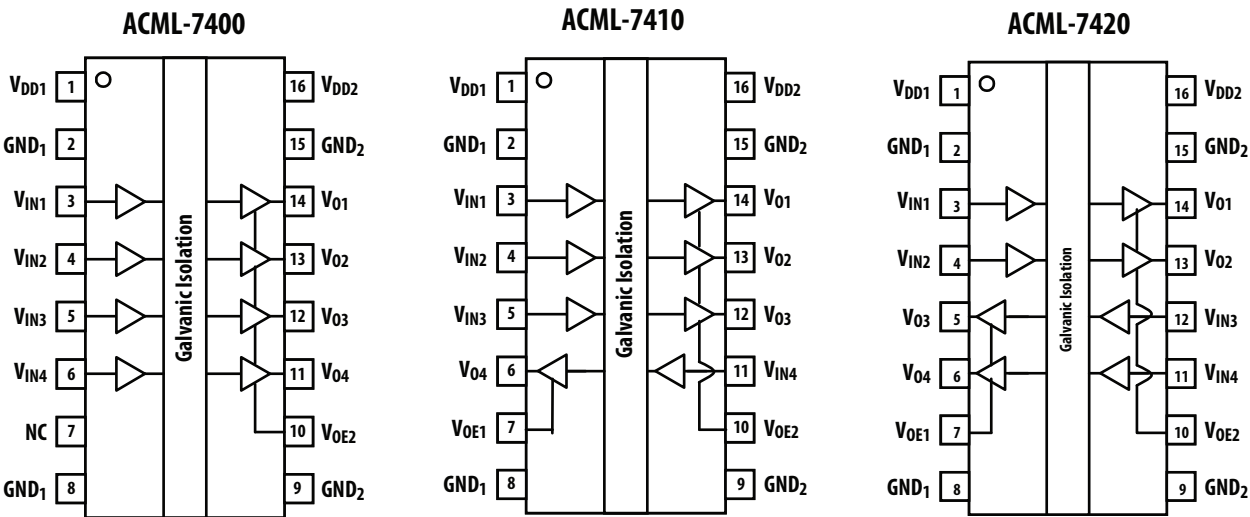
To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACML-7420-500E to order product of Wide Body SO-16 package in Tape and Reel in RoHS compliant.

Functional Diagram

Quad Channel



## Pin Description

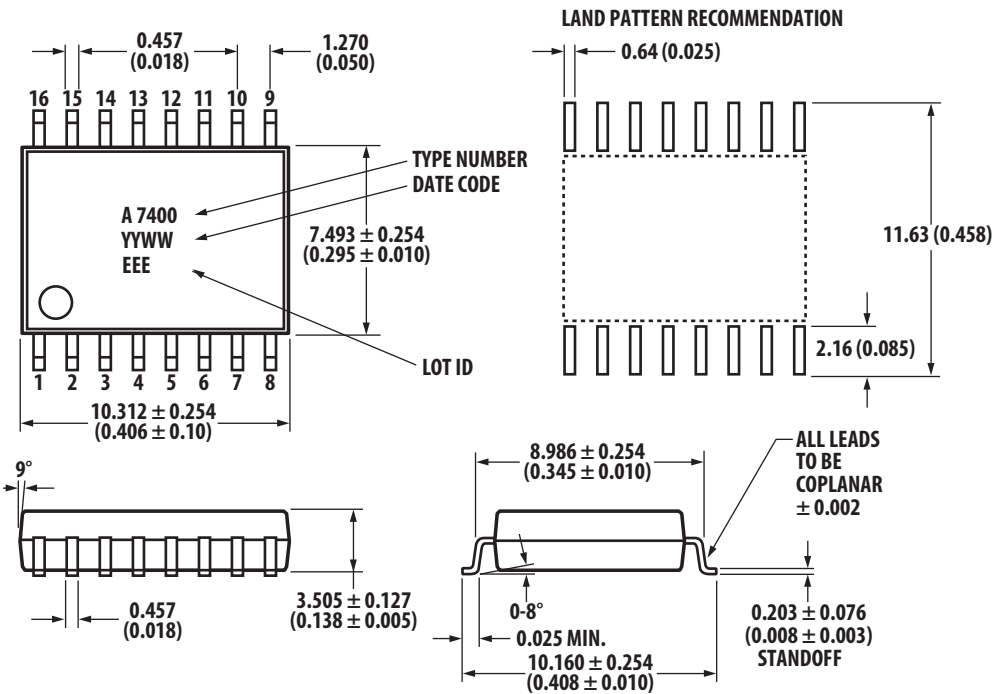
| Pin                                           | Description                                                                                                          |
|-----------------------------------------------|----------------------------------------------------------------------------------------------------------------------|
| $V_{DD1}$ , $V_{DD2}$                         | Power supply at primary and secondary side                                                                           |
| $GND_1$ , $GND_2$                             | Ground at primary and secondary side                                                                                 |
| $V_{IN1}$ , $V_{IN2}$ , $V_{IN3}$ , $V_{IN4}$ | Input for channel 1, 2, 3, and 4                                                                                     |
| $V_{O1}$ , $V_{O2}$ , $V_{O3}$ , $V_{O4}$     | Output for channel 1, 2, 3, and 4                                                                                    |
| $V_{OE1}$ , $V_{OE2}$                         | Output enable at $V_{DD1}$ and $V_{DD2}$ side, these pins should be connected to the respective VDD when not in use. |
| NC                                            | No connectivity                                                                                                      |

## Truth Table (ACML-7410)

| $V_{DD1}$ | $V_{IN1, IN2, IN3}$ | $V_{OE1}$ | $V_{O4}$ | $V_{DD2}$ | $V_{IN4}$ | $V_{OE2}$ | $V_{O1, O2, O3}$ | Remark                                                                                                                                                                                    |
|-----------|---------------------|-----------|----------|-----------|-----------|-----------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| H         | H                   | X         | X        | H         | X         | H or NC   | H                | Input ( $V_{IN1}$ , $IN2$ , $IN3$ ) logic High during normal operation. The enable ( $V_{OE2}$ ) default state is High.                                                                   |
| H         | L                   | X         | X        | H         | X         | H or NC   | L                | Input ( $V_{IN1}$ , $IN2$ , $IN3$ ) logic Low during normal operation. The enable ( $V_{OE2}$ ) default state is High.                                                                    |
| H         | X                   | X         | X        | H         | X         | L         | Z                | Output ( $V_{O1}$ , $O2$ , $O3$ ) is disabled to high impedance state when $V_{OE2}$ is set to Low.                                                                                       |
| L         | X                   | X         | X        | H         | X         | H         | H                | When $V_{DD1}$ is not powered, the output ( $V_{O1}$ , $O2$ , $O3$ ) default state is High. Output ( $V_{O1}$ , $O2$ , $O3$ ) typically restored 100 $\mu$ s after $V_{DD1}$ is restored. |
| H         | X                   | H or NC   | H        | H         | H         | X         | X                | Input ( $V_{IN4}$ ) logic High during normal operation. The enable ( $V_{OE1}$ ) default state is High.                                                                                   |
| H         | X                   | H or NC   | L        | H         | L         | X         | X                | Input ( $V_{IN4}$ ) logic Low during normal operation. The enable ( $V_{OE1}$ ) default state is High.                                                                                    |
| H         | X                   | L         | Z        | H         | X         | X         | X                | Output ( $V_{O4}$ ) is disabled to high impedance state when $V_{OE1}$ is set to Low.                                                                                                     |
| H         | X                   | H         | H        | L         | X         | X         | X                | When $V_{DD2}$ is not powered, the output ( $V_{O4}$ ) default state is High. Output ( $V_{O4}$ ) typically restored 100 ms after $V_{DD2}$ is restored.                                  |

Package Outline Drawings

ACML-7400, ACML-7410 and ACML-7420 16-Lead Surface Mount (SOIC-16) Package



DIMENSIONS IN MILLIMETERS AND (INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-halide flux should be used.

Regulatory Information

The ACML-7400, ACML-7410 and ACML-7420 are approved by the following organizations.

|     |                                              |
|-----|----------------------------------------------|
| UL  | UL1577, component recognition program.       |
| CSA | CSA Component Acceptance Service Notice #5A. |

TUV Rhelndland

| Insulation Category | IEC 60950-1                                      |                                                   | IEC 61010-1                                      |                                                   | IEC 60601-1                                      |                                                  |
|---------------------|--------------------------------------------------|---------------------------------------------------|--------------------------------------------------|---------------------------------------------------|--------------------------------------------------|--------------------------------------------------|
|                     | Reinforced                                       | Basic                                             | Reinforced                                       | Basic                                             | 2 Means of Patient Protection                    | 2 Means of Operator Protection                   |
| Working Voltage     | 400 V <sub>RMS</sub><br>(567 V <sub>PEAK</sub> ) | 800 V <sub>RMS</sub><br>(1132 V <sub>PEAK</sub> ) | 400 V <sub>RMS</sub><br>(567 V <sub>PEAK</sub> ) | 800 V <sub>RMS</sub><br>(1132 V <sub>PEAK</sub> ) | 250 V <sub>RMS</sub><br>(354 V <sub>PEAK</sub> ) | 400 V <sub>RMS</sub><br>(567 V <sub>PEAK</sub> ) |

## Insulation and Safety-Related Specifications

| Parameter                                         | Symbol | ACML-7400<br>ACML-7410<br>ACML-7420 | Units | Conditions                                                                                                                         |
|---------------------------------------------------|--------|-------------------------------------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| Minimum External Air Gap (Clearance)              | L(101) | 8.1                                 | mm    | Measured from input terminals to output terminals, shortest distance through air.                                                  |
| Minimum External Tracking (Creepage)              | L(102) | 8.1                                 | mm    | Measured from input terminals to output terminals, shortest distance path along body.                                              |
| Minimum Internal Plastic Gap (Internal Clearance) |        | 0.05                                | mm    | Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector. |
| Tracking Resistance (Comparative Tracking Index)  | CTI    | >175                                | V     | DIN IEC 112/VDE 0303 Part 1                                                                                                        |
| Isolation Group                                   |        | IIla                                |       | Material Group (DIN VDE 0110, 1/89, Table 1)                                                                                       |

All creepage and clearance pertain to the isolation component itself. These dimensions are needed as a starting point for the designer when determining the circuit insulation requirements, and not reflective of the equipment standard requirements.

**NOTE:** These isolators are suitable for *safe electrical isolation* only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

## Absolute Maximum Ratings

| Parameter                         |                     | Symbol                                    | Min. | Max.                 | Units |
|-----------------------------------|---------------------|-------------------------------------------|------|----------------------|-------|
| Storage Temperature               |                     | T <sub>S</sub>                            | −55  | +125                 | °C    |
| Ambient Operating Temperature     |                     | T <sub>A</sub>                            | −40  | +125                 | °C    |
| Supply Voltages                   |                     | V <sub>DD1</sub> , V <sub>DD2</sub>       | 0    | 6.5                  | Volts |
| Input Voltage                     |                     | V <sub>I</sub>                            | −0.5 | V <sub>DD</sub> +0.5 | Volts |
| Output Voltage                    |                     | V <sub>O</sub>                            | −0.5 | V <sub>DD</sub> +0.5 | Volts |
| Average Output Current            |                     | I <sub>O</sub>                            | —    | ±15                  | mA    |
| Electrostatic Discharge           | Human Body Model    | HBM                                       | —    | ±4                   | kV    |
|                                   | Charge Device Model | CDM                                       | —    | ±1                   | kV    |
| Solder Reflow Temperature Profile |                     | See the Solder Reflow Temperature Profile |      |                      |       |

## Recommended Operating Conditions

| Parameter                         | Symbol             | Min.                | Max.                | Units | Notes |
|-----------------------------------|--------------------|---------------------|---------------------|-------|-------|
| Ambient Operating Temperature     | $T_A$              | -40                 | +105                | °C    |       |
| Supply Voltages ( 3.3V operation) | $V_{DD1}, V_{DD2}$ | 3.0                 | 3.6                 | V     |       |
| Supply Voltages (5V operation)    | $V_{DD1}, V_{DD2}$ | 4.5                 | 5.5                 | V     |       |
| Logic High Input Voltage          | $V_{IH}$           | $0.7 \times V_{DD}$ | $V_{DD}$            | V     |       |
| Logic Low Input Voltage           | $V_{IL}$           | 0.0                 | $0.3 \times V_{DD}$ | V     |       |

# Electrical Specifications

## ACML-7400

The following specifications apply to ACML-7400 and are applicable to ambient temperature of  $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ , input supply of  $3.0\text{V} \leq V_{DD1} \leq 3.6\text{V}$  or  $4.5\text{V} \leq V_{DD1} \leq 5.5\text{V}$ , and output supply of  $3.0\text{V} \leq V_{DD2} \leq 3.6\text{V}$  or  $4.5\text{V} \leq V_{DD2} \leq 5.5\text{V}$ . All typical specifications at  $T_A = +25^{\circ}\text{C}$ .

| Parameter                                | Symbol                | Min.                  | Typ.                   | Max. | Unit | Test Conditions                                               |                       | Figure | Notes |
|------------------------------------------|-----------------------|-----------------------|------------------------|------|------|---------------------------------------------------------------|-----------------------|--------|-------|
| Input Supply Current, No data            | I <sub>DD1(0)</sub>   | —                     | 5.9 <sup>a</sup>       | 10   | mA   |                                                               | No Input              | 1, 7   | b     |
|                                          |                       |                       | 6.8 <sup>c</sup>       |      |      | V <sub>DD1</sub> = 5.5V                                       |                       |        |       |
| Input Supply Current, 25 MBd data rate   | I <sub>DD1(25)</sub>  | —                     | 16                     | —    | mA   | V <sub>DD1</sub> = 3.3V                                       | 12.5-MHz logic signal | 1, 7   | d     |
|                                          |                       |                       | 17                     |      |      | V <sub>DD1</sub> = 5.0V                                       |                       |        |       |
| Input Supply Current, 100 MBd data rate  | I <sub>DD1(100)</sub> | —                     | 30 <sup>a</sup>        | 40   | mA   | V <sub>DD1</sub> = 3.6V                                       | 50-MHz logic signal   | 1, 7   | d     |
|                                          |                       |                       | 31 <sup>c</sup>        | 40   |      | V <sub>DD1</sub> = 5.5V                                       |                       |        |       |
| Output Supply Current, No data           | I <sub>DD2(0)</sub>   | —                     | 12 <sup>a</sup>        | 16   | mA   |                                                               | No Input              | 2, 8   | e     |
|                                          |                       |                       | 13 <sup>c</sup>        |      |      | V <sub>DD1</sub> = 5.5V                                       |                       |        |       |
| Output Supply Current, 25 MBd            | I <sub>DD2(25)</sub>  | —                     | 15                     | —    | mA   | V <sub>DD1</sub> = 3.3V                                       | 12.5-MHz logic signal | 2, 8   | f     |
|                                          |                       |                       | 17                     |      |      | V <sub>DD1</sub> = 5.0V                                       |                       |        |       |
| Output Supply Current, 100 MBd data rate | I <sub>DD2(100)</sub> | —                     | 23 <sup>a</sup>        | 32   | mA   | V <sub>DD1</sub> = 3.6V                                       | 50-MHz logic signal   | 2, 8   | f     |
|                                          |                       |                       | 30 <sup>c</sup>        | 40   |      | V <sub>DD1</sub> = 5.5V                                       |                       |        |       |
| Logic Input Current                      | I <sub>IN</sub>       | −10                   | —                      | 10   | μA   |                                                               |                       |        |       |
| Logic High Output Voltage                | V <sub>OH</sub>       | V <sub>DD</sub> − 0.1 | V <sub>DD</sub> − 0.02 | —    | V    | I <sub>OUT</sub> = −20 μA, V <sub>IN</sub> = V <sub>DD1</sub> |                       |        |       |
|                                          |                       | 0.8 × V <sub>DD</sub> | V <sub>DD</sub> − 0.25 | —    | V    | I <sub>OUT</sub> = −4 mA, V <sub>IN</sub> = V <sub>DD1</sub>  |                       |        |       |
| Logic Low Output Voltage                 | V <sub>OL</sub>       | −                     | 0.02                   | 0.1  | V    | I <sub>OUT</sub> = 20 μA, V <sub>IN</sub> = 0V                |                       |        |       |
|                                          |                       |                       | 0.25                   | 0.8  | V    | I <sub>OUT</sub> = 4 mA, V <sub>IN</sub> = 0V                 |                       |        |       |

a. Typical data based on 3.3V supply.

b.  $I_{DD1(0)}$  is the supply current consumption at  $V_{DD1}$  when there is no signal to all inputs.

c. Typical data based on 5.0V supply.

d.  $I_{DD1(F)}$  is the supply current consumption at  $V_{DD1}$  when inputs are switching at the specified data rate, and outputs are switching at same data rate with no load.

e.  $I_{DD2(0)}$  is the supply current consumption at  $V_{DD2}$  when there is no signal to all inputs.

f.  $I_{DD2(F)}$  is the supply current consumption at  $V_{DD2}$  when inputs are switching at the specified data rate, and outputs are switching at same data rate with no load.

## ACML-7410

The following specifications apply to ACML-7410 and are applicable to ambient temperature of  $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ , input supply of  $3.0\text{V} \leq V_{DD1} \leq 3.6\text{V}$  or  $4.5\text{V} \leq V_{DD1} \leq 5.5\text{V}$ , and output supply of  $3.0\text{V} \leq V_{DD2} \leq 3.6\text{V}$  or  $4.5\text{V} \leq V_{DD2} \leq 5.5\text{V}$ . All typical specifications at  $T_A = +25^{\circ}\text{C}$ .

| Parameter                                | Symbol                | Min.                  | Typ.                   | Max. | Unit | Test Conditions                                               |                       | Figure | Notes |
|------------------------------------------|-----------------------|-----------------------|------------------------|------|------|---------------------------------------------------------------|-----------------------|--------|-------|
| Input Supply Current, No data            | I <sub>DD1(0)</sub>   | —                     | 8.4 <sup>a</sup>       | 11.5 | mA   |                                                               | No Input              | 3, 7   | b     |
|                                          |                       |                       | 9.4 <sup>c</sup>       |      |      | V <sub>DD1</sub> = 5.5V                                       |                       |        |       |
| Input Supply Current, 25 MBd data rate   | I <sub>DD1(25)</sub>  | —                     | 15.5 <sup>a</sup>      | —    | mA   | V <sub>DD1</sub> = 3.3V                                       | 12.5-MHz logic signal | 3, 7   | d     |
|                                          |                       |                       | 17 <sup>c</sup>        | —    |      | V <sub>DD1</sub> = 5.0V                                       |                       |        |       |
| Input Supply Current, 100 MBd data rate  | I <sub>DD1(100)</sub> | —                     | 28.5 <sup>a</sup>      | 40   | mA   | V <sub>DD1</sub> = 3.6V                                       | 50-MHz logic signal   | 3, 7   | d     |
|                                          |                       |                       | 30.5 <sup>c</sup>      | 40   |      | V <sub>DD1</sub> = 5.5V                                       |                       |        |       |
| Output Supply Current, No data           | I <sub>DD2(0)</sub>   | —                     | 9.5 <sup>a</sup>       | 16   | mA   |                                                               | No Input              | 4, 8   | e     |
|                                          |                       |                       | 10.4 <sup>c</sup>      | —    |      | V <sub>DD1</sub> = 5.5V                                       |                       |        |       |
| Output Supply Current, 25 MBd            | I <sub>DD2(25)</sub>  | —                     | 15 <sup>a</sup>        | —    | mA   | V <sub>DD1</sub> = 3.3V                                       | 12.5-MHz logic signal | 4, 8   | f     |
|                                          |                       |                       | 17 <sup>c</sup>        | —    |      | V <sub>DD1</sub> = 5.0V                                       |                       |        |       |
| Output Supply Current, 100 MBd data rate | I <sub>DD2(100)</sub> | —                     | 25 <sup>a</sup>        | 34   | mA   | V <sub>DD1</sub> = 3.6V                                       | 50-MHz logic signal   | 4, 8   | f     |
|                                          |                       |                       | 30 <sup>c</sup>        | 40   |      | V <sub>DD1</sub> = 5.5V                                       |                       |        |       |
| Logic Input Current                      | I <sub>IN</sub>       | −10                   | —                      | 10   | μA   |                                                               |                       |        |       |
| Logic High Output Voltage                | V <sub>OH</sub>       | V <sub>DD</sub> − 0.1 | V <sub>DD</sub> − 0.02 | —    | V    | I <sub>OUT</sub> = −20 μA, V <sub>IN</sub> = V <sub>DD1</sub> |                       |        |       |
|                                          |                       | 0.8 × V <sub>DD</sub> | V <sub>DD</sub> − 0.25 | —    | V    | I <sub>OUT</sub> = −4 mA, V <sub>IN</sub> = V <sub>DD1</sub>  |                       |        |       |
| Logic Low Output Voltage                 | V <sub>OL</sub>       | −                     | 0.02                   | 0.1  | V    | I <sub>OUT</sub> = 20 μA, V <sub>IN</sub> = 0V                |                       |        |       |
|                                          |                       |                       | 0.25                   | 0.8  | V    | I <sub>OUT</sub> = 4 mA, V <sub>IN</sub> = 0V                 |                       |        |       |

- Typical data based on 3.3V supply.
- $I_{DD1(0)}$  is the supply current consumption at  $V_{DD1}$  when there is no signal to all inputs.
- Typical data based on 5.0V supply.
- $I_{DD1(F)}$  is the supply current consumption at  $V_{DD1}$  when inputs are switching at the specified data rate, and outputs are switching at same data rate with no load.
- $I_{DD2(0)}$  is the supply current consumption at  $V_{DD2}$  when there is no signal to all inputs.
- $I_{DD2(F)}$  is the supply current consumption at  $V_{DD2}$  when inputs are switching at the specified data rate, and outputs are switching at same data rate with no load.

## ACML-7420

The following specifications apply to ACML-7420 and are applicable to ambient temperature of  $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ , input supply of  $3.0\text{V} \leq V_{DD1} \leq 3.6\text{V}$  or  $4.5\text{V} \leq V_{DD1} \leq 5.5\text{V}$ , and output supply of  $3.0\text{V} \leq V_{DD2} \leq 3.6\text{V}$  or  $4.5\text{V} \leq V_{DD2} \leq 5.5\text{V}$ . All typical specifications at  $T_A = +25^{\circ}\text{C}$ .

| Parameter                                | Symbol                | Min.                  | Typ.                   | Max. | Unit | Test Conditions                                               |                       | Figure | Notes |
|------------------------------------------|-----------------------|-----------------------|------------------------|------|------|---------------------------------------------------------------|-----------------------|--------|-------|
| Input Supply Current, No data            | I <sub>DD1(0)</sub>   | —                     | 9.0 <sup>a</sup>       | 13   | mA   |                                                               | No Input              | 5, 7   | b     |
|                                          |                       |                       | 9.9 <sup>c</sup>       |      |      | V <sub>DD1</sub> = 5.5V                                       |                       |        |       |
| Input Supply Current, 25 MBd data rate   | I <sub>DD1(25)</sub>  | —                     | 15 <sup>a</sup>        | —    | mA   | V <sub>DD1</sub> = 3.3V                                       | 12.5-MHz logic signal | 5, 7   | d     |
|                                          |                       |                       | 17 <sup>c</sup>        |      |      | V <sub>DD1</sub> = 5.0V                                       |                       |        |       |
| Input Supply Current, 100 MBd data rate  | I <sub>DD1(100)</sub> | —                     | 27 <sup>a</sup>        | 36   | mA   | V <sub>DD1</sub> = 3.6V                                       | 50-MHz logic signal   | 5, 7   | d     |
|                                          |                       |                       | 30 <sup>c</sup>        | 40   |      | V <sub>DD1</sub> = 5.5V                                       |                       |        |       |
| Output Supply Current, No data           | I <sub>DD2(0)</sub>   | —                     | 9.0 <sup>a</sup>       | 13   | mA   |                                                               | No Input              | 6, 8   | e     |
|                                          |                       |                       | 9.9 <sup>c</sup>       |      |      | V <sub>DD1</sub> = 5.5V                                       |                       |        |       |
| Output Supply Current, 25 MBd            | I <sub>DD2(25)</sub>  | —                     | 15 <sup>a</sup>        | —    | mA   | V <sub>DD1</sub> = 3.3V                                       | 12.5-MHz logic signal | 6, 8   | f     |
|                                          |                       |                       | 17 <sup>c</sup>        |      |      | V <sub>DD1</sub> = 5.0V                                       |                       |        |       |
| Output Supply Current, 100 MBd data rate | I <sub>DD2(100)</sub> | —                     | 27 <sup>a</sup>        | 36   | mA   | V <sub>DD1</sub> = 3.6V                                       | 50-MHz logic signal   | 6, 8   | f     |
|                                          |                       |                       | 30 <sup>c</sup>        | 40   |      | V <sub>DD1</sub> = 5.5V                                       |                       |        |       |
| Logic Input Current                      | I <sub>IN</sub>       | −10                   | —                      | 10   | μA   |                                                               |                       |        |       |
| Logic High Output Voltage                | V <sub>OH</sub>       | V <sub>DD</sub> − 0.1 | V <sub>DD</sub> − 0.02 | —    | V    | I <sub>OUT</sub> = −20 μA, V <sub>IN</sub> = V <sub>DD1</sub> |                       |        |       |
|                                          |                       | 0.8 × V <sub>DD</sub> | V <sub>DD</sub> − 0.25 | —    | V    | I <sub>OUT</sub> = −4 mA, V <sub>IN</sub> = V <sub>DD1</sub>  |                       |        |       |
| Logic Low Output Voltage                 | V <sub>OL</sub>       | −                     | 0.02                   | 0.1  | V    | I <sub>OUT</sub> = 20 μA, V <sub>IN</sub> = 0V                |                       |        |       |
|                                          |                       |                       | 0.25                   | 0.8  | V    | I <sub>OUT</sub> = 4 mA, V <sub>IN</sub> = 0V                 |                       |        |       |

- Typical data based on 3.3V supply.
- $I_{DD1(0)}$  is the supply current consumption at  $V_{DD1}$  when there is no signal to all inputs.
- Typical data based on 5.0V supply.
- $I_{DD1(F)}$  is the supply current consumption at  $V_{DD1}$  when inputs are switching at the specified data rate, and outputs are switching at same data rate with no load.
- $I_{DD2(0)}$  is the supply current consumption at  $V_{DD2}$  when there is no signal to all inputs.
- $I_{DD2(F)}$  is the supply current consumption at  $V_{DD2}$  when inputs are switching at the specified data rate, and outputs are switching at same data rate with no load.

## Switching Specifications

Over the recommended temperature of  $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ , supply voltage of  $3.0\text{V} \leq V_{DD1} \leq 3.6\text{V}$  or  $4.5\text{V} \leq V_{DD1} \leq 5.5\text{V}$ , and of  $3.0\text{V} \leq V_{DD2} \leq 3.6\text{V}$  or  $4.5\text{V} \leq V_{DD2} \leq 5.5\text{V}$ , unless further specified. All typical specifications are at  $T_A = +25^{\circ}\text{C}$ .

| Parameter                                           | Symbol        | Min. | Typ. | Max. | Unit              | Test Conditions                                                                                         | Figure | Notes |
|-----------------------------------------------------|---------------|------|------|------|-------------------|---------------------------------------------------------------------------------------------------------|--------|-------|
| Maximum Data Rate                                   |               | 100  | —    | —    | MBd               | 50-MHz Logic Signal                                                                                     |        |       |
| Minimum Pulse Width                                 |               | —    | —    | 10   | ns                | 50-MHz Logic Signal                                                                                     |        |       |
| Propagation Delay Time to Logic Low Output          | $t_{PHL}$     | 18   | 27   | 32   | ns                | $4.5\text{V} \leq V_{DD1} = V_{DD2} \leq 5.5\text{V}$ , $C_L = 15\text{ pF}$                            | 9      | a     |
| Propagation Delay Time to Logic High Output         | $t_{PLH}$     | 18   | 27   | 32   | ns                |                                                                                                         | 9      | a     |
| Pulse Width Distortion                              | PWD           | -2   | 0    | 2    | ns                |                                                                                                         | 11     | b     |
| Propagation Delay Channel Skew                      | $t_{CSK}$     | —    | 0    | 3    | ns                |                                                                                                         | 12     | c     |
| Propagation Delay Part Skew                         | $t_{PSK}$     | —    | 1    | 5    | ns                |                                                                                                         |        | d     |
| Propagation Delay Time to Logic Low Output          | $t_{PHL}$     | 20   | 28   | 36   | ns                | $C_L = 15\text{ pF}$                                                                                    | 9, 10  | a     |
| Propagation Delay Time to Logic High Output         | $t_{PLH}$     | 20   | 27.5 | 36   | ns                |                                                                                                         | 9, 10  | a     |
| Pulse Width Distortion                              | PWD           | -3   | 0.5  | 3    | ns                |                                                                                                         | 11     | b     |
| Propagation Delay Channel Skew                      | $t_{CSK}$     | —    | 0    | 4    | ns                |                                                                                                         | 12     | c     |
| Propagation Delay Part Skew                         | $t_{PSK}$     | —    | 1    | 8    | ns                |                                                                                                         |        | d     |
| Output Rise Time (10% – 90%)                        | $t_R$         | —    | 3    | —    | ns                | $C_L = 15\text{ pF}$                                                                                    |        |       |
| Output Fall Time (90% - 10%)                        | $t_F$         | —    | 3    | —    | ns                | $C_L = 15\text{ pF}$                                                                                    |        |       |
| Output Enable time                                  | $t_{ENABLE}$  | —    | 10   | —    | ns                | $V_{IN} = 0\text{V}$ or $V_{DD}$                                                                        |        | e     |
| Output Disable time                                 | $t_{DISABLE}$ | —    | 10   | —    | ns                | $V_{IN} = 0\text{V}$ or $V_{DD}$                                                                        |        | f     |
| Common Mode Transient Immunity at Logic High Output | $ CM_H $      | 75   | —    | —    | kV/ $\mu\text{s}$ | $V_{CM} = 1500\text{V}$ , $T_A = 25^{\circ}\text{C}$ ,<br>$V_{IN} = V_{DD}$ , $V_O > 0.8 \times V_{DD}$ |        | g     |
| Common Mode Transient Immunity at Logic Low Output  | $ CM_L $      | 75   | —    | —    | kV/ $\mu\text{s}$ | $V_{CM} = 1500\text{V}$ , $T_A = 25^{\circ}\text{C}$ ,<br>$V_{IN} = 0\text{V}$ , $V_O < 0.8\text{V}$    |        | g     |

- $t_{PHL}$  propagation delay is measured from the 50% level on the falling edge of the  $V_{IN}$  signal to the 50% level of the falling edge of the  $V_{OUT}$  signal.  $t_{PLH}$  propagation delay is measured from the 50% level on the rising edge of the  $V_{IN}$  signal to the 50% level of the rising edge of the  $V_{OUT}$  signal.
- PWD is defined as  $t_{PHL} - t_{PLH}$ .
- $t_{CSK}$  is equal to the magnitude of the worst case difference in  $t_{PHL}$  and/or  $t_{PLH}$  that will be seen between channels of the same unit at any given temperature and supply voltages within the recommended operating conditions.
- $t_{PSK}$  is equal to the magnitude of the worst case difference in  $t_{PHL}$  and/or  $t_{PLH}$  that will be seen between units at any given temperature and supply voltages within the recommended operating conditions.
- $t_{ENABLE}$  is the duration when  $V_{OE}$  is set to High state and output is restored per input signal ( $V_O = V_{IN}$ ).
- $t_{DISABLE}$  is the duration when  $V_{OE}$  is set to Low and  $V_O$  is switched to high impedance state.
- $CM_H$  is the maximum common mode voltage slew rate that can be sustained while maintaining  $V_{OUT} > 0.8 V_{DD2}$ .  $CM_L$  is the maximum common mode input voltage that can be sustained while maintaining  $V_{OUT} < 0.8\text{V}$ . The common mode voltage slew rates apply to both rising and falling common mode voltage edges.

## Package Characteristics

All Typicals at  $T_A = 25^\circ\text{C}$ .

| Parameters                               | Symbol           | Min. | Typ.      | Max. | Unit             | Test Conditions                                              | Notes   |
|------------------------------------------|------------------|------|-----------|------|------------------|--------------------------------------------------------------|---------|
| Input-Output Momentary Withstand Voltage | $V_{\text{ISO}}$ | 5600 | —         | —    | $V_{\text{RMS}}$ | $RH \leq 50\%$ , $t = 1$ minute,<br>$T_A = 25^\circ\text{C}$ | a, b, c |
| Input-Output Resistance                  | $R_{\text{I-O}}$ | —    | $10^{14}$ | —    | $\Omega$         | $V_{\text{I-O}} = 500\text{V dc}$                            | a       |
| Input-Output Capacitance                 | $C_{\text{I-O}}$ | —    | 1.9       | —    | pF               | $f = 1\text{ MHz}$                                           | a       |
| Input Capacitance                        | $C_{\text{I}}$   | —    | 4.3       | —    | pF               |                                                              | d       |
| Package Power Dissipation                | $P_{\text{PD}}$  |      | —         | 750  | mW               | $T_A = 25^\circ\text{C}$                                     |         |

- Device considered a two-terminal device: pins 1, 2, 3, 4, 5, 6, 7, and 8 shorted together and pins 9, 10, 11, 12, 13, 14, 15 and 16 shorted together.
- In accordance with UL1577, each device is proof tested by applying an insulation test voltage  $6800 V_{\text{RMS}}$  for 1 second.
- The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refers to your equipment level safety specification.
- $C_{\text{I}}$  is the capacitance measured at input pin.

## Characteristic Curves

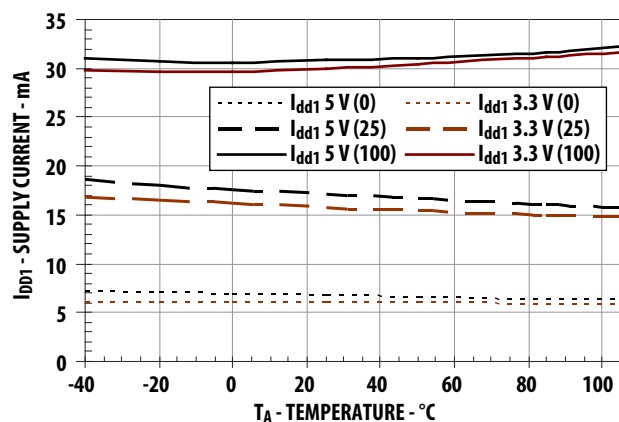
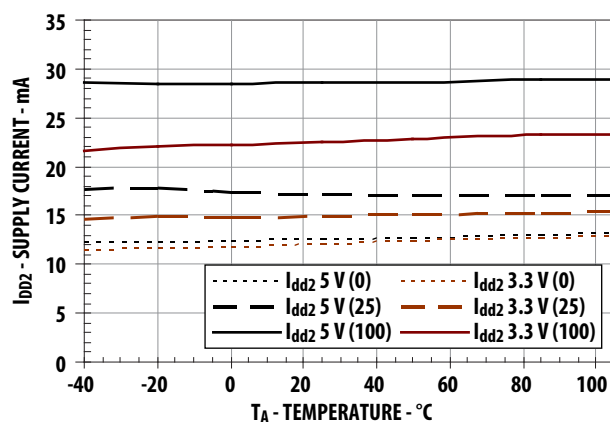
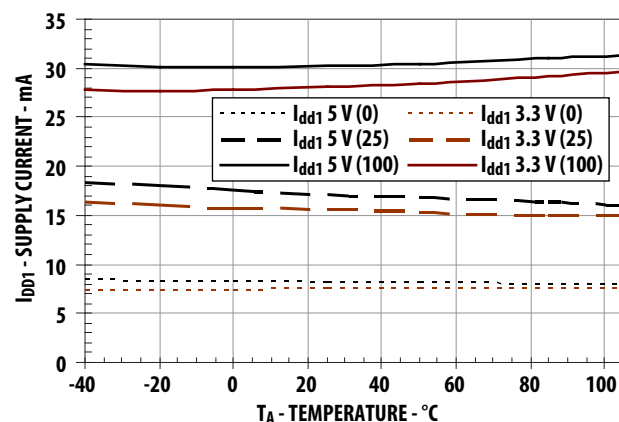
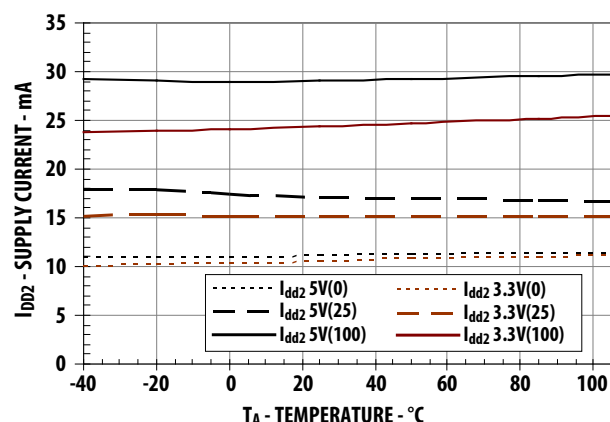
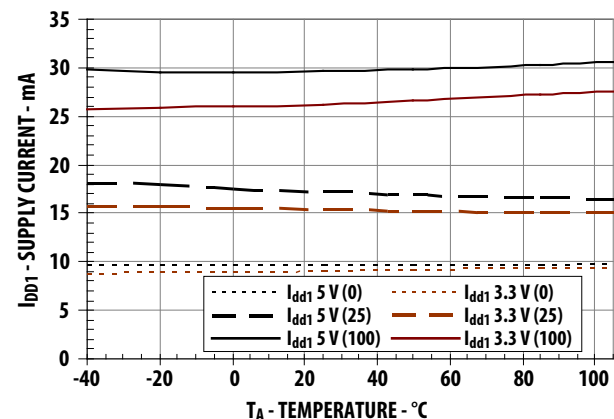
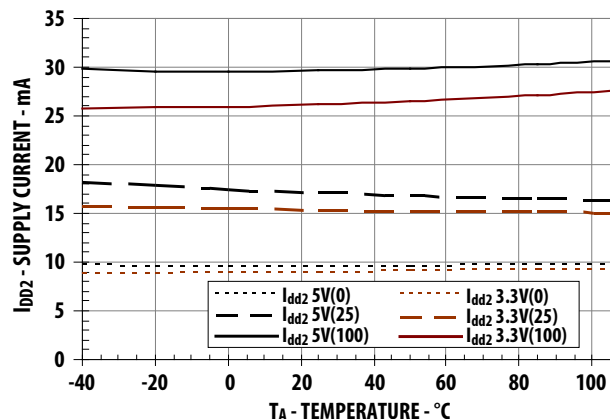
Figure 1: Typical  $I_{DD1}$  of ACML-7400 vs. TemperatureFigure 2: Typical  $I_{DD2}$  of ACML-7400 vs. TemperatureFigure 3: Typical  $I_{DD1}$  of ACML-7410 vs. TemperatureFigure 4: Typical  $I_{DD2}$  of ACML-7410 vs. TemperatureFigure 5: Typical  $I_{DD1}$  of ACML-7420 vs. TemperatureFigure 6: Typical  $I_{DD2}$  of ACML-7420 vs. Temperature

Figure 7: Typical Supply Current per Transmit Channel vs. Data Rate

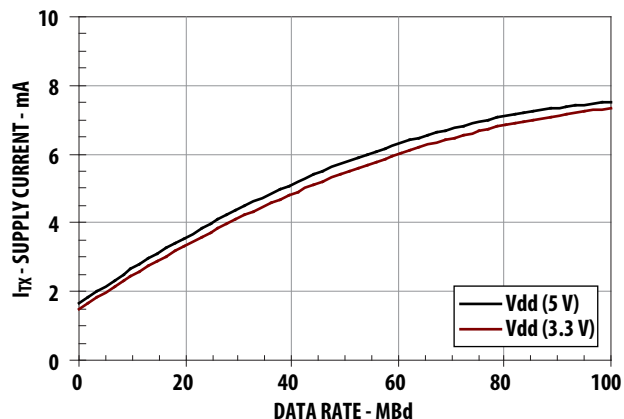


Figure 8: Typical Supply Current per Receive Channel vs. Data Rate

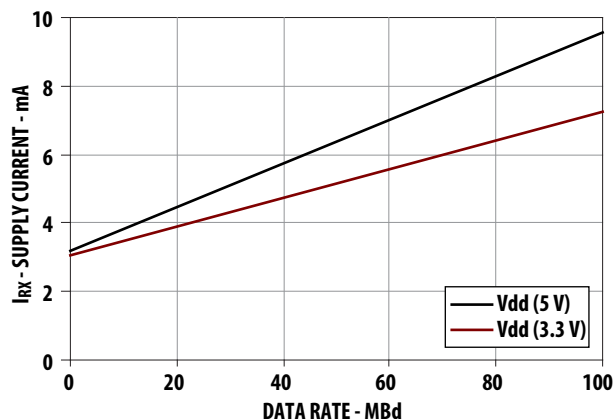


Figure 9: Typical Propagation Delay vs. Temperature

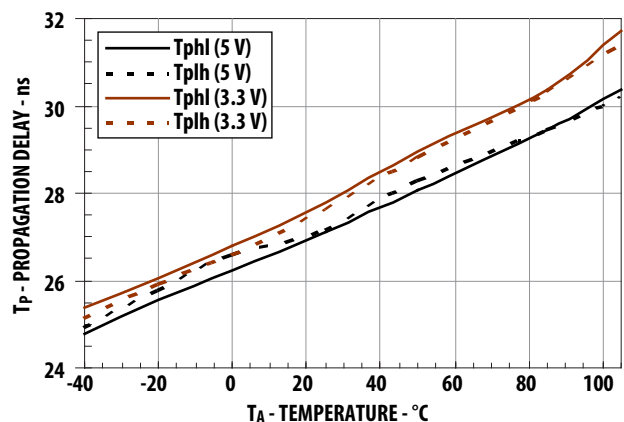


Figure 10: Typical Propagation Delay vs. Temperature

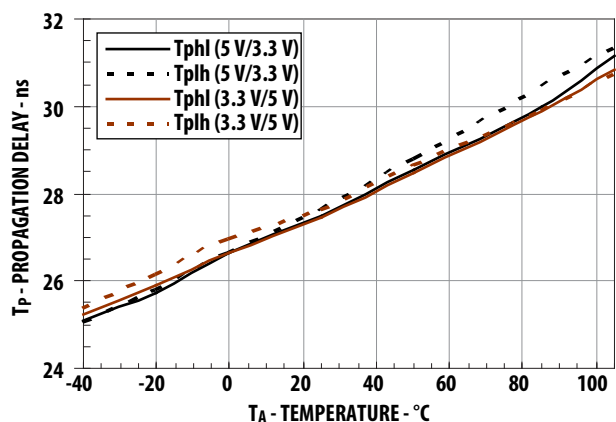


Figure 11: Typical Pulse Width Distortion vs. Temperature

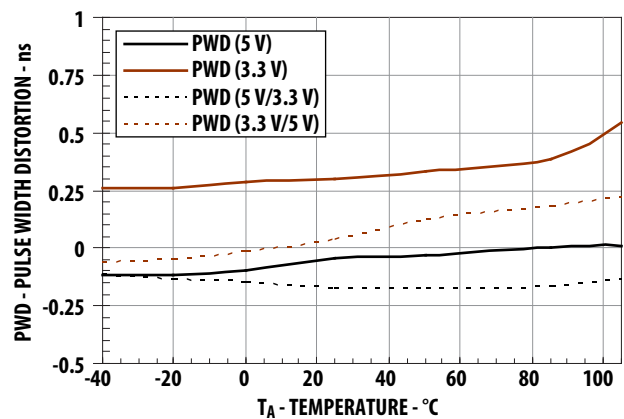
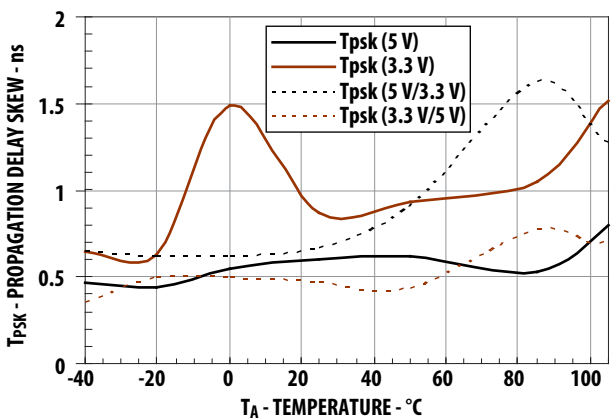


Figure 12: Typical Channel-Channel Delay Skew vs. Temperature



## Supply Current Consumption

It should be noted that the output supply current is specified under no load conditions. Additional supply current consumption from board or components loading can be computed based on:

$$I_{DD} = CVF$$

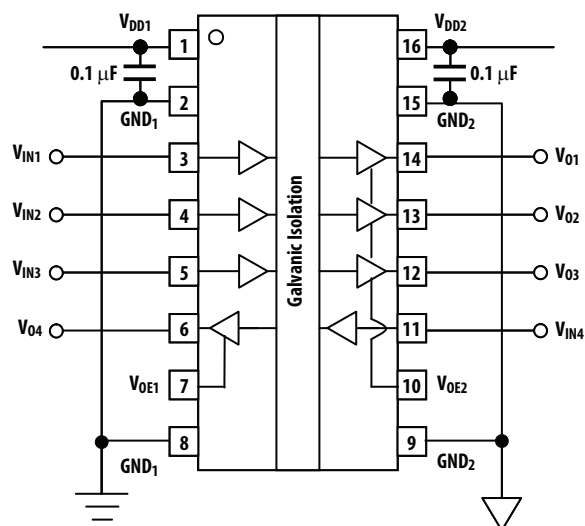
Where  $I_{DD}$  is the additional supply current consumption per output channel,  $C$  is the load capacitance,  $V$  is the supply voltage and  $F$  is the frequency of the signal

## Bypassing and PC Board Layout

The ACML-7400 series digital isolators are extremely easy to use. No external interface circuitry is required because ACML-7400 series use high speed CMOS IC technology allowing CMOS logic to be connected directly to the inputs and outputs.

As shown in [Figure 13](#), the only external components required for proper operation are two bypass capacitors for decoupling the power supply. Capacitor values should typically be 0.1  $\mu$ F. For each capacitor, the total lead length between both ends of the capacitor and the power supply pins should be as short as possible.

Figure 13: Typical Schematic of ACML-7410 on PC Board



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