1. DESCRIPTION

XD4059 standard“A"-Series types are divide-by-N down-counters that can be pro.grammed to divide an input frequency by any number "N" from 3 to 15,999. The out-put signal is a .pulse one clock-cycle wide occurring at a rate equal to the input frequency divided by N. This single output hasTTL drive capability. The down-counter is preset by means of 16 jam inputs.

The three Mode-Select Inputs Ka, Kb, and Kc determine the modulus('divide-by"number) of the first and last counting .sec.tions in accordance with the truth table shown in Table I. Every time the first (fastest)counting section goes through one cycle, it reduces by 1 the number that has been preset (jammed) into the three decades of the intermediate counting section and into the last counting section, which consists of flip-flops that are not needed for operatingthe first counting section. For example, in the ÷ 2 mode, only one flip-flop is needed in the first counting section. Therefore the last counting section has three flip-flops that can be preset to a maximum count of seven with a place value of thousands. If ÷10 is desired for the first section, Ka is set to 1, Kb to 1, and Kc to 0. Jam Inputs J1,J2,J3,and J4 are used to preset the first counting section and there is no last counting section. The intermediate counting section consists of three cascaded BCD de- cade (÷.10) counters presettable by means of Jam Inputs J5 through J16.

The Mode-Select Inputs permit frequency.synthesizer channel separations of 10,12.5,20,25, or 50 parts. These inputs set themaximum value of N at 9999 (when thefirst counting section divides by 5 or 10) or15,999 (when the first counting sectiondivides by 8,4, or 2).

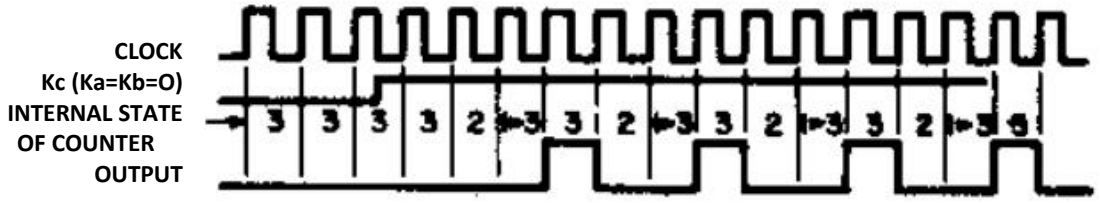
The three decades of the intermediate count.ing section can be preset to a binary 15 in-stead of a binary 9, while their place valuesare still 1,10, and 100, multiplied by thenumber of the ÷ N mode. For example, inthe÷8 mode, the number from which count-ing-down begins can be preset to:

3rd decade:1500，2nd decade:150，1st decade:15，Last counting section 1000

The total of these numbers (2665) times8 equals 21,320.The first counting sectioncan be preset to 7. Therefore, 21,327 is themaximum possible count in the ÷8 mode.The highest count of the various modes isshown in the column entitled Extended Counter Range of Table 1. Control inputsKb and Kc can be used to initiate and lockthe counter in the "master preset" state.In this condition the flip-flops in the counterare preset in accordance with the jam in-puts and the counter remains in that stateas long as Kb and Kc both remain low. Thecounter begins to count down from thepreset state when a counting mode otherthan the master preset mode is selected.

The counter should always be put in themaster preset mode before the ÷5 mode isselected.Whenever the master preset mode is used,control signals Kb=0 and Kc=0 must beapplied for at least 3 full clock pulses.

After the Master Preset Mode inputs havebeen changed to one of the ÷ modes, thenext positive-going clock transition changesan internal ftip-flop so that the countdowncan begin at the second positive-going clocktransition. Thus, after an MP (Master Preset)mode, there is always one extra count beforethe output goes high. Fig.1 illustrates a total count of 3.(÷ 8 mode). If the MasterPreset mode is started two clockcycles orless before an output pulse, the output pulsewill appear at the time due. If the MasterPreset Mode is not used the counter jumpsback to the "JAM" count when the outputpulse appears.



A"1" on the Latch Enable input will causethe counter output to remain high once anoutput pulse occurs, and to remain in thehigh state until the latch input returns to"0". If the Latch Enable is "0", the outputpulse will remain high for only .1 cycle of the clock-input signal.

As illustrated in the sample applications, thisdevice is particularly advantageous in com.munication digital frequency synthesis (VHF,UHF， FM, AM,etc.)where programmabledivide-by-"N" counters are an integral partof the synthesizer phase-locked-loop sub-system. The XD4059 can also be used toperform the synthesizer "Fixed Divide-by-R"counting function. It is also useful in general-purpose counters for instrumentation func-tions such as totalizers, production counters,and "time out" timers.

2. FEATURES

- ynchronous Programmable ÷N Counter:N=3 to 9999 or 15,999
- Presettable down-counter
- Fulty static operation
- Mode-select cantrol of initial decade： counting function (÷ 10,8,5,4,2)
- T^2L drive capability
- Master preset initialization
- Latchable ÷N output
- Quiescent current specified to 15 volts
- Max. input leakage current of 1 μA at 15 volts,full package-temperature range
- 1 volt noise margin, full package.temperature range
- 5-V and 10-V parametric ratings

3. APPLICATIONS

- Communications digital frequency,synthesizers: VHF, UHF, FM, AM,etc.
- Fixed or programmable frequency division
- "Time out" timer for consumer-appli-cation industrial controls

4. MAXIMUM RATINGS, Absolute-Maximum Values:

- DC SUPPLY-VOLTAGE RANGE,(V_{DD})

  Voltages referenced to Vss Terminal) .....-0.5V to +15V

  INPUT VOLTAGE RANGE, ALL INPUTS.....-0.5V to V_{DD}+0.5V

- DEVICE DISSIPATION PER OUTPUT TRANSISTOR

  FORKAGE-TEMPERATURE RANGE.....100mW

- OPERATING-TEMPERATURE RANGE (TA).....-0°C to +70°C
- STORAGE TEMPERATURE RANGE (Tstg).....-65°C to +150°C

5. STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits					Units
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-0°	+70°	+25° Min	+25° Typ	+25° Max	
Quiescent Device Current,IL Max.			5	10	700	—	0.02	10	μA
			10	20	200	—	0.02	20	
			15	—	—	—	—	500	
Output Voltage: Low Level,VOL Max.		0,5	5	0.05		—	0	0.05	V
		0,10	10	0.05		—	0	0.05	
High Level, VOH Min.		0,5	5	4.95		4.95	5	—	
		0,10	10	9.95		9.95	10	—	
Noise Immunity: Inputs Low,VNL Min.			5	1.5		1.5	2.25	—	V
			10	3		3	4.5	—	
Inputs High, VNH Min.			5	1.5		1	2.25	—	
			10	3		3	4.5	—	
Noise Margin:, Inputs Low,VNML Min..	4.5		5	1					V
	9		10	1					
Inputs High, VNMH Min.	0.5		5	1					
	1		10	1					
Output DriveCurrent: N-Channel(Sink) I_DN Min.	0.4		5	2.3	1.6	2	4	—	mA
	0.5		10	4.7	3.3	4	9	—	
P-Channel (Source) I_DP Min.	2.5		5	-1.8	-1.3	-1.6	-3.2	—	
	4.6		5	-0.45	-0.36	-0.4	-0.8	—	
	9.5		10	-1	-0.75	-0.9	-1.8	—	
Input Leakage Current:(1) I_{IL},I_{IH} Max.			15	±1			$\pm 10^{-5}$	±1	μA

Note 1:Any Input

DYNAMIC ELECTRICAL CHARACTERISTICS AT T_A =25°C,C_L=50 pF, Input t_r,t_f=20 ns,R_L=200kΩ

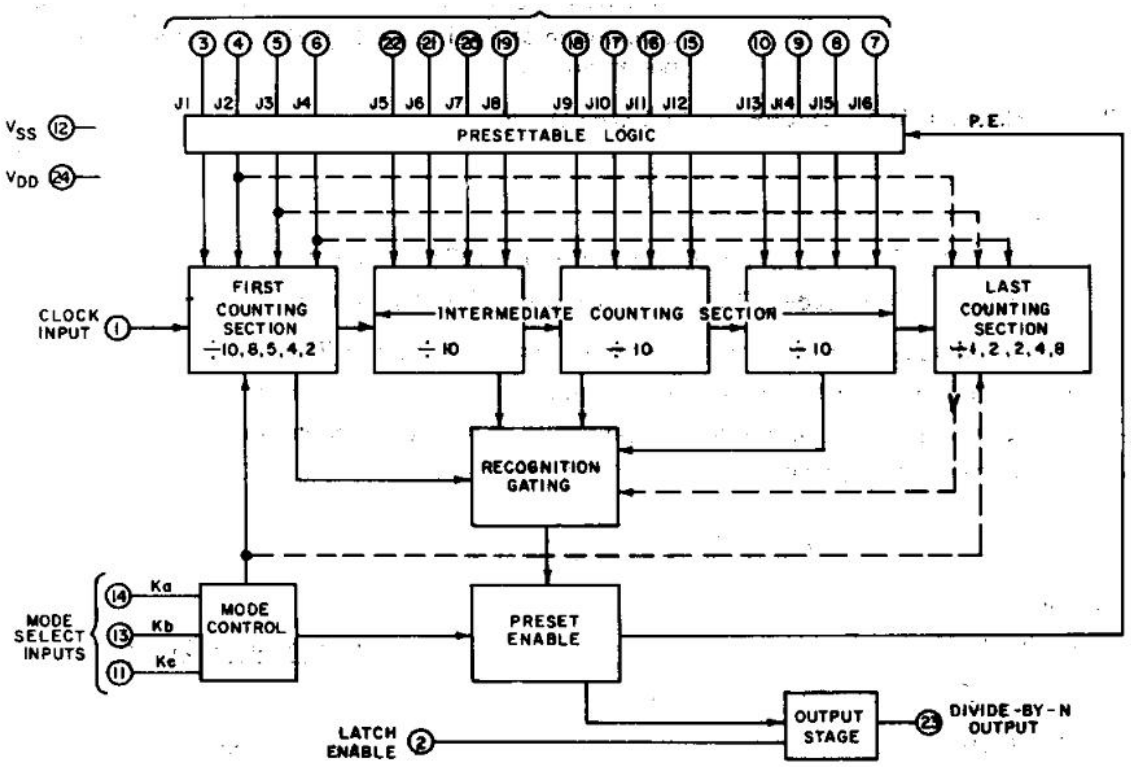
CHARACTERISTIC		CONDITIONS VDD(V)	LIMITS ALL PACKAGES Min	Typ	Max	UNITS
Propagation Delay Time; t_{PHL},t_{PLH}		5	—	180	360	ns
		10	—	90	180	
Transition Time	t_{THL}	5	—	35	70	ns
		10	—	20	40	
	t_{TLH}	5	—	100	200	
		10	—	50	100	
Maximum Clock Input Frequency, f_{CL}		5	1.5	3	—	MHZ
		10	3	6	—	
Average Input Capacitance, CI (any input)		—	—	5	—	pF

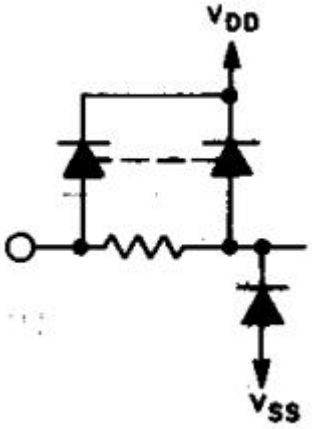
6. OPERATING CONDITIONS AT TA =25°C(Unless otherwise specified)

For maximum reliability, nominal operating condi-tions should be selected so that operation is alwayswithin the following ranges.

Characteristic	VDD	MIN	MAX	UNITS
Supply VoltageRange (over full temp.range)	—	3	12	V
Clock Pulse Width	5 10	200 100	— —	ns
Clock Input 'Frequency	5 10	— —	1.5 3	MHZ
Clock Input Rise and Fall Time	5 10	— —	15 5	μs

PROGRAM JAM INPUTS (BCD)





ALL INPUTS PROTECTED
BY CMOS PROTECTION NETWORK

Fig.1 - Functional block diagram.

MODESELECT INPUT			FIRST COUNTING SECTION			LAST COUNTING SECTION			COUNTERRANGE	
									DESIGN	EXTENDED
Ka	Kb	Kc	MODE Divides by:	Can be Preset to a max of:	Jam(1) inputs used:	MODE Divides by:	Can be Preset to a max of:	Jam(1) inputs used	Max	Max
1	1	1	2	1	J1	8	7	J2,J3,J4	15,999	17,331
0	1	1	4	3	J1,J2	4	3	J3,J4	15,999	18,663
1	0	1	5(3)	4	J1,J2,J3	2	1	J4	9,999	13,329
0	0	1	8	7	J1,J2,J3	2	1	J4	15,999	21,327
1	1	0	10	9	J1,J2,J3,J4	1	0	—	9,999	16,659
X	0	0	MASTER PRESET			MASTER PRESET			—	—

X = Don't Care

(1)J1 = Least significant bit. J4 = Most significant bit.

(2)Operation in the +5mode (1st counting section) requiresgoing through the Master Preset mode prior to going into the ÷5 mode. At power turn-on, kc must be a logic "0" for a period of 3 input clock pulses after VDD reaches a minimum of 3 volts.

7. HOW TO PRESET THE XD4059 TO DESIRED÷N

The value N is determined as follows:

N =[MODE*} [1000 x Decade 5 Preset+100X Decade 4 Preset+10X Decade 3Preset+1X Decade 2 Preset } + Decade 1Preset (1)

*MODE= First counting section divider (10, 8, 5, 4 or 2)

To calculate preset values for any N count, divide the N count by the Mode.

The resultant is the corresponding preset values of the 5th through 2nd decade with the remainder being equal to the 1st decade value.

$$\text{Preset Value} = \frac{N}{\text{Mode}} \quad (2)$$

Examples:

A) N = 8479, Mode = 5

1695 + 4 ← Preset Values

5 ⌈ 8479

Mode, N

MODE SELECT = 5

Ka	Kb	Kc
1	0	1

PROGRAM JAM INPUTS (BCD)

4			1	5				9				6			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
0	0	1	1	1	0	1	0	1	0	0	1	0	1	1	0

To verify the results use equation 1 :

N = 5 (1000X 1 + 100 X 6 + 10 X 9 + 1 X 5) + 4

N = 8479

MODE SELECT = 8

B) N = 12382, Mode = 8

1547 + 6

8 ⌈ 12382

Ka	Kb	Kc
0	0	1

PROGRAM JAM INPUTS

6			1	7				4				5			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
0	1	1	1	1	1	1	0	0	0	1	0	1	0	1	0

To verify:

N = 8 (1000 X 1 + 100 X 5 + 10 X 4 + 1 X 7) + 6

N = 12382

MODE SELECT = 10

C) N = 8479, Mode = 10

$$10 \overline{)\,8479}\quad 0847 + 9$$

Ka	Kb	Kc
1	1	0

PROGRAM JAM INPUTS

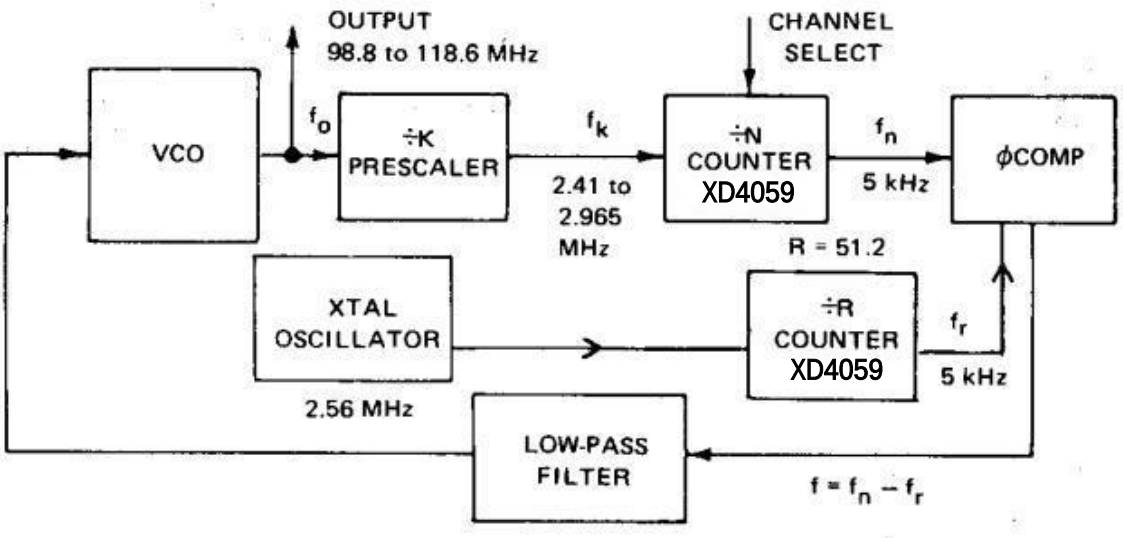
9				7				4				8			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
1	0	0	1	1	1	1	0	0	0	1	0	0	0	0	1

To Verify:

N = 10 (1000 X 0 + 100 X 8 + 10 X 4 + 1 X 7) + 9

N = 8479

8. DIGITAL PHASE-LOCKED LOOP (PLL) FOR FM BAND SYNTHESIZER



8.1.Calculating Min & Max "N" Values :

Output Freq. Range (1o) = 98.8 to 118.6 MHz

Channel Spacing Freq. (fc) = 200 kHz

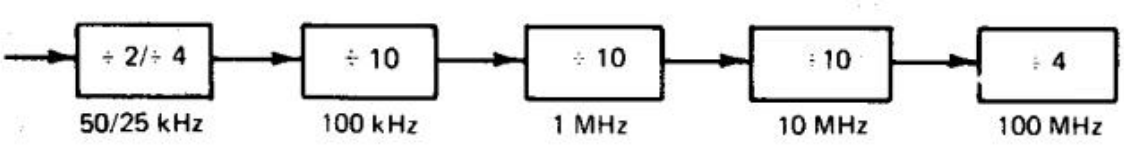
Division Factor (k)=40 Reference Freq. (fr) = $\frac{fc}{K} = \frac{200}{40}$ kHz = 5 kHz

fk = $\frac{fo}{40}$: fkMax = $\frac{118.6MHz}{40}$ =2.965MHz; fkMin = $\frac{98.8MHz}{40}$ = 2.47MHz N = $\frac{fo}{fc}$

$N_{Max} = \frac{118.6MHz}{200kHz}$ = 593 $N_{Min} = \frac{98.8MHz}{200kHz}$ = 494 R = $\frac{2.56MHz}{5kHz}$ = 512

8.2.÷N Counter Configuration for UHF - 220 to 400 MHz

Channel Spacing : 50kHz or 25kHZ



$N_{Max} = \frac{400MHz}{25kHz}$ = 16000 $N_{Max} = \frac{400MHz}{50kHz}$ = 8000

$N_{Min} = \frac{220MHz}{25kHz}$ = 8800 $N_{Min} = \frac{220MHz}{50kHz}$ = 4400

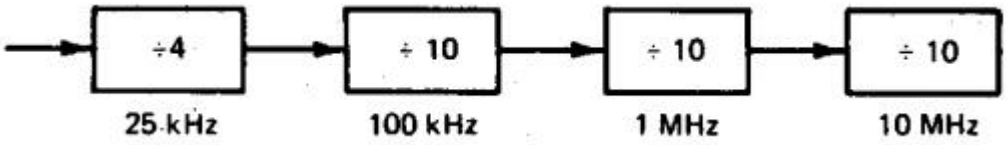
8.3.÷N Counter Configuration to VHF-116 MHz

Channel Spacing = 12.5 kHz

$N_{Max} = \frac{160MHz}{12.5kHz}$ = 12800 $N_{Min} = \frac{116MHz}{12.5kHz}$ = 9300

8.4.÷N Counter Configuration for VHF - 30 to 80 MHz

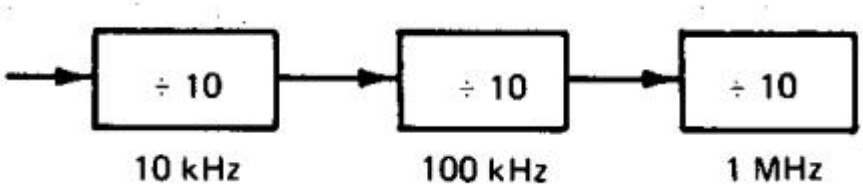
Channel Spacing:25kHz



$N_{Max} = \frac{80MHz}{25kHz} = 3200$ $N_{Min} = \frac{30MHz}{25kHz} = 1200$

8.5.÷N Counter Configuration for AM-995 to 2055 kHz

Channei Spacing =10 kHz



$N_{Max} = \frac{2055MHz}{10kHz} = 205$ $N_{Min} = \frac{995MHz}{10kHz} = 99$

9. "CASCADING" VIA OTHER COUNTERS

Fig. 2 shows a BCD-switch compatible ar-rangement suitable for ÷ 8 and ÷5 modes,which can be adapted, with slight changes,to the other divide-by-modes. In order to beable to preset to any number from three toabout 256,000,while preserving the BCD.switch compatible character of the jam inputs, a rather complex cascading scheme is required. Such a cascading scheme is neces.sary because the XD4059 can never be pre-set to a count less than 3 and logic is needed to detect the condition that one of the num.bers to be preset in the XD4059 is rather small. In order to simplify the detectionlogic, only that condition is detected wherethe jam inputs to terminals 6, 7, and 9 wouldbe low during one count. If such a conditionis detected, and if at least 1 is expected to be jammed into the MSB counter,the detectiontogic removes one from the number to be jammed into the MSB counter (with a place value of 2000 times the divide-by-mode) andjams the same 2000 into the XD4059 by forcing terminals 6, 7, and 9 high.

The general circuit in Fig.2 can be simplified considerably if the range of the cas. caded counters does not have to start at a very low value. Fig.3 shows an arrange. ment in the ÷ 4 mode, where the counting range extends in a BCD-switch compatible manner from 88,003 to 103,999. The arrangement shown in Fig.3 is easy to follow ;once during each cycle, the less significant digits are jammed in (14,712 in this case) and then 11,000 (4 x 2750) is jammed in eight times in succession, by forcing jam in- puts high or low, as required.

Numbers larger than the extended counterrange can also be produced by cascading the XD4059 with some other counting device. Fig.4 shows such an arrangement where only one fixed divide-by number is desired which is close to three times the extended counter range as shown in the last column of Table I.. .In Fig.4 the ÷N subsystem is preset once to a number smaller than the desired divide-by number. This smaller number represents the less significant digits of the divide-by number. The subsystem is then preset one or more times to a round number (e.g.1000,2000) and multiplied by the number of the divide-by mode (÷ 2 in the example of Fig.4). It is important that the second counting device has an output that is high or low, as the case may be, during only one of its counting states.

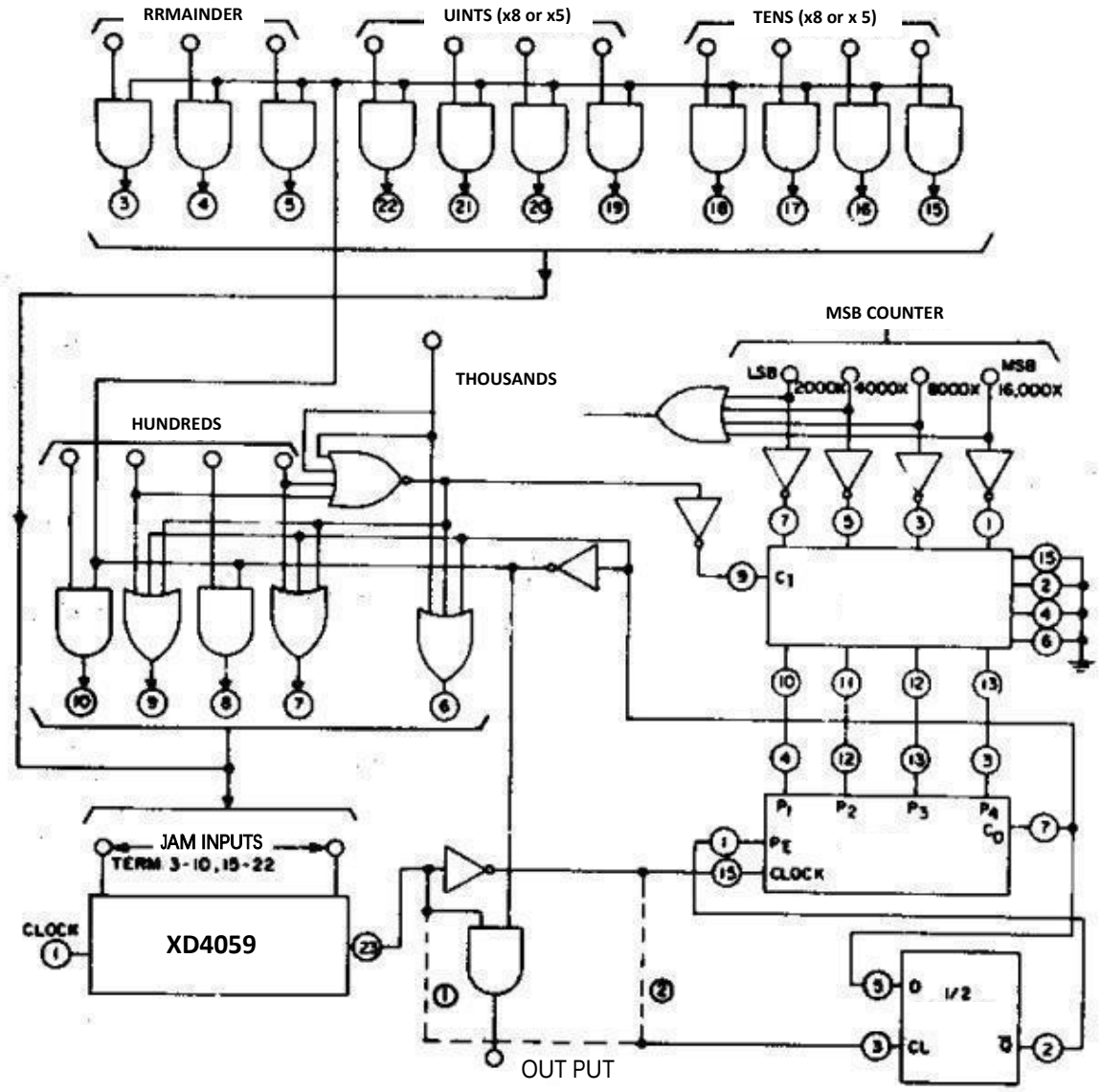


Fig.2 -BCD switch-compatible ÷N system of the most general kind.

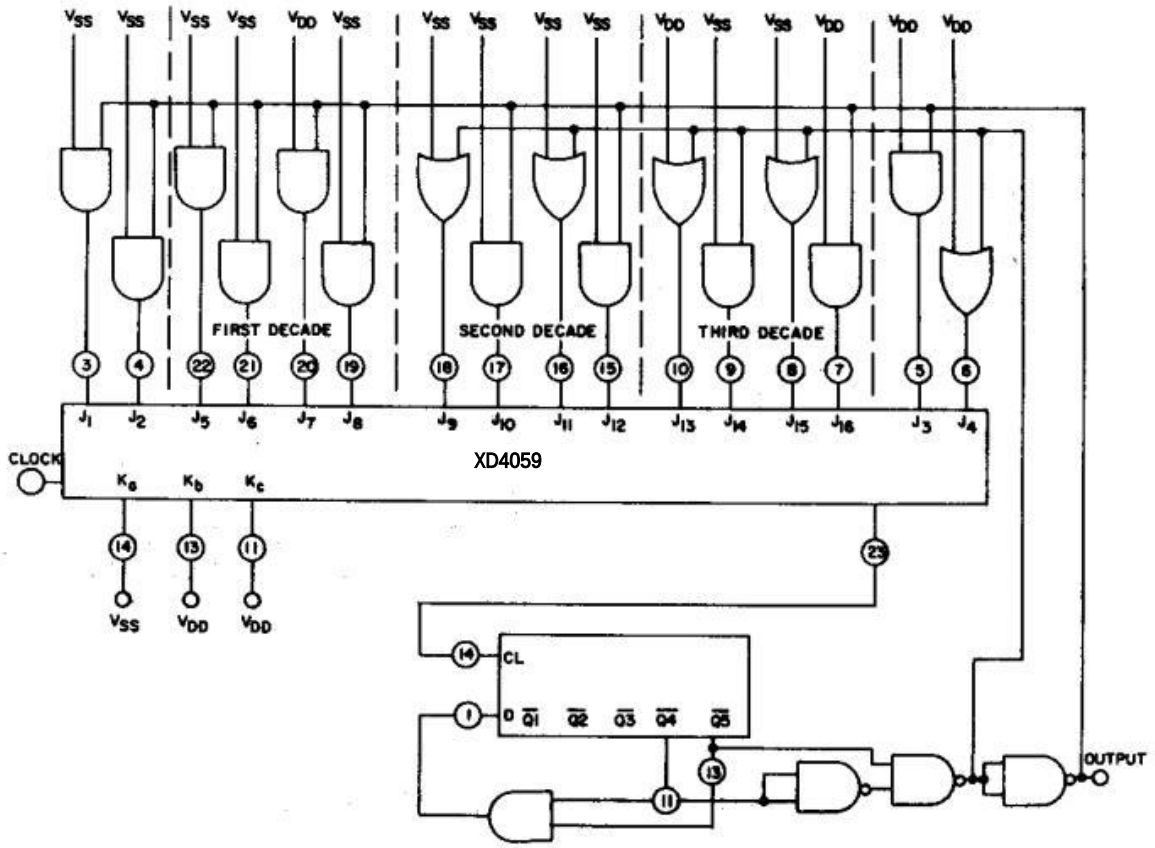


Fig.3 - Division by 47,690 in ÷2 mode.

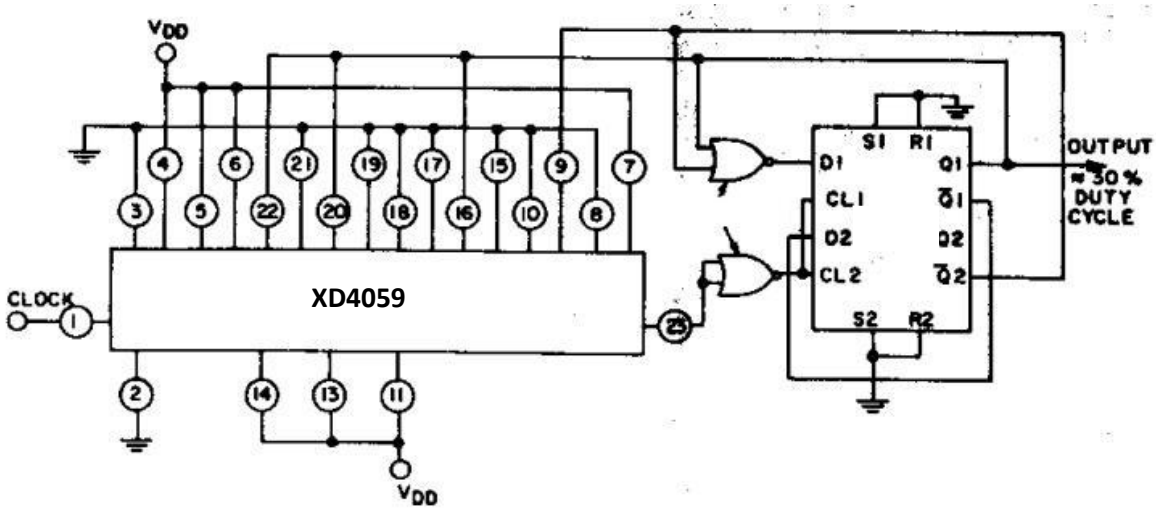


Fig.4 - Division by 47,690 in ÷2 mode.

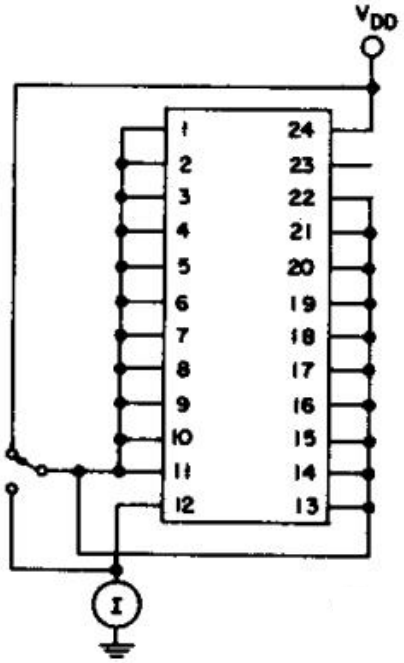


Fig.5 - Quiescent device current test circuit.

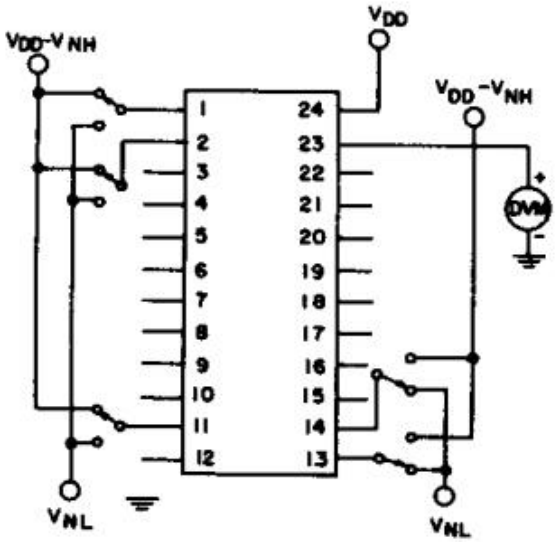


Fig.6 - Noise immunity test circuit.

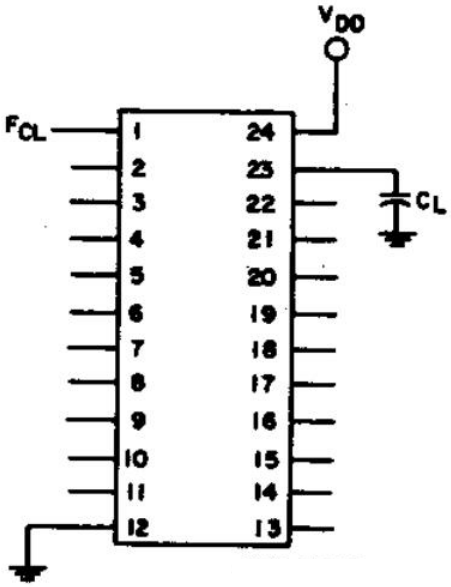
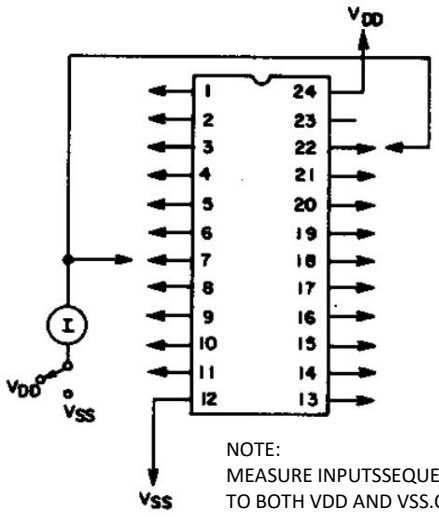


Fig.7 -- Power dissipation test circuit (oil ÷modes).



NOTE:
MEASURE INPUTSSEQUENTIALLY, TO BOTH VDD AND VSS.CONNECT ALL UNUSED INPUTS TO EITHER VDO OR VSS.

Fig.8 - Input leakage current test circuit.

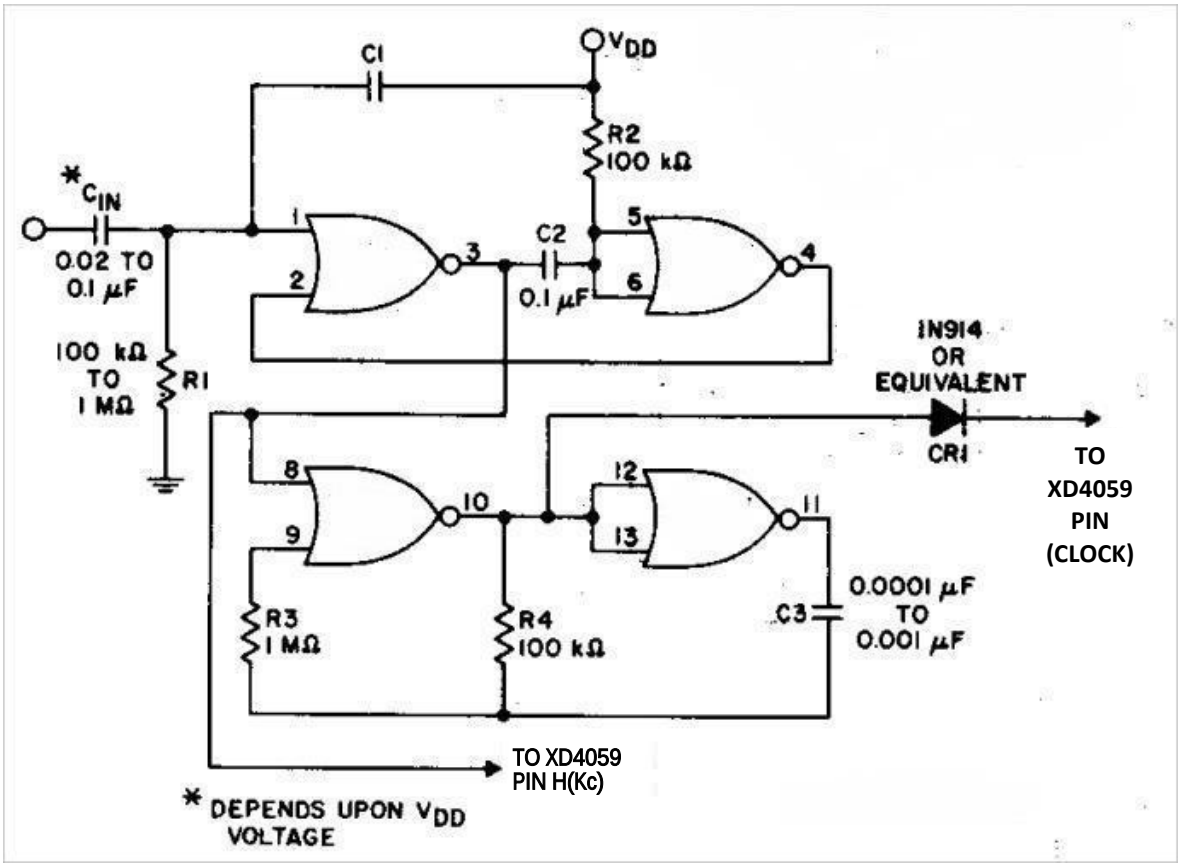


Fig.9 -XD4059 mode 5 power on maste'r preset

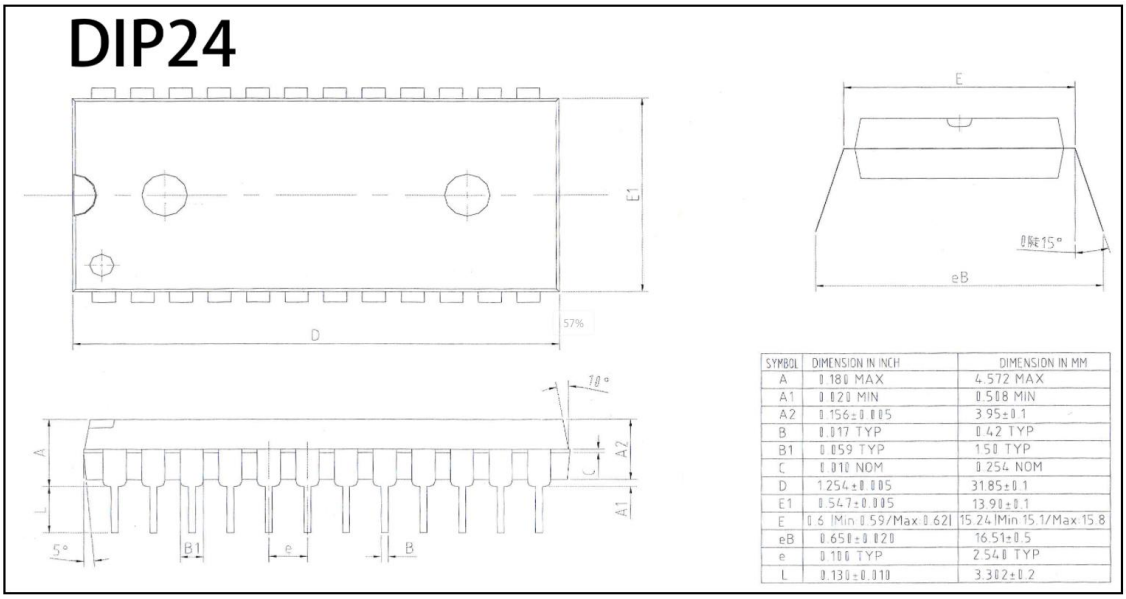
For changing.from any mode other than mode 5(with power on), apply positive pulse to Cin. Thiscircuit automatically seiects master preset mode(K_b = 0, K。 = 0) before going into the select conditions for mode 5 (K= 1, k。 = 0, K = 1).The selection of C1and Cz is critica!C, is determinedby the VDD voltage--the lowerVDD's need larger C,'s. C_2 must be 0.1 μF or larger.

10. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XD4059	XD4059	DIP24	31.85*13.90	-0 to +70	MSL3	Tube 15	300

11. DIMENSIONAL DRAWINGS



SYMBOL	DIMENSION IN INCH	DIMENSION IN MM
A	0.180 MAX	4.572 MAX
A1	0.020 MIN	0.508 MIN
A2	0.156±0.005	3.95±0.1
B	0.017 TYP	0.42 TYP
B1	0.059 TYP	1.50 TYP
C	0.010 NOM	0.254 NOM
D	1.254±0.005	31.85±0.1
E1	0.547±0.005	13.90±0.1
E	0.6 [Min 0.59/Max 0.62]	15.24 [Min 15.1/Max 15.8
eB	0.650±0.020	16.51±0.5
e	0.100 TYP	2.540 TYP
L	0.130±0.010	3.302±0.2