MP4088

Non-Isolated, High PFC, TRIAC Dimmable LED Driver for 230VAC, Up to 10W LEDs

The Future of Analog IC Technology

DESCRIPTION

The MP4088 is a highly integrated, TRIAC dimmable LED driver with an integrated 500V MOSFET that regulates precise LED currents in non-isolated lighting applications and requires only a single winding inductor. The MP4088 features MPS' proprietary hybrid operation mode, which is designed to achieve optimal dimming performance. The MP4088 is designed specifically for high-line input (230VAC) and TRIAC dimmable LED lighting applications, especially for low-cost and small form-factor applications.

The accurate output LED current is achieved by an internal averaging current feedback loop. An internal high-voltage regulator makes the MP4088 start up quickly without a perceptible delay. The power de-rating at high temperatures makes the system flicker-free when the ambient temperature is high.

Full protections features include VCC under-voltage lockout (UVLO), over-voltage protection (OVP), and short-circuit protection (SCP). All of these features make the MP4088 an ideal solution for simple, offline, and non-isolated TRIAC dimmable LED lighting applications.

The MP4088 is available in TSOT23-5, SOIC8-7A, and SOIC-8 EP packages.

FEATURES

- Excellent TRIAC Dimming Performance
- Lowest BOM Cost
- Constant Current LED Driver
- Integrated 500V MOSFET
- Internal HV Fast Start-Up
- Single Winding Inductor
- High Power Factor (>0.7)
- Good LED Current Accuracy
- Supports Buck and Buck-Boost Topology
- LED Current Foldback at High Temperature
- Thermal Shutdown (Auto-Restart with Hysteresis)
- VCC Under-Voltage Lockout with Hysteresis (UVLO)
- Programmable Over-Voltage Protection (OVP)
- Output Short-Circuit Protection (SCP)
- Auto-Restart Function
- Available in TSOT23-5, SOIC8-7A, and SOIC-8 EP Packages

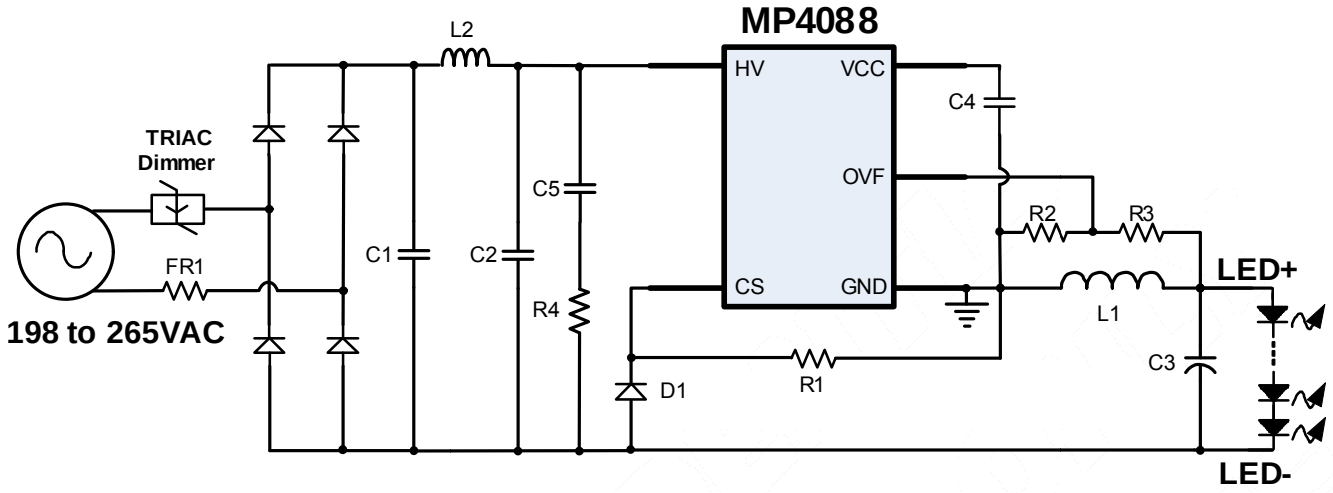
APPLICATIONS

- 230VAC, Up to 10W LED Lighting
- Residential and Commercial Lighting
- TRIAC Dimmable LED Lighting, A19, GU10, PAR Lamps

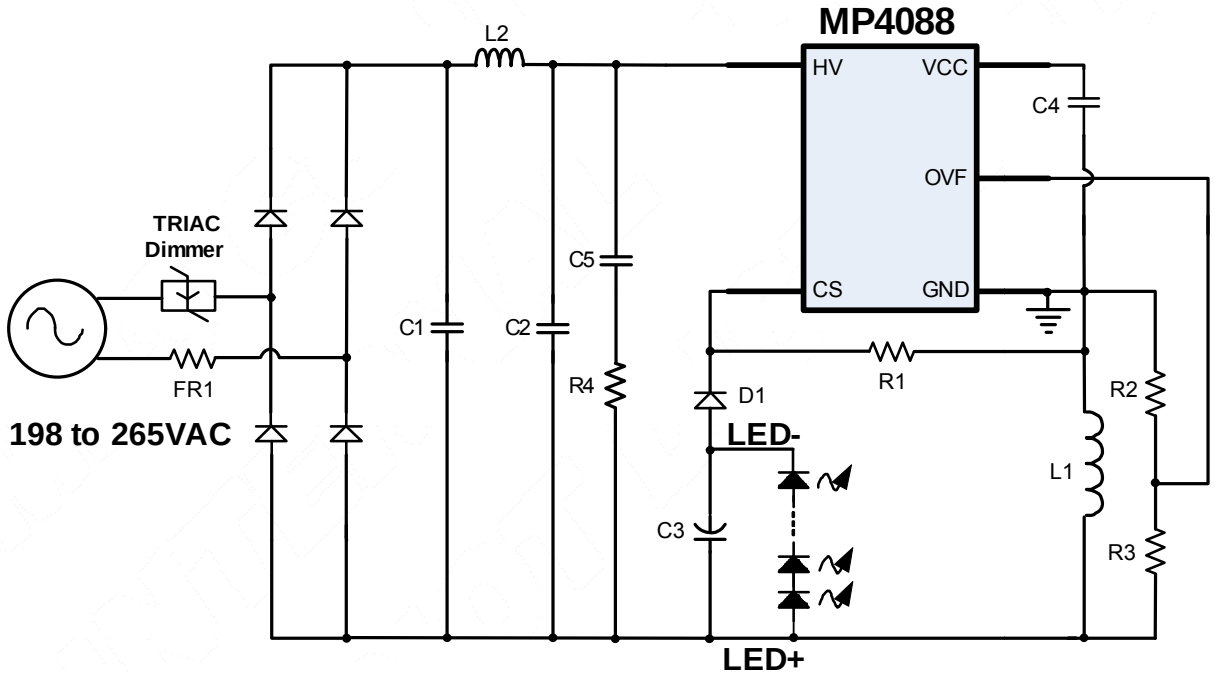
All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

TYPICAL APPLICATION (BUCK)



TYPICAL APPLICATION (BUCK-BOOST)



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number	Package	Top Marking
MP4088GJ*	TSOT23-5	*See Below*
MP4088GS**	SOIC8-7A	*See Below*
MP4088GN***	SOIC-8 EP	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP4088GN–Z)
** For Tape & Reel, add suffix –Z (e.g. MP4088GS–Z)
*** For Tape & Reel, add suffix –Z (e.g. MP4088GN–Z)

TOP MARKING (MP4088GJ)

|ARNY

ARN: Product code of MP4088GJ
Y: Year code

TOP MARKING (MP4088GS)

MP4088
LLLLLLLL
MPSYWW

MP4088: Product code of MP4088GS
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

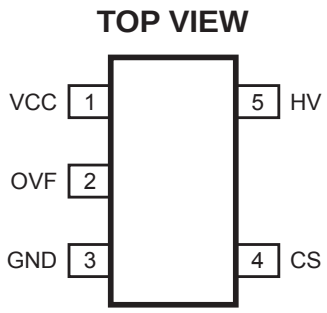
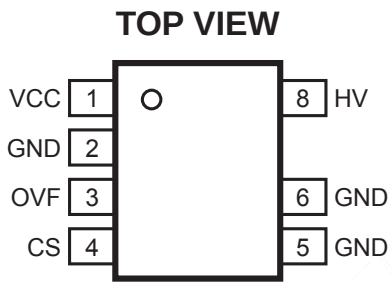
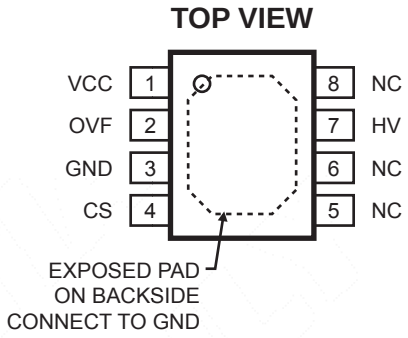
TOP MARKING (MP4088GN)

MP4088
LLLLLLLL
MPSYWW

MP4088: Product code of MP4088GN
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

PACKAGE REFERENCE

TSOT23-5	SOIC8-7A	SOIC-8 EP
		

ABSOLUTE MAXIMUM RATINGS (1)

HV to CS..... -0.3V to 500V
VCC, CS to GND ..... -0.3V to 6.5V
OVF to GND ..... -0.7V to 6.5V
Source current on OVF 4mA
Continuous power dissipation (T_A = +25°C) (2)
TSOT23-5.....1.25W
SOIC8-7A …….....1.6W
SOIC-8 EP.....2.6W
Lead temperature .....260°C
Storage temperature.....-60°C to +150°C
ESD capability human body mode 2.0kV
CDM ESD capability
TSOT23-5.....1.5kV
SOIC8-7A/SOIC-8 EP..... 2kV

Recommended Operating Conditions (3)

Operating VCC range ..... 4.5V to 5V

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
TSOT23-5	100	55	°C/W
SOIC8-7A	76	35	°C/W
SOIC-8 EP	48	10	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

Typical values are VCC = 5V, T_J = 25°C, unless otherwise noted.

Minimum and maximum values are VCC = 5V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Start-Up Current Source (HV)						
Internal regulator supply current	$I_{REGULATOR}$	VCC = 0V, V_{HV} = 100V	3.8	5	6.1	mA
Leakage current from HV	$I_{HV\ LKG}$	VCC = 5V, V_{HV} = 400V		14	22	µA
Supply Voltage Management (VCC)						
VCC upper threshold for internal regulator turn-off	VCC_{OFF}	VCC rising edge	4	4.35	4.7	V
VCC normal level	VCC_{NOR}	Normal operation		4.25		V
VCC lower threshold for internal regulator turn-on	VCC_{ON}	VCC falling edge	3.8	4.1	4.45	V
VCC hysteresis between regulator on/off	VCC_{OFF-ON}		0.12	0.21	0.3	V
VCC lower threshold for IC shutdown	VCC_{STOP}	VCC falling edge	3.0	3.4	3.8	V
VCC hysteresis between regulator off/IC shutdown	$VCC_{OFF-STOP}$		0.5	0.95	1.4	V
VCC lower threshold where protection phase ends	VCC_{PRO}	VCC falling edge	1.90	2.35	2.80	V
Internal IC consumption	I_{CC}	VCC = 4.3V, fsw = 33kHz, duty = 84%		350	400	µA
Internal IC consumption, latch-off phase	I_{CC_LATCH}	VCC = 5V		18	32	µA
Internal MOSFET (HV to CS)						
Breakdown voltage	V_{BR}	I_{HV} = 80µA	500			V
On-state resistance	$R_{DS(ON)}$	I_{HV} = 10mA, T_J = 25°C		8.5	12	Ω
		VCC = VCC_{STOP} + 50mV, I_{HV} = 10mA, T_J = 25°C		8.5	12	Ω
Current Sampling Management (CS)						
Peak current limit at normal operation	V_{CS_LIMIT}		0.40	0.46	0.52	V
Leading edge blanking	t_{LEB}			200		ns
Feedback threshold to turn on MOSFET	V_{REF}		0.186	0.195	0.204	V
Minimum off-time limitation at normal operation	t_{OFF_MIN}		7.1	9.3	11.8	µs
Maximum on-time limitation	t_{ON_MAX}		3.3	4.5	6	µs
Ratio of t_{ON_MAX}/t_{OFF_MIN}	σ		0.42	0.48	0.58	

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are VCC = 5V, T_J = 25°C, unless otherwise noted.

Minimum and maximum values are at VCC = 5V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Protection Input (OVF)						
Threshold to trigger OVP	V_{OVP}		1.85	2.0	2.15	V
Time constraint on OVP comparator	t_{OVP}			21	32	µs
Thermal Protection						
Power de-rating threshold(5)	T_{START}			145		°C
Thermal shutdown threshold(5)	T_{SD}			160		°C
Thermal shutdown recovery hysteresis(5)	T_{HYS}			50		°C

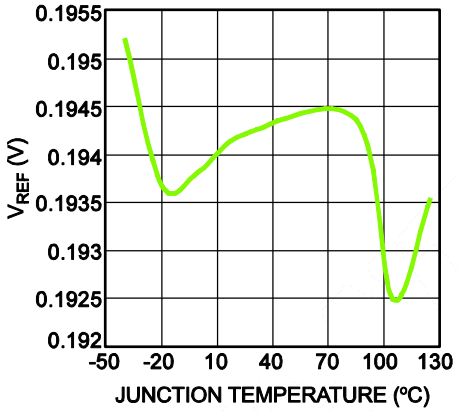
NOTE:

5) Guaranteed by characterization.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS

Reference Voltage vs. Junction Temperature



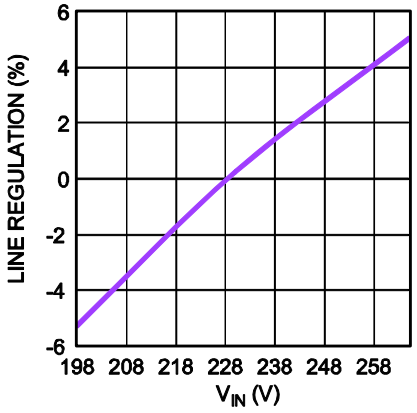
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 230VAC, V_{OUT} = 50V, I_{LED} = 160mA, T_A = 25°C, unless otherwise noted.

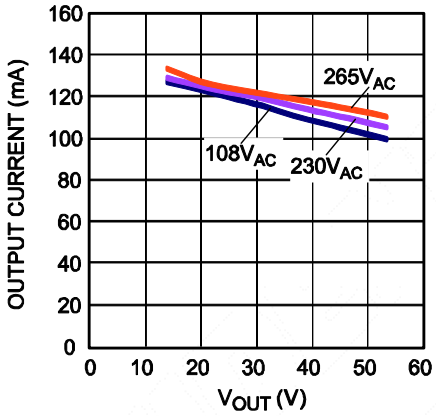
Line Regulation

V_{IN}=(198-265)V_{AC}/50Hz, Full Load



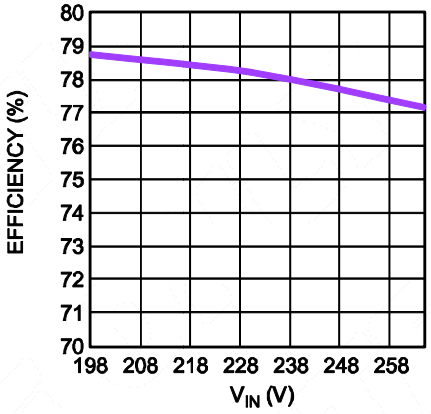
Load Regulation

V_{IN}=(198-265)V_{AC}/50Hz



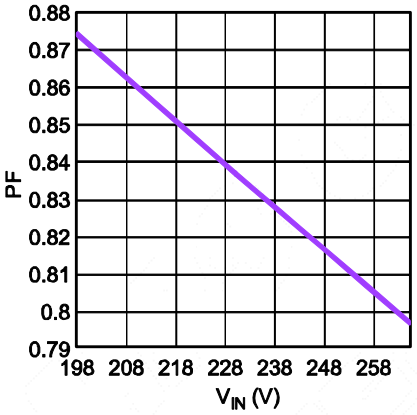
Efficiency

V_{IN}=(198-265)V_{AC}/50Hz, Full Load



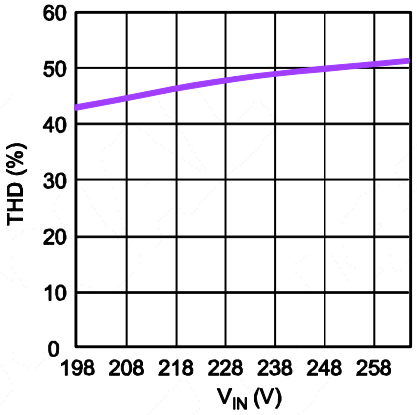
PF vs. V_{IN}

V_{IN}=(198-265)V_{AC}/50Hz, Full Load



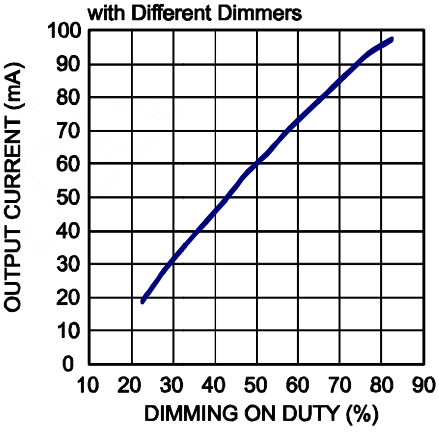
THD vs. V_{IN}

V_{IN}=(198-265)V_{AC}/50Hz, Full Load



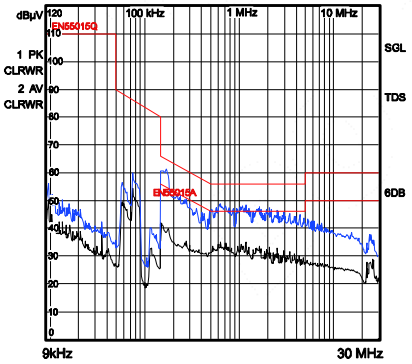
Dimming Curve

V_{IN}=230V_{AC}/50Hz, Full Load,
with Different Dimmers



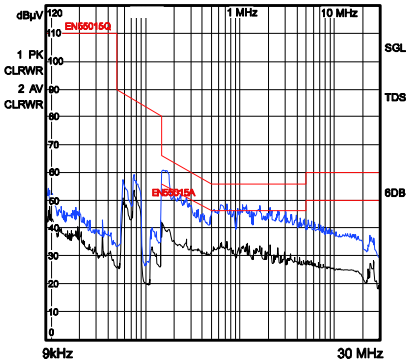
Conducted EMI, L-Line

V_{IN}=230V_{AC}, RBW=9kHz, MT=20ms



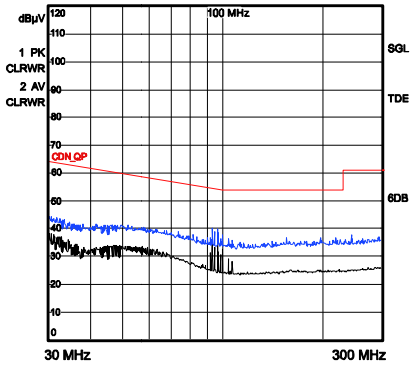
Conducted EMI, N-Line

V_{IN}=230V_{AC}, RBW=9kHz, MT=20ms



CDN Test

V_{IN}=230V_{AC}, RBW=120kHz, MT=1ms

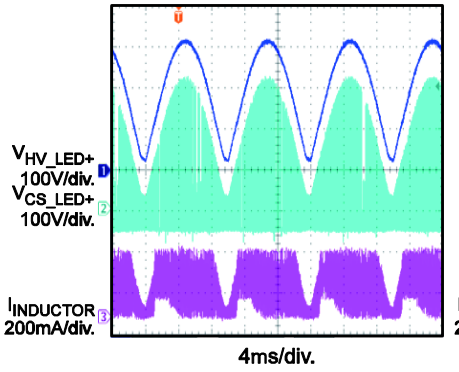


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

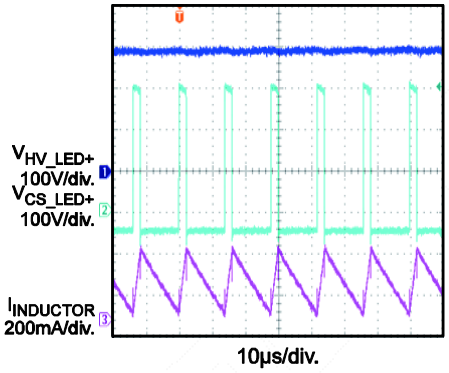
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 230VAC, V_{OUT} = 50V, I_{LED} = 160mA, T_A = 25°C, unless otherwise noted.

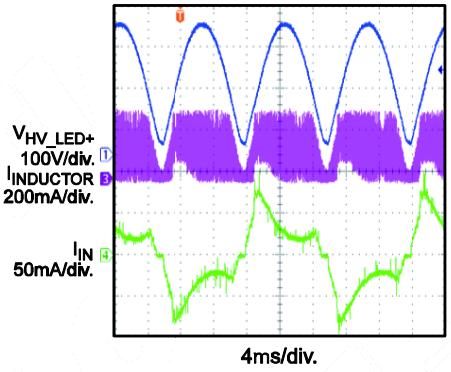
Steady State
V_{IN}=230V_{AC}/50Hz, Full Load



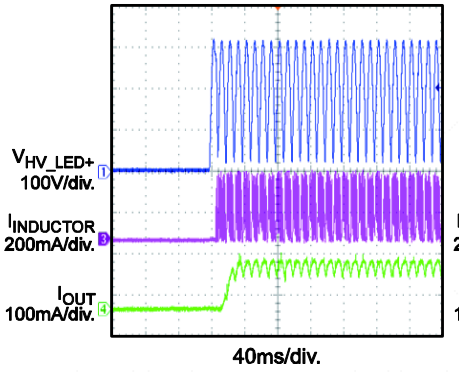
Steady State
V_{IN}=230V_{AC}/50Hz, Full Load



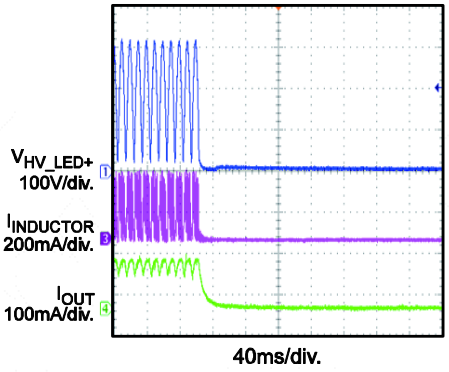
Steady State
V_{IN}=230V_{AC}/50Hz, Full Load



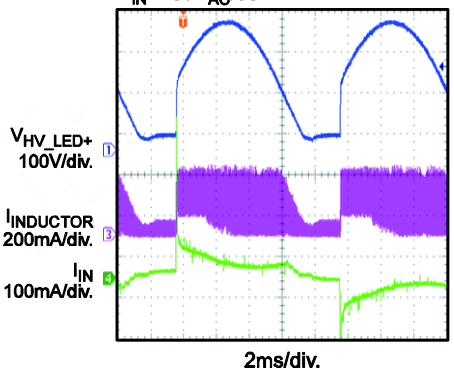
V_{IN} Start-Up
V_{IN}=230V_{AC}/50Hz, Full Load



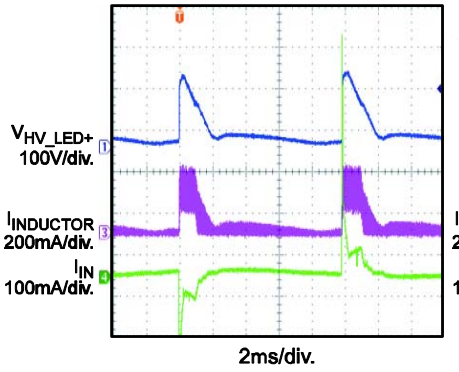
V_{IN} Shutdown
V_{IN}=230V_{AC}/50Hz, Full Load



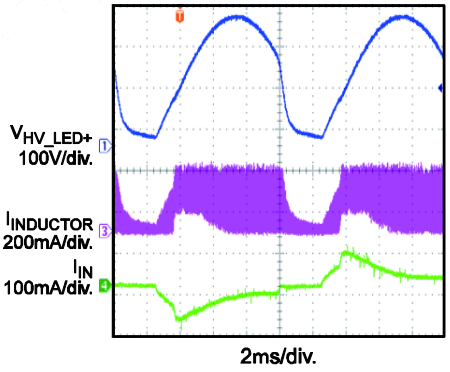
Dimming Performance
Max Dmming On Phase
with Leading-Edge Dimmer
V_{IN}=230V_{AC}/50Hz



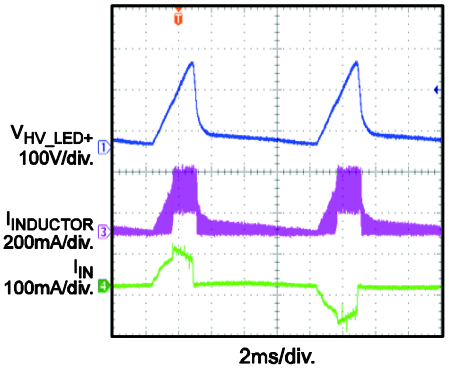
Dimming Performance
Min Dmming On Phase
with Leading-Edge Dimmer
V_{IN}=230V_{AC}/50Hz



Dimming Performance
Max Dmming On Phase
with Trailing-Edge Dimmer
V_{IN}=230V_{AC}/50Hz



Dimming Performance
Min Dmming On Phase
with Trailing-Edge Dimmer
V_{IN}=230V_{AC}/50Hz



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

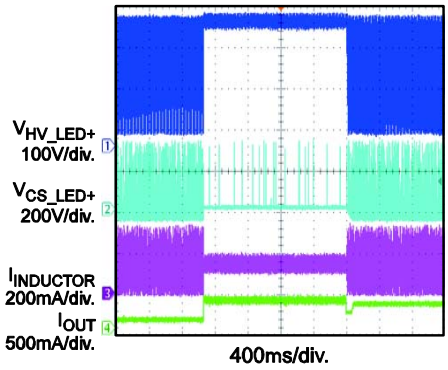
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 230VAC, V_{OUT} = 50V, I_{LED} = 160mA, T_A = 25°C, unless otherwise noted.

SCP

LED+ Short to LED- and then Recovery

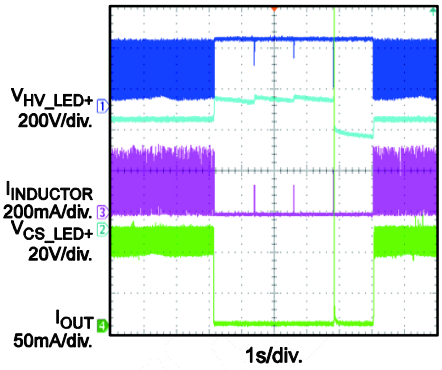
V_{IN}=230V_{AC}/50Hz



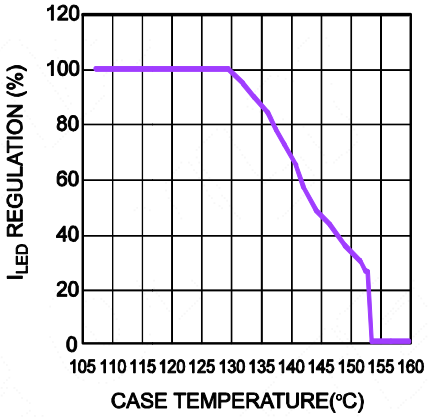
OVP

LED Load Open, then Recovery

V_{IN}=230V_{AC}/50Hz



Output Current Thermal Foldback Curve



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #			Name	Description
TSOT23-5	SOIC8-7A	SOIC-8 EP		
1	1	1	VCC	**Power supply.** VCC is the supply power for all of the control circuits. Connect VCC to an external bulk capacitor.
3	2, 5, 6	3	GND	**Ground.** GND is the virtual ground of the IC.
2	3	2	OVF	**Output voltage feedback.** The over-voltage condition is detected on OVF. When the voltage on OVF exceeds V_{OVP} after a blanking time, OVP is triggered, and the chip shuts down.
4	4	4	CS	**Current sense of the internal power MOSFET.** Connect a resistor from CS to GND to sense the current through the inductor. When the voltage on CS exceeds V_{CS_LIMIT}, the internal MOSFET is turned off. If the start-up time exceeds the maximum on-time, the internal MOSFET is turned off, even though the voltage on CS has not reached $V_{CS\ LIMIT}$.
5	8	7	HV	**High-voltage input of the internal power MOSFET.** HV is also the input of the internal high-voltage current source.
--	--	5, 6, 8	NC	**Not connected.**
			Exposed Pad	**The exposed pad should be connected to the GND plane for optimal thermal performance.**

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

BLOCK DIAGRAM

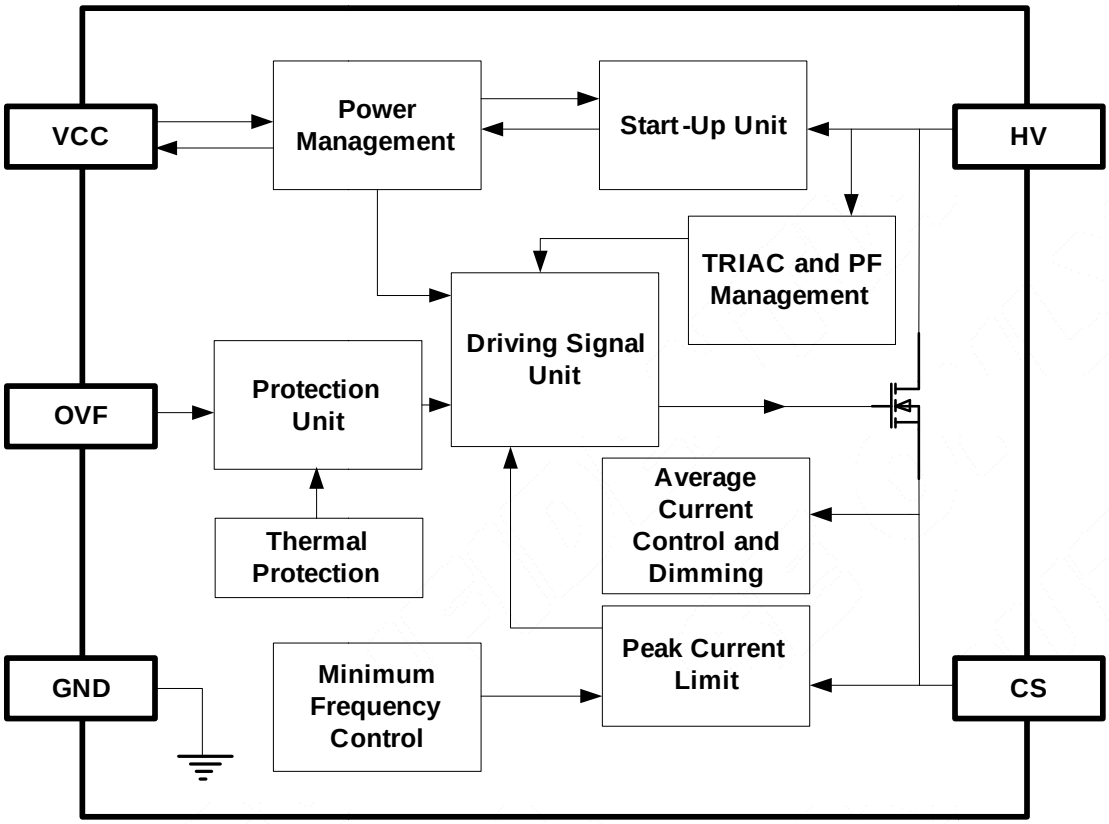


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

OPERATION

The MP4088 is a highly integrated, cost-effective, TRIAC dimmable LED driver. The MP4088 requires only a minimal number of external components, making it a competitive IC in high-line (230VAC) input and non-isolated applications, especially for small form-factor applications. Hybrid operation mode achieves both good dimming performance and accurate output current. The power factor exceeds 0.7 in most applications to eliminate harmonic pollution on the AC line. The integrated high-voltage regulator enables fast start-up without any perceptible delay. The power de-rating function at high temperatures protects the IC from thermal damage.

Hybrid Operation Mode

To achieve smooth TRIAC dimming, the MP4088 implements proprietary hybrid operation mode, in which the IC self-adjusts the internal switching mode between CCM and DCM during different times of the AC cycle. The hybrid operation mode actively maintains the latching current and holding current of the leading edge TRIAC to enable a good power factor.

The hybrid operation mode also achieves a small dimming duty condition. The IC works in CCM during the entire dimming on time when the dimmer is set to a small dimming duty. A higher and smoother input current can achieve excellent dimming performance.

Power Supply

The IC is self-supplied by the internal high-voltage regulator, which is drawn from HV. The IC begins switching, and the internal high-voltage regulator turns off once the voltage on VCC reaches VCC_{OFF}. When the voltage on VCC falls below VCC_{ON}, the internal high-voltage regulator turns on again to charge the external VCC capacitor. VCC is regulated at VCC_{NOR} for normal operation.

In TRIAC dimming applications, the internal high-voltage regulator only works when the dimmer is on. To maintain a sufficient driving capacity, a capacitor of 10μF or larger is recommended for VCC. If a single VCC capacitor cannot provide enough power supply for the chip, an external charging circuit is recommended (see Figure 2).

When VCC drops below VCC_{STOP}, the IC stops working, and the internal high-voltage regulator recharges the VCC capacitor.

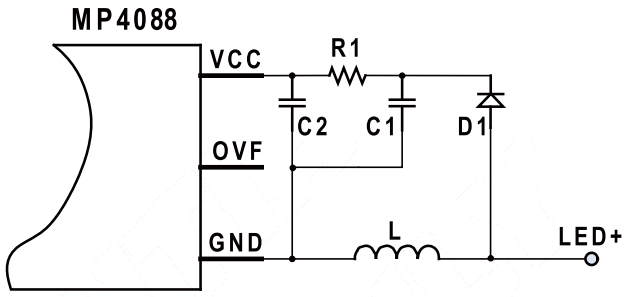


Figure 2: VCC Charging Circuit

When a fault conditions occurs, such as OVP or OTP, the MP4088 stops working, and an internal current source (ICC_LATCH) discharges the VCC capacitor. After VCC drops below VCC_{PRO}, the internal high-voltage regulator recharges the VCC capacitor. The restart time can be calculated with Equation (1):

$$t_{RESTART} = C_{VCC} \times \frac{VCC_{NOR} - VCC_{PRO}}{I_{CC_LATCH}} + C_{VCC} \times \frac{VCC_{OFF} - VCC_{PRO}}{I_{REGULATOR}} \quad (1)$$

Figure 3 shows the typical waveform with VCC under-voltage lockout.

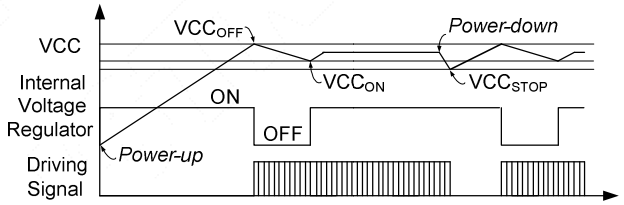


Figure 3: VCC Under-Voltage Lockout (UVLO)

Constant Current Operation

The MP4088 is a highly integrated driver. The internal feedback logic responds to the internal sample and hold circuit to achieve constant output-current regulation. The voltage of the internal sampling capacitor (V_{FB}) is compared to the internal reference (V_{REF}). When the sampling capacitor voltage (V_{FB}) falls below the reference voltage, indicating an insufficient output current, the integrated MOSFET is turned on. The on period is determined by the peak current limit. After the on period elapses, the integrated MOSFET turns off (see Figure 4).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

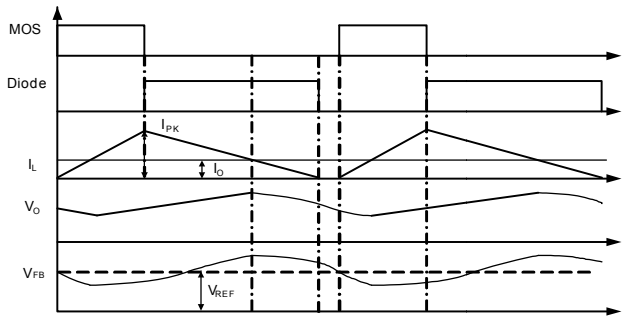


Figure 4: V_{FB} vs. I_{OUT}

The inductor's average current can be regulated by monitoring the internal sampling capacitor voltage. The inductor average current can be calculated with Equation (2):

$$I_{L_AVG} = \frac{V_{REF}}{R_S} \quad (2)$$

The peak inductor current can be calculated with Equation (3):

$$I_{PK} = \frac{V_{CS_LIMIT}}{R_S} \quad (3)$$

Where R_S is the sense resistor connected from CS to GND.

Minimum Operating Frequency Limit

The MP4088 incorporates a minimum operating frequency (22kHz) to eliminate audible noise. When the operating frequency is less than 22kHz, the internal peak current regulator decreases the peak current value to keep the operating frequency constant at about 22kHz.

Minimum Off-Time Limit

The MP4088 implements a minimum off-time limit. During normal operation, the minimum off-time limit is 9.3μs. In the start-up period, the minimum off-time limit is shortened gradually from 3.5 times to 1.2 times the normal minimum off-time (see Figure 5). Each minimum off-time limit lasts for 32 switching cycles. This process ensures a soft-start function of the IC to safely start up the part.

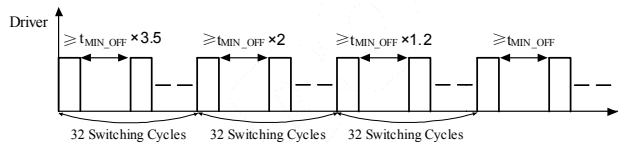


Figure 5: t_{OFF_MIN} at Start-Up

Thermal Protection

To protect the IC and the system from thermal damage, the MP4088 reduces the reference to decrease the output current. This limits the temperature rising speed of the IC when the junction temperature exceeds 145°C. The output current drops to around 20% when the IC temperature rises to 160°C. Once the junction temperature exceeds 160°C, the MP4088 shuts down the switching cycle. Once the junction temperature drops below 110°C, the power supply resumes operation. During thermal shutdown, VCC is discharged to VCC_{PRO}, and then it is recharged by the internal high-voltage regulator.

Over-Voltage Protection (OVP)

If V_{OVF} is higher than V_{OVP} when the MOSFET turns off, the MP4088 stops working and a restart cycle begins. When OVP occurs, the chip works in hiccup mode. The MP4088 monitors the OVF voltage continuously, and VCC discharges and recharges repeatedly. The MP4088 resumes operation once the fault is removed.

Short-Circuit Protection (SCP)

When an LED short circuit occurs, the switching off-time is extended. Due to the minimum operating frequency limit, the IC reduces the switching frequency automatically and achieves a closed loop control. The output power at this condition is limited at a safe range. The MP4088 resumes normal operation once the short circuit is released.

Leading Edge Blanking (LEB)

Internal leading edge blanking (LEB) is employed to prevent a switching pulse from terminating prematurely due to parasitic capacitance discharging when the MOSFET turns on. During the blanking time, the path from CS to the current comparator input is blocked. Figure 6 shows the leading-edge blanking time.

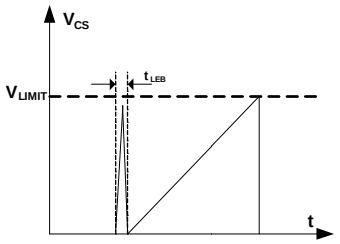


Figure 6: Leading Edge Blanking (LEB)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

APPLICATION INFORMATION

Selecting the **Inductor**

The MP4088 has a minimum off-time limit. The inductor current ripple at CCM is determined by the inductor value and the minimum off-time limit. The current ripple is limited to 80% to achieve a tradeoff between the power factor and the dimming performance. The inductance value can be calculated with Equation (4):

$$L = \frac{V_{OUT} \times t_{OFF_MIN}}{0.8 \times I_{PEAK}} \quad (4)$$

If the inductance value is too large, then the switching frequency is low and the EMI performance is good. However, the TRIAC dimming performance is poor in this condition. If the inductance value is too small, the TRIAC dimming performance is good, but the system may work in an open-loop condition, making the current consistency poor. Therefore, a tradeoff must be made.

Freewheeling Diode

The diode should have a maximum reverse-voltage rating greater than the maximum input voltage. The current rating of the diode is determined by the output current, which should be larger than 1.5 to 2 times the output current.

Slow diodes cause excessive and unwanted leading edge current spikes during start-up. A long reverse-recovery time of the freewheeling diode can affect efficiency and circuit operation as well. An ultrafast diode (t_{rr} < 75ns), such as WUGC10JH or ES1G, is recommended.

Over-Voltage Protection (OVP) Point Set

A feedback resistor is used to detect an over-voltage condition. Figure 7 shows the connection of the feedback resistor.

The MP4088 employs an over-voltage protection (OVP). When OVP is triggered, the maximum output voltage can be calculated with Equation (5):

$$V_{OUT_OVP} = V_{OVP} \cdot \frac{R2 + R3}{R2} - V_D \quad (5)$$

Where V_D is the freewheeling diode forward voltage drop.

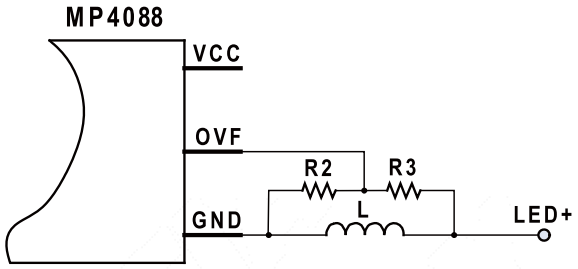


Figure 7: Feedback Resistor Connection

The upper feedback resistor (R3) should be larger than 100kΩ to avoid an efficiency reduction in the application. A 1% tolerance type is recommended to achieve accurate protection.

Dummy Load

The dummy load is used to consume the power transferred to the output capacitor when OVP occurs. The IC works in hiccup mode without any power consumption.

Normally, a dummy load less than 1mA is recommended. This does not deteriorate the system efficiency but can guarantee normal over-voltage protection.

Surge

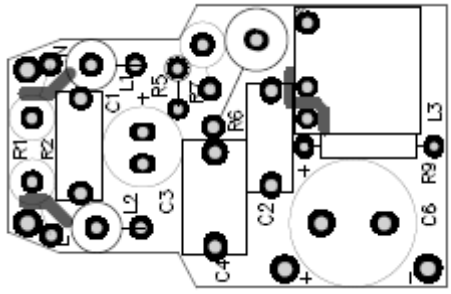
Place an appropriate RCD snubber beside the diode rectifier bridge for optimal surge performance. For most applications, a 1μF/400V electrolytic capacitor with a 1000V diode is recommended. The resistor can be as large as 1MΩ to reduce power loss during normal operation.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

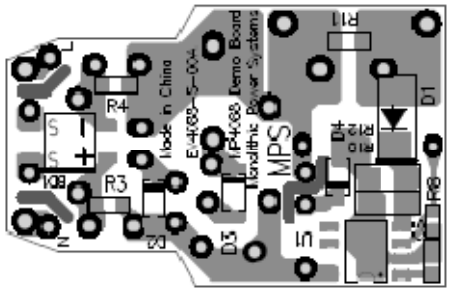
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation, good EMI, and good thermal performance, especially in very small LED applications. For best results, refer to Figure 8 and follow the guidelines below:

1. Keep the loop formed between the MP4088, the inductor, the freewheeling diode, and the output capacitor as small as possible for better EMI.
2. Place the AC input far away from the switching nodes to minimize the noise coupling that may bypass the input filter.
3. Place the VCC capacitor as close to VCC and GND as possible.
4. Place the feedback resistor as close to OVF as possible to minimize the feedback sampling loop and minimize the noise coupling route.
5. If using SOIC-8 EP package IC, remember to connect the exposed pad to GND plane.



Top Layer



Bottom Layer

Figure 8: Recommended PCB Layout

Design Example

Table 1 is a design example following the application guidelines based on the following specifications:

Table 1: Design Example

V_{IN}	198VAC to 265VAC
V_{OUT}	55V
I_{OUT}	100mA

Figure 9 shows the detailed application schematic. This circuit is used for the typical performance and circuit waveforms. For more device applications, please refer to the related evaluation board datasheets.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

Figure 9 shows a typical application example of a 55V, 100mA, non-isolated, buck-boost topology LED driver with the MP4088.

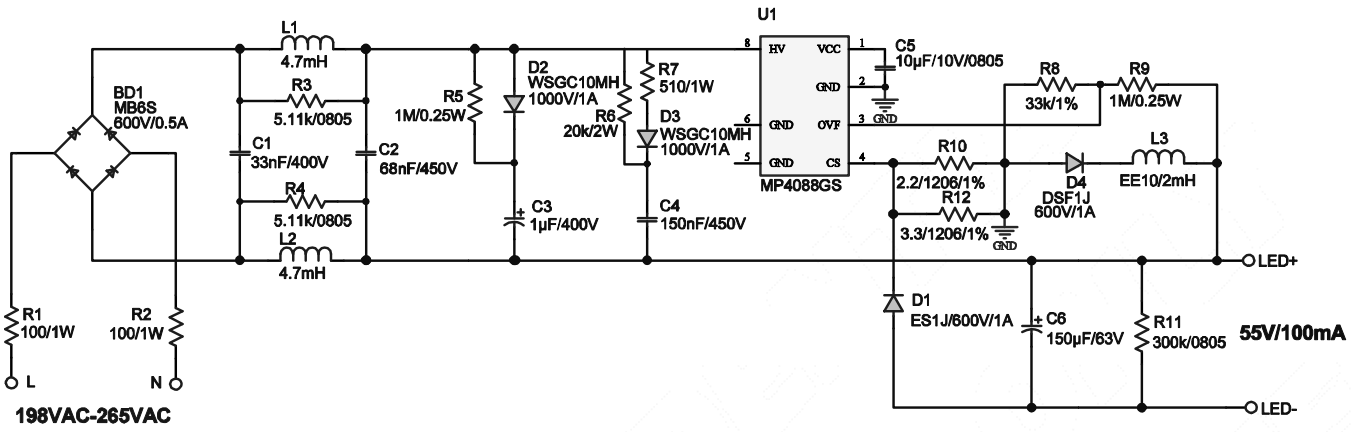
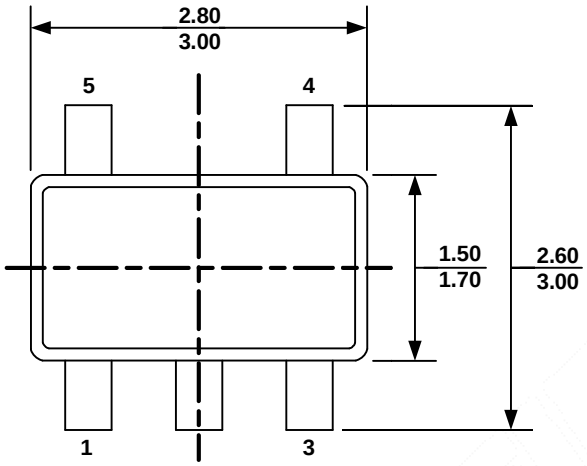


Figure 9: Typical Buck-Boost Converter Application

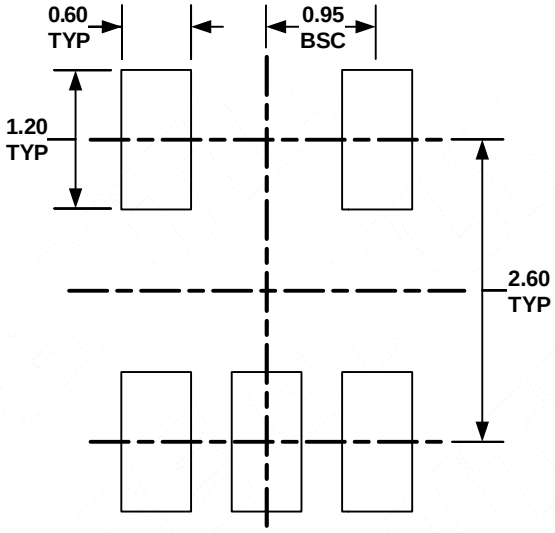
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

PACKAGE INFORMATION

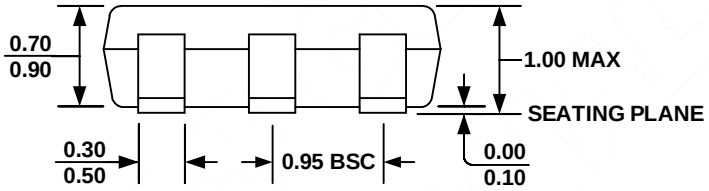
TSOT23-5



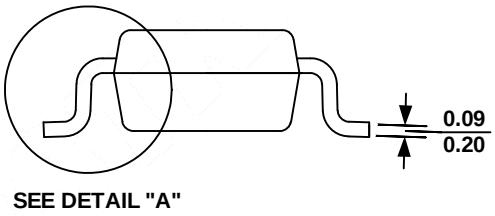
TOP VIEW



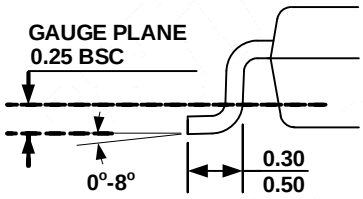
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

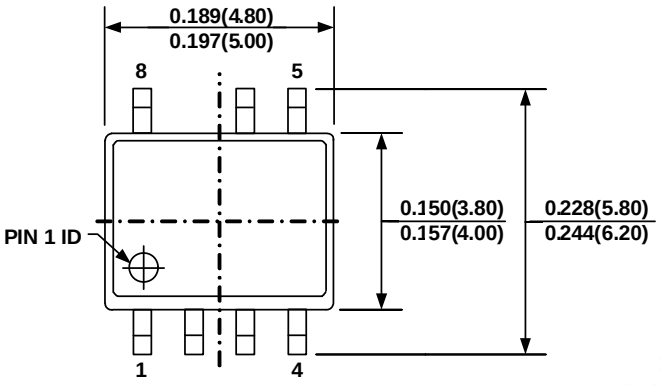
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA.
6) DRAWING IS NOT TO SCALE

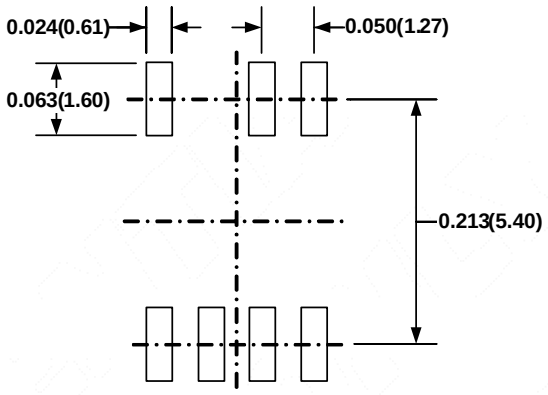
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

PACKAGE INFORMATION *(continued)*

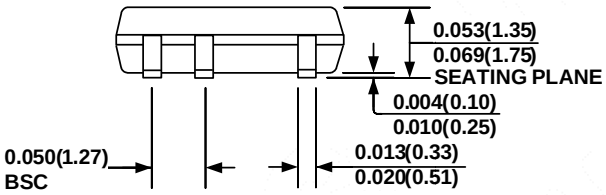
SOIC8-7A



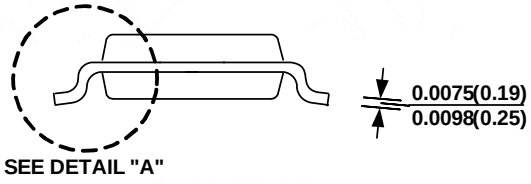
TOP VIEW



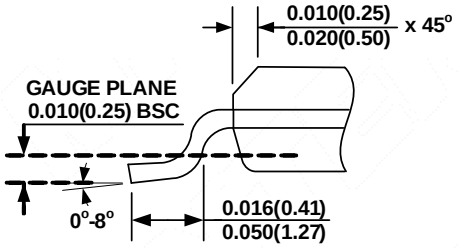
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

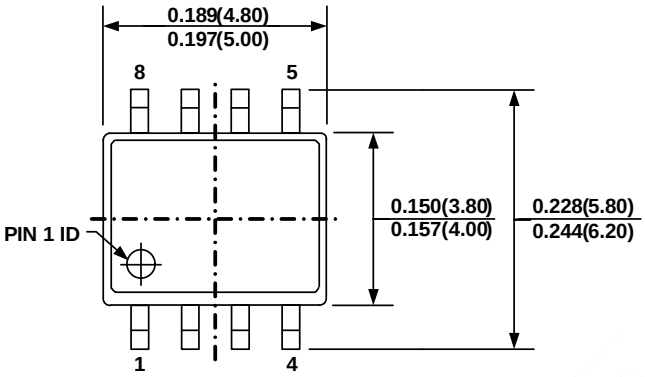
NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) JEDEC REFERENCE IS MS-012.
6) DRAWING IS NOT TO SCALE

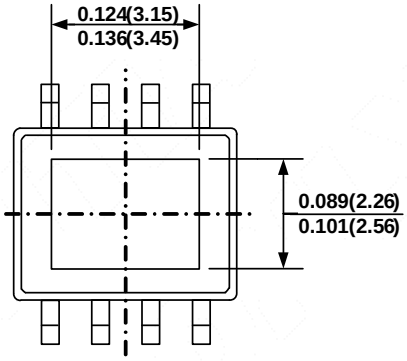
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

PACKAGE INFORMATION *(continued)*

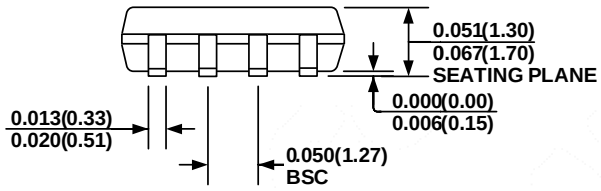
SOIC-8 EP



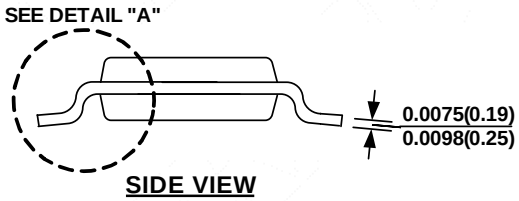
TOP VIEW



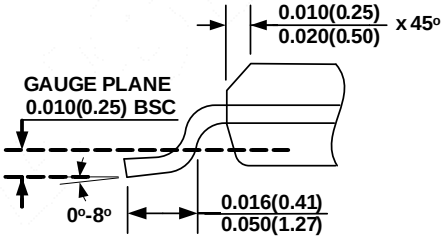
BOTTOM VIEW



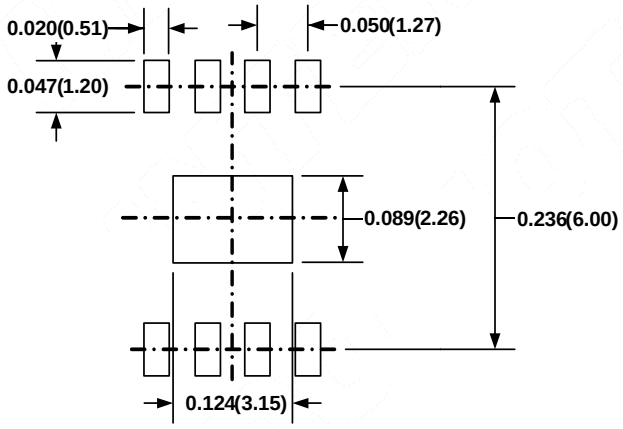
FRONT VIEW



SIDE VIEW



DETAIL "A"



RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.