



**Please note that Cypress is an Infineon Technologies Company.**

The document following this cover page is marked as "Cypress" document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

**Continuity of document content**

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

**Continuity of ordering part numbers**

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

## 8-Mbit (512K words × 16-bit) Static RAM with Error-Correcting Code (ECC)

### Features

- AEC-Q100 Qualified
- Ultra-low standby power
  - Typical standby current: 5  $\mu$ A
  - Maximum standby current: 35  $\mu$ A
- High speed: 45 ns/55 ns
- Embedded error-correcting code (ECC) for single-bit error correction<sup>[1, 2]</sup>
- Temperature ranges:
  - Automotive-A: -40 °C to +85 °C
- Wide operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V
- 1.5-V data retention
- Transistor-transistor logic (TTL)-compatible inputs and outputs
- Available in Pb-free 48-ball VFBGA, 48-pin TSOP II, and 44-pin TSOP I packages

### Functional Description

CY62157G is a high-performance CMOS low-power (MoBL®) SRAM device with embedded ECC. This device is offered in dual chip-enable.

Devices with dual chip-enable are accessed by asserting both chip-enable inputs –  $\overline{CE}_1$  as LOW and  $CE_2$  as HIGH.

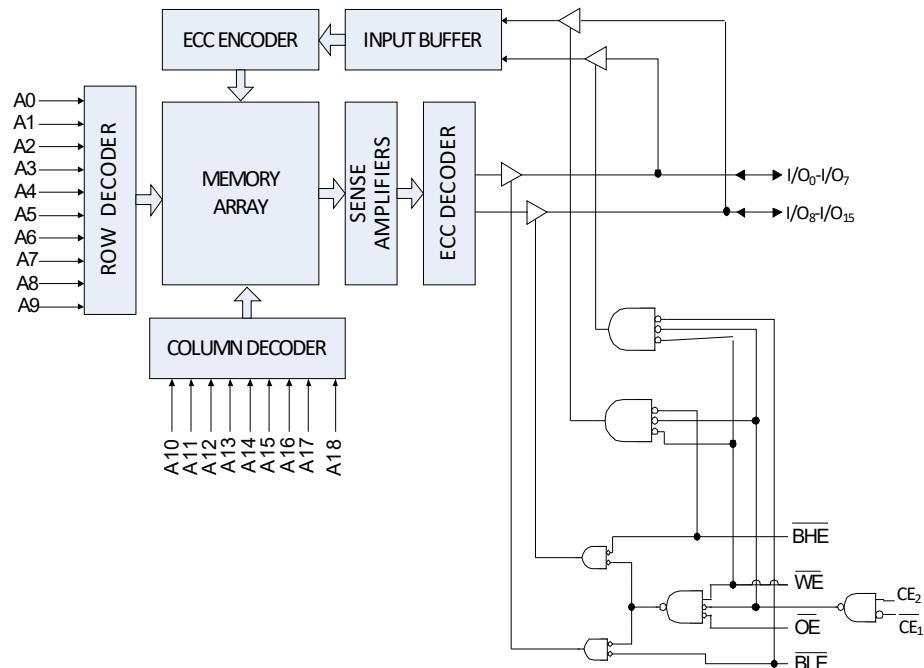
### Product Portfolio

Product	Range	$V_{CC}$ Range (V)	Speed (ns)	Power Dissipation			
				Operating $I_{CC}$ , (mA), $f = f_{max}$		Standby, $I_{SB2}$ ( $\mu$ A)	
				Typ [3]	Max	Typ [3]	Max
CY62157G18	Automotive-A	1.65 V to 2.2 V	55	18	22	4.5	8
CY62157G30		2.2 V to 3.6 V	45	18	25	1.4	6.5

#### Notes

1. SER FIT rate <0.1 FIT/Mb. Refer to [AN88889](#) for details.
2. This device does not support automatic write-back on error detection.
3. Indicates the value for the center of distribution at 3.0 V (or 1.8 V), 25 °C and not 100% tested.

## Logic Block Diagram – CY62157G

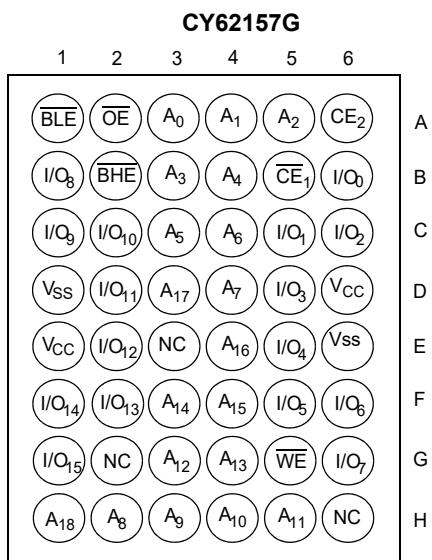


## Contents

<b>Pin Configurations</b> .....	<b>4</b>
<b>Maximum Ratings</b> .....	<b>6</b>
<b>Operating Range</b> .....	<b>6</b>
<b>DC Electrical Characteristics</b> .....	<b>7</b>
<b>Capacitance</b> .....	<b>8</b>
<b>Thermal Resistance</b> .....	<b>8</b>
<b>AC Test Loads and Waveforms</b> .....	<b>8</b>
<b>Data Retention Characteristics</b> .....	<b>9</b>
<b>Data Retention Waveform</b> .....	<b>9</b>
<b>Switching Characteristics</b> .....	<b>10</b>
<b>Switching Waveforms</b> .....	<b>11</b>
<b>Truth Table – CY62157G</b> .....	<b>15</b>
<b>Ordering Information</b> .....	<b>16</b>
Ordering Code Definitions .....	16
<b>Package Diagrams</b> .....	<b>17</b>
<b>Acronyms</b> .....	<b>20</b>
<b>Document Conventions</b> .....	<b>20</b>
Units of Measure .....	20
<b>Document History Page</b> .....	<b>21</b>
<b>Sales, Solutions, and Legal Information</b> .....	<b>22</b>
Worldwide Sales and Design Support .....	22
Products .....	22
PSoC® Solutions .....	22
Cypress Developer Community .....	22
Technical Support .....	22

## Pin Configurations

**Figure 1. 48-ball VFBGA Pinout** <sup>[4]</sup>



**Figure 2. 44-pin TSOP II Pinout** <sup>[4]</sup>

**CY62157G**

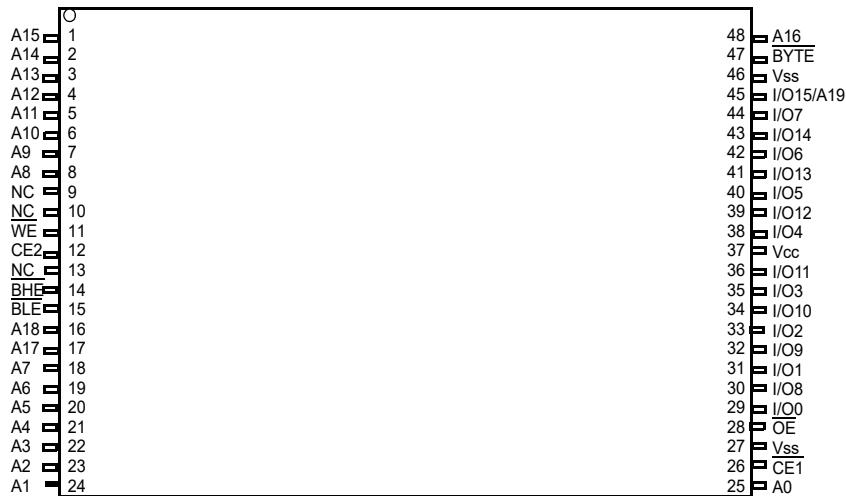
A <sub>4</sub>	1	44	A <sub>5</sub>
A <sub>3</sub>	2	43	A <sub>6</sub>
A <sub>2</sub>	3	42	A <sub>7</sub>
A <sub>1</sub>	4	41	OE
A <sub>0</sub>	5	40	BHE
CE	6	39	BLE
I/O <sub>0</sub>	7	38	I/O <sub>15</sub>
I/O <sub>1</sub>	8	37	I/O <sub>14</sub>
I/O <sub>2</sub>	9	36	I/O <sub>13</sub>
I/O <sub>3</sub>	10	35	I/O <sub>12</sub>
V <sub>CC</sub>	11	34	V <sub>SS</sub>
V <sub>SS</sub>	12	33	V <sub>CC</sub>
I/O <sub>4</sub>	13	32	I/O <sub>11</sub>
I/O <sub>5</sub>	14	31	I/O <sub>10</sub>
I/O <sub>6</sub>	15	30	I/O <sub>9</sub>
I/O <sub>7</sub>	16	29	I/O <sub>8</sub>
WE	17	28	A <sub>8</sub>
A <sub>18</sub>	18	27	A <sub>9</sub>
A <sub>17</sub>	19	26	A <sub>10</sub>
A <sub>16</sub>	20	25	A <sub>11</sub>
A <sub>15</sub>	21	24	A <sub>12</sub>
A <sub>14</sub>	22	23	A <sub>13</sub>

**Note**

4. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.

## Pin Configurations

**Figure 3. 48-pin TSOP I Pinout (Top View)** <sup>[5, 6]</sup>



### Notes

5. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
6. Tie the BYTE pin in the 48-pin TSOP I package to V<sub>CC</sub> to use the device as a 512K × 16 SRAM. The 48-pin TSOP I package can also be used as a 1M × 8 SRAM by tying the BYTE signal to V<sub>SS</sub>. In the 1M × 8 configuration, Pin 45 is the extra address line A19, while BHE, BLE, and I/O<sub>8</sub> to I/O<sub>14</sub> pins are not used and can be left floating.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature	.....	–65 °C to + 150 °C
Ambient temperature with power applied	.....	–55 °C to + 125 °C
Supply voltage to ground potential [7]	.....	–0.5 V to $V_{CC}$ + 0.5 V
DC voltage applied to outputs in HI-Z state [7]	.....	–0.5 V to $V_{CC}$ + 0.5 V

DC input voltage [7]	.....	–0.5 V to $V_{CC}$ + 0.5 V
Output current into outputs (LOW)	.....	20 mA
Static discharge voltage (MIL-STD-883, Method 3015)	.....	>2001 V
Latch-up current	.....	>140 mA

## Operating Range

Grade	Ambient Temperature	$V_{CC}$
Automotive-A	–40 °C to +85 °C	1.65 V to 2.2 V 2.2 V to 3.6 V

### Note

7.  $V_{IL(min)} = -2.0$  V and  $V_{IH(max)} = V_{CC} + 2$  V for pulse durations of <2 ns.

## DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45/55 ns (Automotive-A)			Unit		
			Min	Typ [9]	Max			
V <sub>OH</sub>	Output HIGH voltage	1.65 V to 2.2 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1 mA	1.4	-	-		
		2.2 V to 2.7 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1 mA	2.0	-	-		
		2.7 V to 3.6 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -1.0 mA	2.4	-	-		
V <sub>OL</sub>	Output LOW voltage	1.65 V to 2.2 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 0.1 mA	-	-	0.2		
		2.2 V to 2.7 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 0.1 mA	-	-	0.4		
		2.7 V to 3.6 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 2.1 mA	-	-	0.4		
V <sub>IH</sub>	Input HIGH voltage <sup>[8]</sup>	1.65 V to 2.2 V	-	1.4	-	V <sub>CC</sub> + 0.2		
		2.2 V to 2.7 V	-	1.8	-	V <sub>CC</sub> + 0.3		
		2.7 V to 3.6 V	-	2.0	-	V <sub>CC</sub> + 0.3		
V <sub>IL</sub>	Input LOW voltage <sup>[8]</sup>	1.65 V to 2.2 V	-	-0.2	-	0.4		
		2.2 V to 2.7 V	-	-0.3	-	0.6		
		2.7 V to 3.6 V	-	-0.3	-	0.8		
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1.0	-	+1.0	µA		
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output disabled	-1.0	-	+1.0	µA		
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	1.65 V to 2.2 V	V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA, CMOS levels	f = f <sub>MAX</sub>	-	18	22	mA
		2.2 V to 3.6 V	V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA, CMOS levels	f = 1 MHz	-	6	7	mA
I <sub>SB1</sub> <sup>[10]</sup>	Automatic power down current – CMOS inputs; V <sub>CC</sub> = 2.2 to 3.6 V	CE <sub>1</sub> ≥ V <sub>CC</sub> – 0.2 V or CE <sub>2</sub> ≤ 0.2 V or (BHE and BLE) ≥ V <sub>CC</sub> – 0.2 V,	-	1.4	6.5	µA		
I <sub>SB1</sub> <sup>[10]</sup>	Automatic power down current – CMOS inputs; V <sub>CC</sub> = 1.65 to 2.2 V	V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V or V <sub>IN</sub> ≤ 0.2 V, f = f <sub>max</sub> (address and data only), f = 0 (OE, and WE), V <sub>CC</sub> = V <sub>CC(max)</sub>	-	-	8	µA		
I <sub>SB2</sub> <sup>[10]</sup>	Automatic power down current – CMOS inputs; V <sub>CC</sub> = 2.2 to 3.6 V	CE <sub>1</sub> ≥ V <sub>CC</sub> – 0.2 V or CE <sub>2</sub> ≤ 0.2 V or (BHE and BLE) ≥ V <sub>CC</sub> – 0.2 V,	-	1.4	6.5 <sup>[11]</sup>	µA		
I <sub>SB2</sub> <sup>[10]</sup>	Automatic power down current – CMOS inputs; V <sub>CC</sub> = 1.65 to 2.2 V	V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V or V <sub>IN</sub> ≤ 0.2 V, f = 0, V <sub>CC</sub> = V <sub>CC(max)</sub>	-	-	8	µA		

### Notes

8. V<sub>IL(min)</sub> = -2.0 V and V<sub>IH(max)</sub> = V<sub>CC</sub> + 2 V for pulse durations of < 2 ns.

9. Indicates the value for the center of Distribution at 3.0 V (or 1.8V), 25 °C and not 100% tested.

10. Chip enables (CE<sub>1</sub> and CE<sub>2</sub>) and BHE, BLE must be tied to CMOS levels to meet the I<sub>SB1</sub>/I<sub>SB2</sub>/I<sub>CCDR</sub> spec. Other inputs can be left floating.

11. ISB2 (max.) for 44TSOP package = 8µA, only when the chip is deselected by disabling both BHE and BLE.

## Capacitance

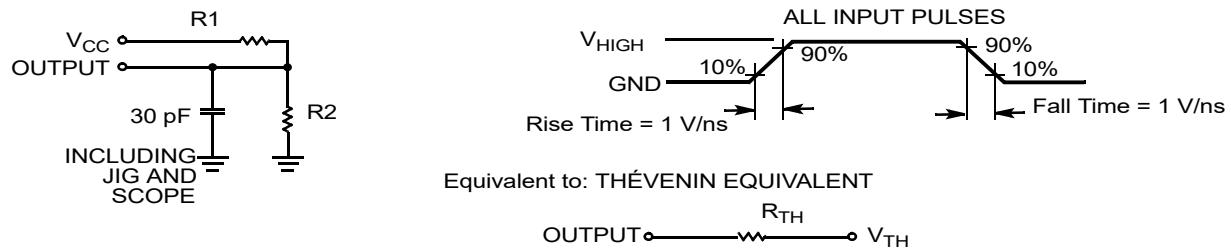
Parameter <sup>[12]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25^\circ C, f = 1 \text{ MHz}, V_{CC} = V_{CC(\text{typ})}$	10	pF
$C_{OUT}$	Output capacitance		10	pF

## Thermal Resistance

Parameter <sup>[12]</sup>	Description	Test Conditions	48-ball VFBGA	44-pin TSOP II	48-pin TSOP I	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	36.92	65.91	60.07	°C/W
$\Theta_{JC}$	Thermal resistance (junction to case)		13.55	13.96	9.73	°C/W

## AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms



Parameters	1.8 V	2.5 V	3.0 V	Unit
R1	13500	16667	1103	$\Omega$
R2	10800	15385	1554	$\Omega$
$R_{TH}$	6000	8000	645	$\Omega$
$V_{TH}$	0.80	1.20	1.75	V

**Note**

12. Tested initially and after any design or process changes that may affect these parameters.

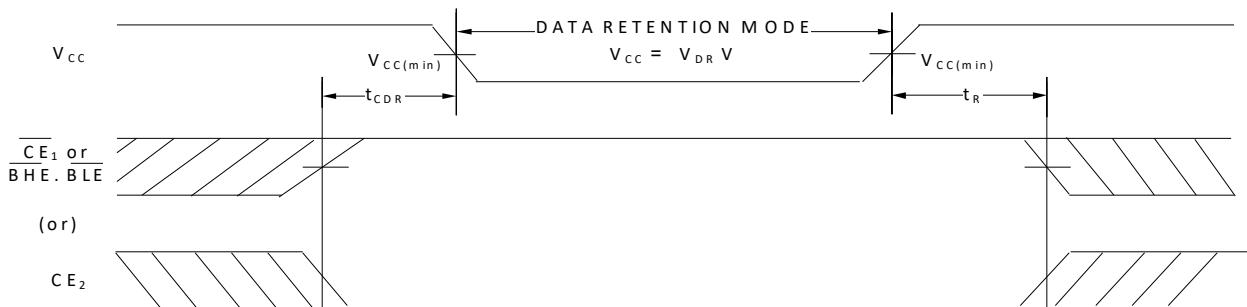
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	(Automotive-A)			Unit
			Min	Typ [13]	Max	
$V_{DR}$	$V_{CC}$ for data retention	$2.2 \text{ V} < V_{CC} \leq 3.6 \text{ V}$	1	—	—	V
		$1.65 \text{ V} < V_{CC} \leq 2.2 \text{ V}$	1	—	—	V
$I_{CCDR}^{[14]}$	Data-retention current (For 3.3-V typical device)	$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $\overline{CE}_2 \leq 0.2 \text{ V}$ or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$	$2.2 \text{ V} < V_{CC} \leq 3.6 \text{ V}$	—	1.4	$\mu\text{A}$
		$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $\overline{CE}_2 \leq 0.2 \text{ V}$ or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$	$V_{CC} = 1.5 \text{ V}$	—	3.2	$\mu\text{A}$
		$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $\overline{CE}_2 \leq 0.2 \text{ V}$ or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$	$V_{CC} = 1.2 \text{ V}$	—	4	$\mu\text{A}$
		$1.2 \text{ V} < V_{CC} \leq 2.2 \text{ V}$ $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $\overline{CE}_2 \leq 0.2 \text{ V}$ or $(\overline{BHE} \text{ and } \overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$	—	5	9	—
$t_{CDR}^{[15]}$	Chip deselect to data-retention time	—	0	—	—	—
$t_R^{[16]}$	Operation-recovery time	—	45/55	—	—	ns

## Data Retention Waveform

Figure 5. Data-Retention Waveform [17]



### Notes

13. Indicates the value for the center of distribution at 3.0 V, 25°C and not 100% tested.
14. Chip enables ( $\overline{CE}_1$  and  $CE_2$ ) must be tied to CMOS levels to meet the  $I_{SB1}/I_{SB2}/I_{CCDR}$  spec. Other inputs can be left floating.
15. Tested initially and after any design or process changes that may affect these parameters.
16. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(\min)} \geq 100 \mu\text{s}$  or stable at  $V_{CC(\min)} \geq 100 \mu\text{s}$ .
17.  $\overline{BHE} \cdot \overline{BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Deselect the chip by either disabling the chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .

## Switching Characteristics

Parameter <sup>[18]</sup>	Description	55 ns		45 ns		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
$t_{RC}$	Read cycle time	55	–	45	–	ns
$t_{AA}$	Address to data valid	–	55	–	45	ns
$t_{OHA}$	Data hold from address change	10	–	10	–	ns
$t_{ACE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to data valid / $\overline{CE}$ LOW	–	55	–	45	ns
$t_{DOE}$	$OE$ LOW to data valid / $\overline{OE}$ LOW	–	25	–	22	ns
$t_{LZOE}$	$OE$ LOW to Low Z <sup>[19]</sup>	5	–	5	–	ns
$t_{HZOE}$	$OE$ HIGH to High Z <sup>[19, 20]</sup>	–	20	–	18	ns
$t_{LZCE}$	$CE_1$ LOW and $CE_2$ HIGH to Low Z <sup>[19]</sup>	10	–	10	–	ns
$t_{HZCE}$	$CE_1$ HIGH and $CE_2$ LOW to High Z <sup>[19, 20]</sup>	–	20	–	18	ns
$t_{PU}$	$CE_1$ LOW and $CE_2$ HIGH to power-up	0	–	0	–	ns
$t_{PD}$	$CE_1$ HIGH and $CE_2$ LOW to power-down	–	55	–	45	ns
$t_{DBE}$	$BLE$ / $BHE$ LOW to data valid	–	55	–	45	ns
$t_{LZBE}$	$BLE$ / $BHE$ LOW to Low Z <sup>[19]</sup>	5	–	5	–	ns
$t_{HZBE}$	$BLE$ / $BHE$ HIGH to High Z <sup>[19, 20]</sup>	–	20	–	18	ns
<b>Write Cycle</b> <sup>[21,22]</sup>						
$t_{WC}$	Write cycle time	55	–	45	–	ns
$t_{SCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to write end	40	–	35	–	ns
$t_{AW}$	Address setup to write end	40	–	35	–	ns
$t_{HA}$	Address hold from write end	0	–	0	–	ns
$t_{SA}$	Address setup to write start	0	–	0	–	ns
$t_{PWE}$	$WE$ pulse width	40	–	35	–	ns
$t_{BW}$	$BLE$ / $BHE$ LOW to write end	40	–	35	–	ns
$t_{SD}$	Data setup to write end	25	–	25	–	ns
$t_{HD}$	Data hold from write end	0	–	0	–	ns
$t_{HZWE}$	$WE$ LOW to High Z <sup>[19, 20]</sup>	–	20	–	18	ns
$t_{LZWE}$	$WE$ HIGH to Low Z <sup>[19]</sup>	10	–	10	–	ns

### Notes

18. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for  $V_{CC} \geq 3$  V) and  $V_{CC}/2$  (for  $V_{CC} < 3$  V), and input pulse levels of 0 to 3 V (for  $V_{CC} \geq 3$  V) and 0 to  $V_{CC}$  (for  $V_{CC} < 3$  V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.
19. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
20.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.
21. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  or  $\overline{BLE}$  or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write. Any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write
22. The minimum write cycle pulse width for the Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be equal to the sum of  $t_{SD}$  and  $t_{HZWE}$ .

## Switching Waveforms

Figure 6. Read Cycle No. 1 of CY62157G (Address Transition Controlled) [23, 24]

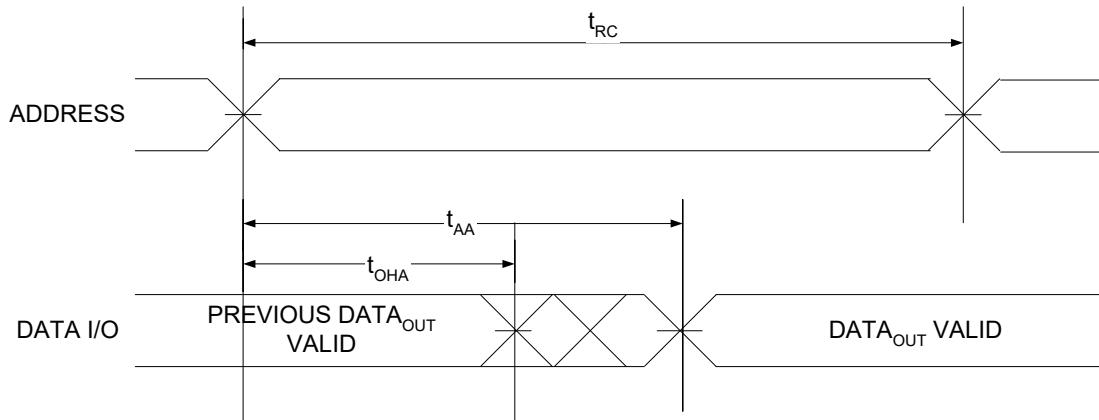
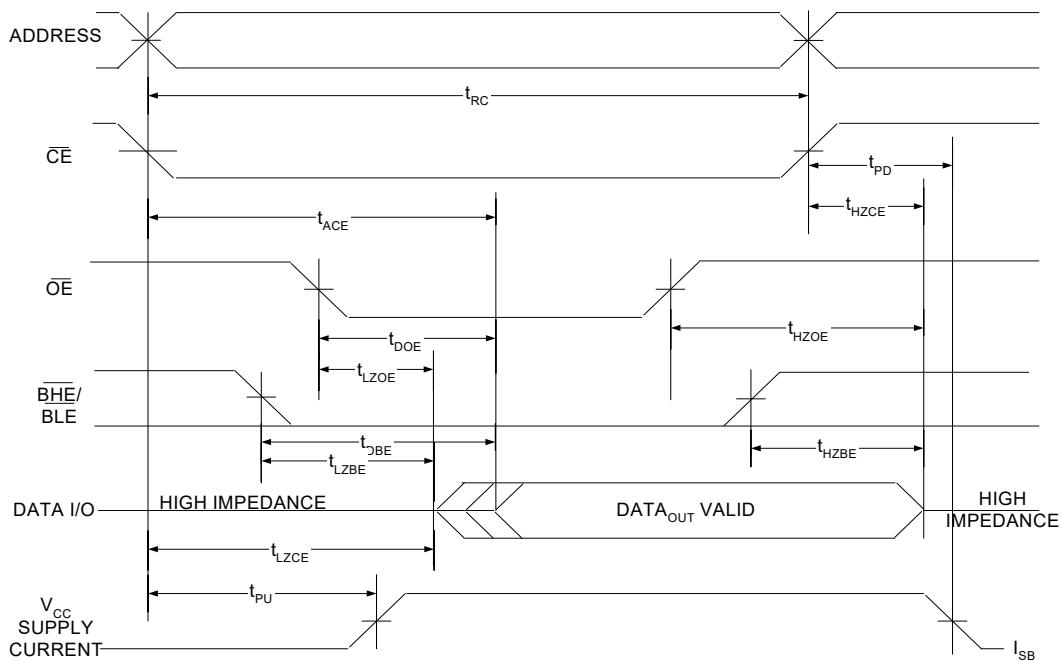


Figure 7. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [24, 25, 26]

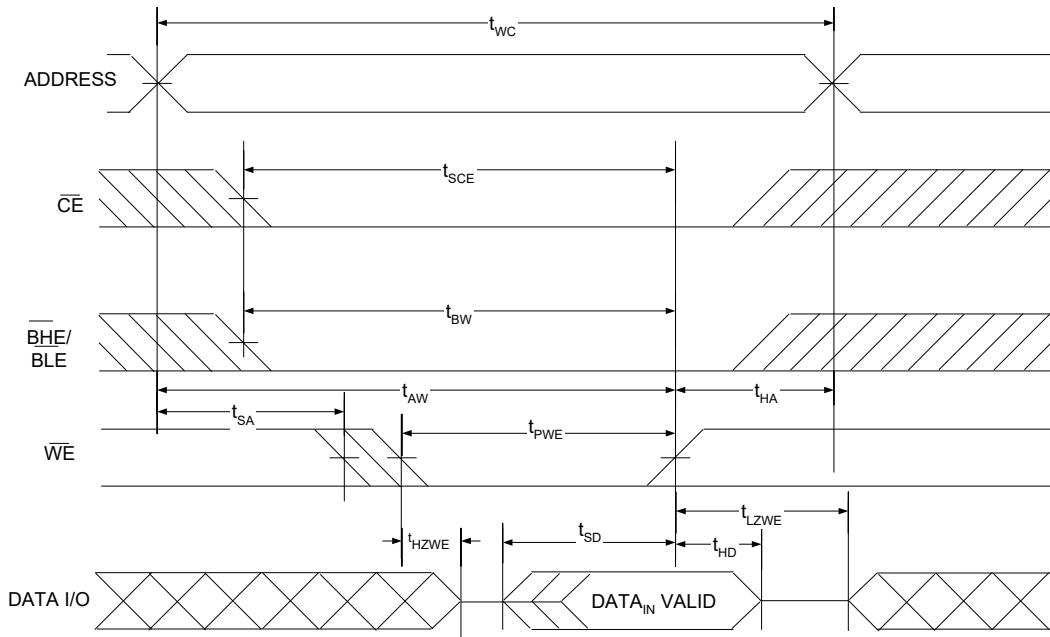


### Notes

23. The device is continuously selected.  $\overline{OE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  or  $\overline{BLE}$  or both =  $V_{IL}$ .
24.  $\overline{WE}$  is HIGH for read cycle.
25. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
26. Address valid prior to or coincident with  $CE$  LOW transition.

## Switching Waveforms (continued)

**Figure 8. Write Cycle No. 1 (WE Controlled) [27, 28, 29]**

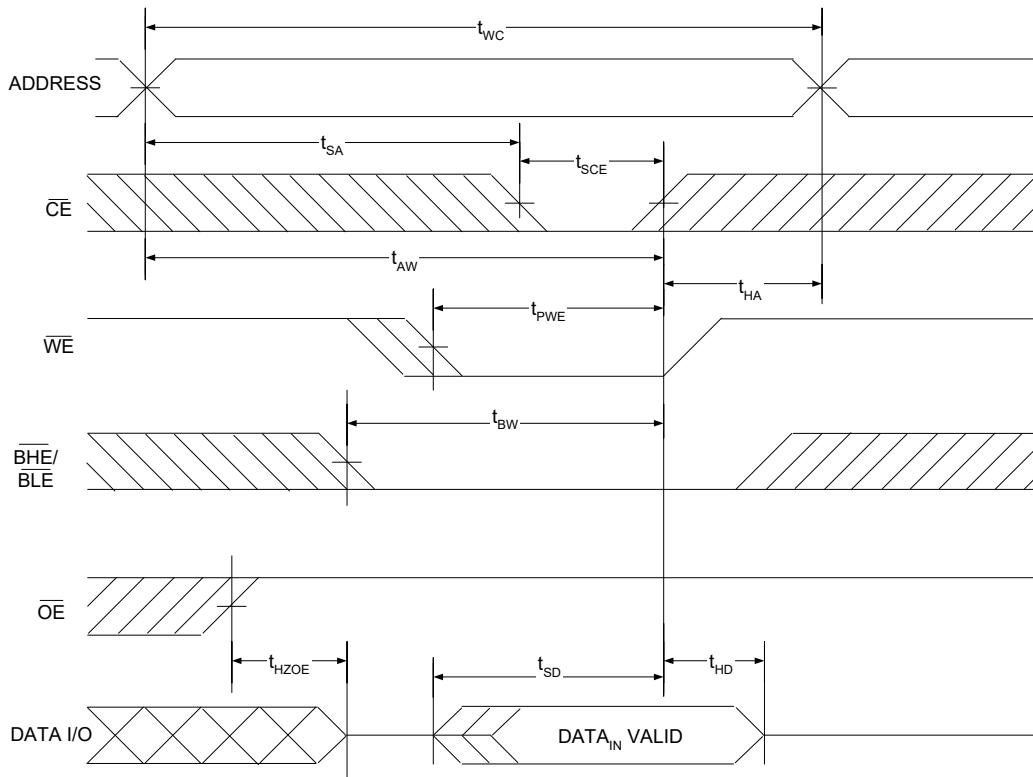


### Notes

27. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
28. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  or  $\overline{BLE}$  or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
29. Data I/O is in HI-Z state if  $\overline{CE} = V_{IH}$ , or  $\overline{OE} = V_{IH}$  or  $\overline{BHE}$ , and/or  $\overline{BLE} = V_{IH}$ .

## Switching Waveforms (continued)

**Figure 9. Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled) [30, 31, 32]**

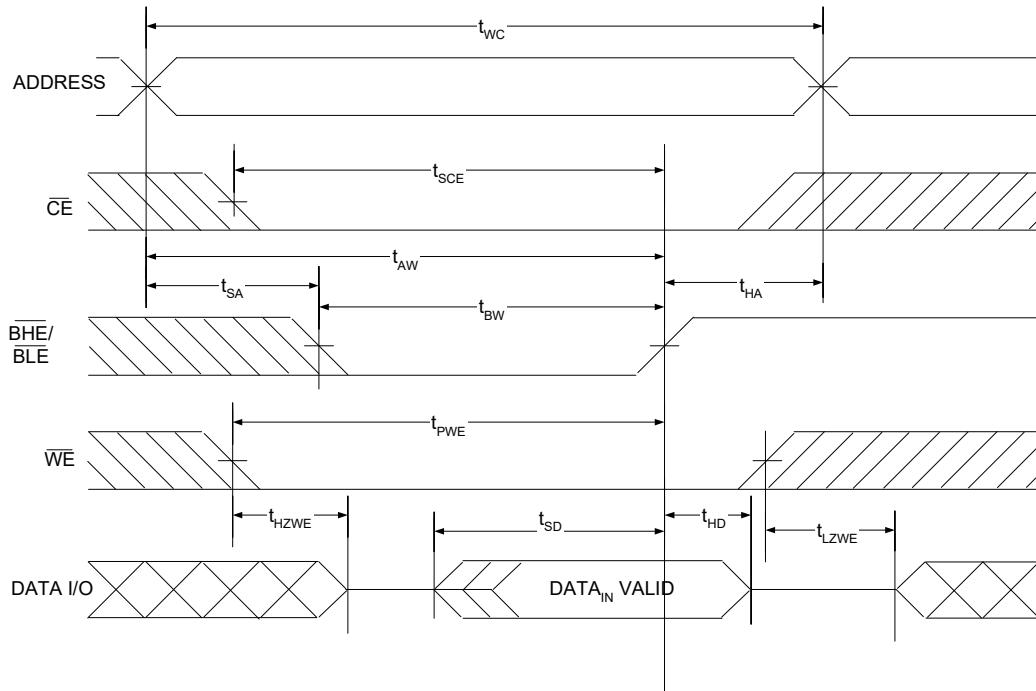


### Notes

30. For all dual chip enable devices,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.
31. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{IL}$ ,  $\overline{\text{CE}}_1 = V_{IL}$ ,  $\overline{\text{BHE}} = V_{IL}$  or  $\overline{\text{BLE}} = V_{IL}$  and  $\text{CE}_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
32. Data I/O is in high impedance state if  $\overline{\text{CE}} = V_{IH}$ , or  $\overline{\text{OE}} = V_{IH}$  or  $\overline{\text{BHE}} = V_{IH}$ , and/or  $\overline{\text{BLE}} = V_{IH}$ .

## Switching Waveforms (continued)

**Figure 10. Write Cycle No. 3 ( $\overline{\text{BHE}}/\overline{\text{BLE}}$  controlled,  $\overline{\text{OE}}$  LOW) [33, 34, 35]**



### Notes

33. For all dual chip enable devices,  $\overline{\text{CE}}$  is the logical combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ . When  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH,  $\overline{\text{CE}}$  is LOW; when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW,  $\overline{\text{CE}}$  is HIGH.
34. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{IL}$ ,  $\overline{\text{CE}}_1 = V_{IL}$ ,  $\overline{\text{BHE}} = V_{IL}$  or  $\overline{\text{BLE}} = V_{IL}$  or both =  $V_{IL}$ , and  $\text{CE}_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
35. Data I/O is in high impedance state if  $\overline{\text{CE}} = V_{IH}$ , or  $\overline{\text{OE}} = V_{IH}$  or  $\overline{\text{BHE}} = V_{IH}$ , and/or  $\overline{\text{BLE}} = V_{IH}$ .

### Truth Table – CY62157G

<b><math>\overline{CE_1}</math></b>	<b><math>\overline{CE_2}</math></b>	<b><math>\overline{WE}</math></b>	<b><math>\overline{OE}</math></b>	<b><math>\overline{BHE}</math></b>	<b><math>\overline{BLE}</math></b>	<b>Inputs/Outputs</b>	<b>Mode</b>	<b>Power</b>
H	$X^{[36]}$	X	X	X	X	HI-Z	Deselect/Power-down	Standby ( $I_{SB}$ )
$X^{[36]}$	L	X	X	X	X	HI-Z	Deselect/Power-down	Standby ( $I_{SB}$ )
$X^{[36]}$	$X^{[36]}$	X	X	H	H	HI-Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	H	L	L	L	Data Out (I/O <sub>0</sub> –I/O <sub>15</sub> )	Read	Active ( $I_{CC}$ )
L	H	H	L	H	L	Data Out (I/O <sub>0</sub> –I/O <sub>7</sub> ); HI-Z (I/O <sub>8</sub> –I/O <sub>15</sub> )	Read	Active ( $I_{CC}$ )
L	H	H	L	L	H	HI-Z (I/O <sub>0</sub> –I/O <sub>7</sub> ); Data Out (I/O <sub>8</sub> –I/O <sub>15</sub> )	Read	Active ( $I_{CC}$ )
L	H	H	H	X	X	HI-Z	Output disabled	Active ( $I_{CC}$ )
L	H	L	X	L	L	Data In (I/O <sub>0</sub> –I/O <sub>15</sub> )	Write	Active ( $I_{CC}$ )
L	H	L	X	H	L	Data In (I/O <sub>0</sub> –I/O <sub>7</sub> ); HI-Z (I/O <sub>8</sub> –I/O <sub>15</sub> )	Write	Active ( $I_{CC}$ )
L	H	L	X	L	H	HI-Z (I/O <sub>0</sub> –I/O <sub>7</sub> ); Data In (I/O <sub>8</sub> –I/O <sub>15</sub> )	Write	Active ( $I_{CC}$ )

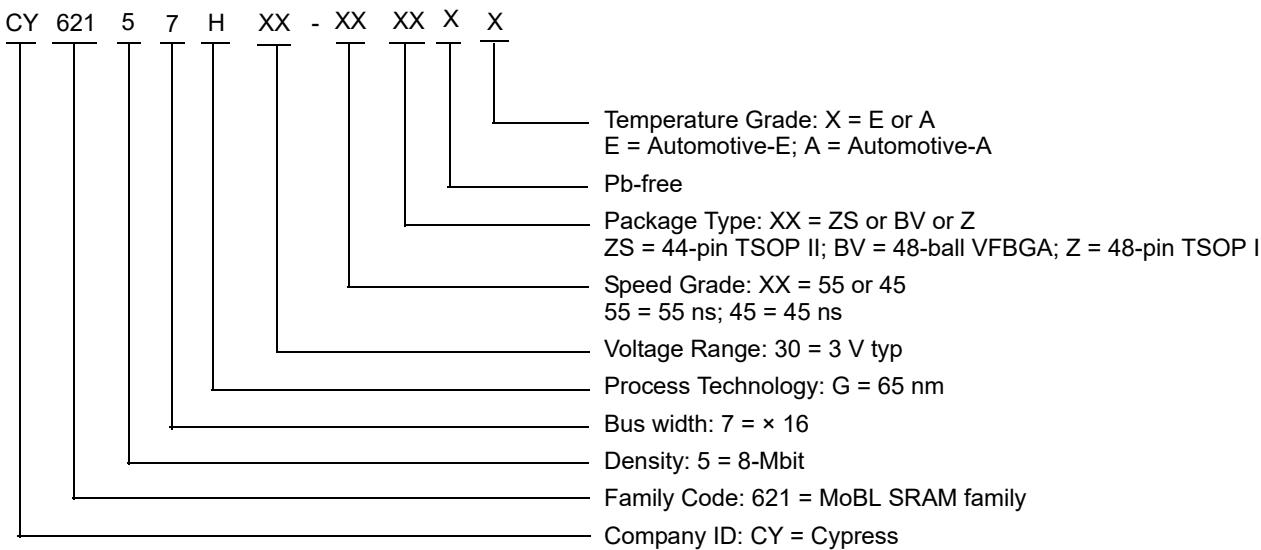
**Note**

36. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

## Ordering Information

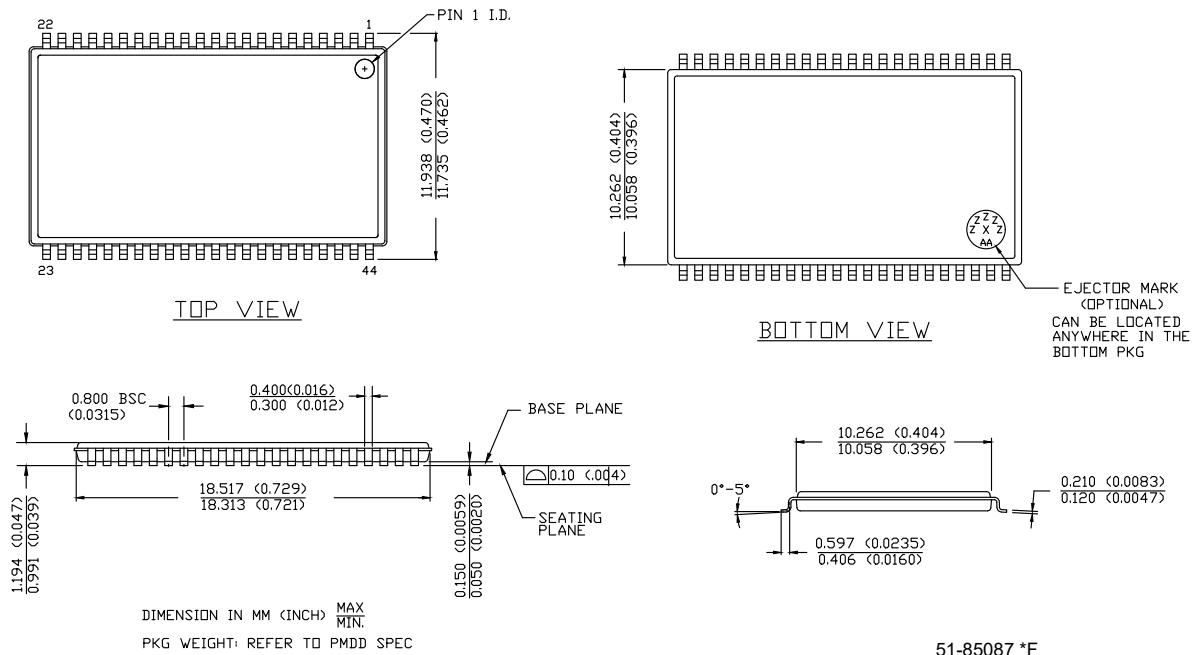
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62157G30-45ZSXA	51-85087	44-pin TSOP II (Pb-free)	Automotive-A
	CY62157G30-45BVXA	51-85150	48-ball VFBGA (6 × 8 × 1.0 mm) (Pb-free)	Automotive-A
	CY62157G30-45ZXA	51-85183	48-pin TSOP I (Pb-free)	Automotive-A

## Ordering Code Definitions



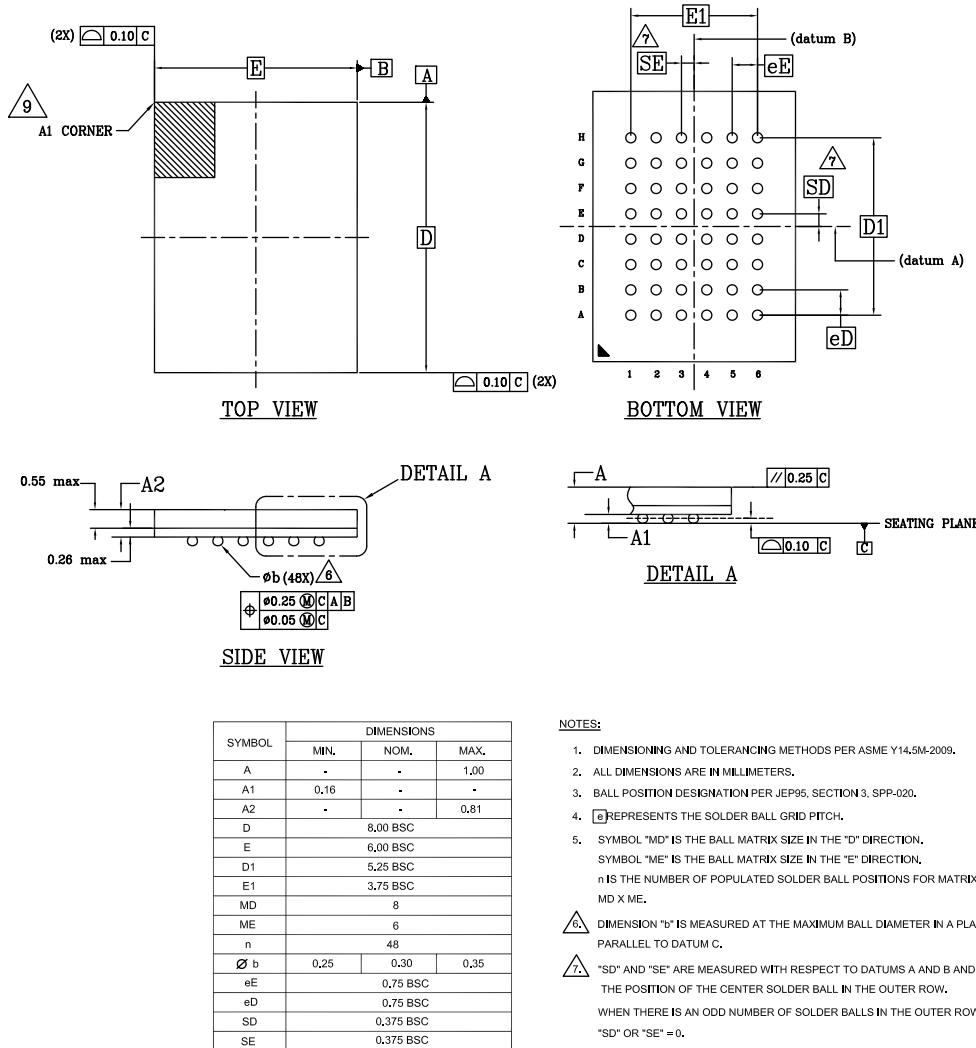
## Package Diagrams

**Figure 11. 44-pin TSOP II Package Outline, 51-85087**



## Package Diagrams (continued)

**Figure 12. 48-ball VFBGA (6 x 8 x 1.0 mm) Package Outline, 51-85150**



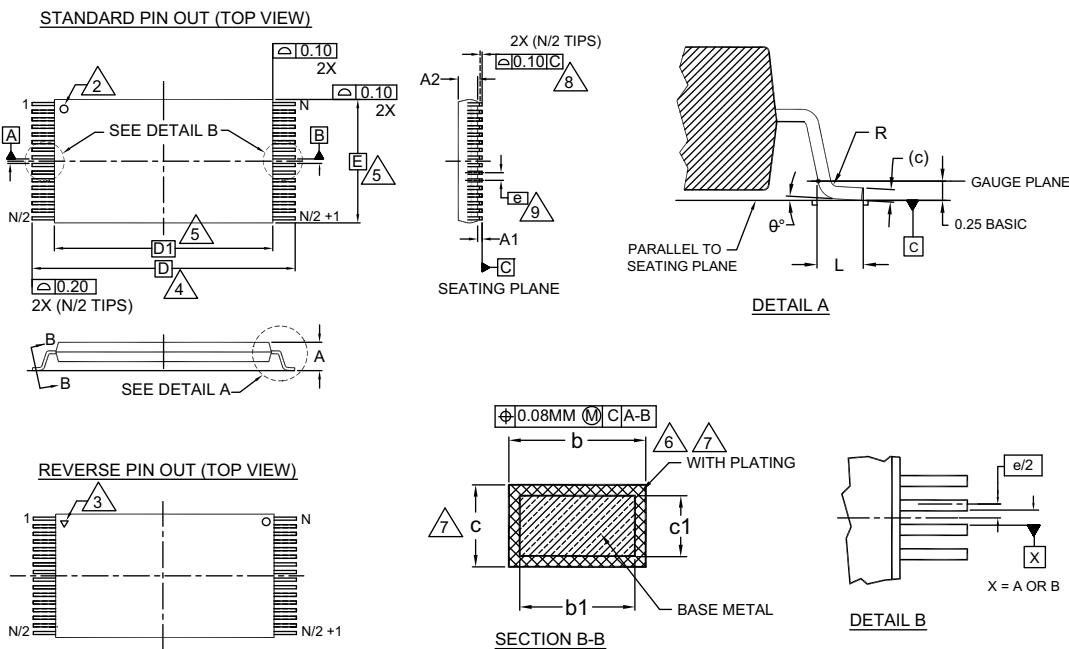
### NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4.  $\triangle$  REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION,  
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION,  
"n" IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE  
MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE  
PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE  
THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW,  
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW,  
"SD" OR "SE" = 0,  
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW,  
"SD" = eD/2 AND "SE" = eE/2.
8.  $^{*+}$  INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9.  $\triangle$  A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED  
MARK, INDENTATION OR OTHER MEANS.

51-85150 \*I

## Package Diagrams (continued)

Figure 13. 48-pin TSOP I (18.4 x 12 x 1.2 mm) Package Outline, 51-85183



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	20.00 BASIC		
D1	18.40 BASIC		
E	12.00 BASIC		
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8
R	0.08	—	0.20
N	48		

### NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS (mm).
- 2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
- 3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
- 4. TO BE DETERMINED AT THE SEATING PLANE [-C-]. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
- 5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
- 6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm .
- 7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- 8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
- 9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
- 10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 \*F

## Acronyms

**Table 1. Acronyms Used in this Document**

Acronym	Description
BHE	byte high enable
BLE	byte low enable
CE	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
OE	output enable
SRAM	static random access memory
TTL	Transistor-transistor logic
VFBGA	very fine-pitch ball grid array
WE	write enable

## Document Conventions

### Units of Measure

**Table 2. Units of Measure**

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microamperes
µs	microseconds
mA	milliamperes
mm	millimeters
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
V	volts
W	watts

**Document History Page**

Document Title: CY62157G Automotive, 8-Mbit (512K words × 16-bit) Static RAM with Error-Correcting Code (ECC)  
Document Number: 002-27989

Rev.	ECN No.	Submission Date	Description of Change
*D	6937006	09/09/2020	Changed datasheet status to Final.

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

### Products

Arm® Cortex® Microcontrollers	<a href="http://cypress.com/arm">cypress.com/arm</a>
Automotive	<a href="http://cypress.com/automotive">cypress.com/automotive</a>
Clocks & Buffers	<a href="http://cypress.com/clocks">cypress.com/clocks</a>
Interface	<a href="http://cypress.com/interface">cypress.com/interface</a>
Internet of Things	<a href="http://cypress.com/iot">cypress.com/iot</a>
Memory	<a href="http://cypress.com/memory">cypress.com/memory</a>
Microcontrollers	<a href="http://cypress.com/mcu">cypress.com/mcu</a>
PSoC	<a href="http://cypress.com/psoc">cypress.com/psoc</a>
Power Management ICs	<a href="http://cypress.com/pmic">cypress.com/pmic</a>
Touch Sensing	<a href="http://cypress.com/touch">cypress.com/touch</a>
USB Controllers	<a href="http://cypress.com/usb">cypress.com/usb</a>
Wireless Connectivity	<a href="http://cypress.com/wireless">cypress.com/wireless</a>

### PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

### Cypress Developer Community

[Community](#) | [Code Examples](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

### Technical Support

[cypress.com/support](http://cypress.com/support)

---

© Cypress Semiconductor Corporation, 2019–2020. This document is the property of Cypress Semiconductor Corporation and its subsidiaries ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress shall have no liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. CYPRESS DOES NOT REPRESENT, WARRANT, OR GUARANTEE THAT CYPRESS PRODUCTS, OR SYSTEMS CREATED USING CYPRESS PRODUCTS, WILL BE FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (collectively, "Security Breach"). Cypress disclaims any liability relating to any Security Breach, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any Security Breach. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. "High-Risk Device" means any device or system whose failure could cause personal injury, death, or property damage. Examples of High-Risk Devices are weapons, nuclear installations, surgical implants, and other medical devices. "Critical Component" means any component of a High-Risk Device whose failure to perform can be reasonably expected to cause, directly or indirectly, the failure of the High-Risk Device, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any use of a Cypress product as a Critical Component in a High-Risk Device. You shall indemnify and hold Cypress, its directors, officers, employees, agents, affiliates, distributors, and assigns harmless from and against all claims, costs, damages, and expenses, arising out of any claim, including claims for product liability, personal injury or death, or property damage arising from any use of a Cypress product as a Critical Component in a High-Risk Device. Cypress products are not intended or authorized for use as a Critical Component in any High-Risk Device except to the limited extent that (i) Cypress's published data sheet for the product explicitly states Cypress has qualified the product for use in a specific High-Risk Device, or (ii) Cypress has given you advance written authorization to use the product as a Critical Component in the specific High-Risk Device and you have signed a separate indemnification agreement.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit [cypress.com](http://cypress.com). Other names and brands may be claimed as property of their respective owners.